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FLOOR PLAN

Fig. 1.

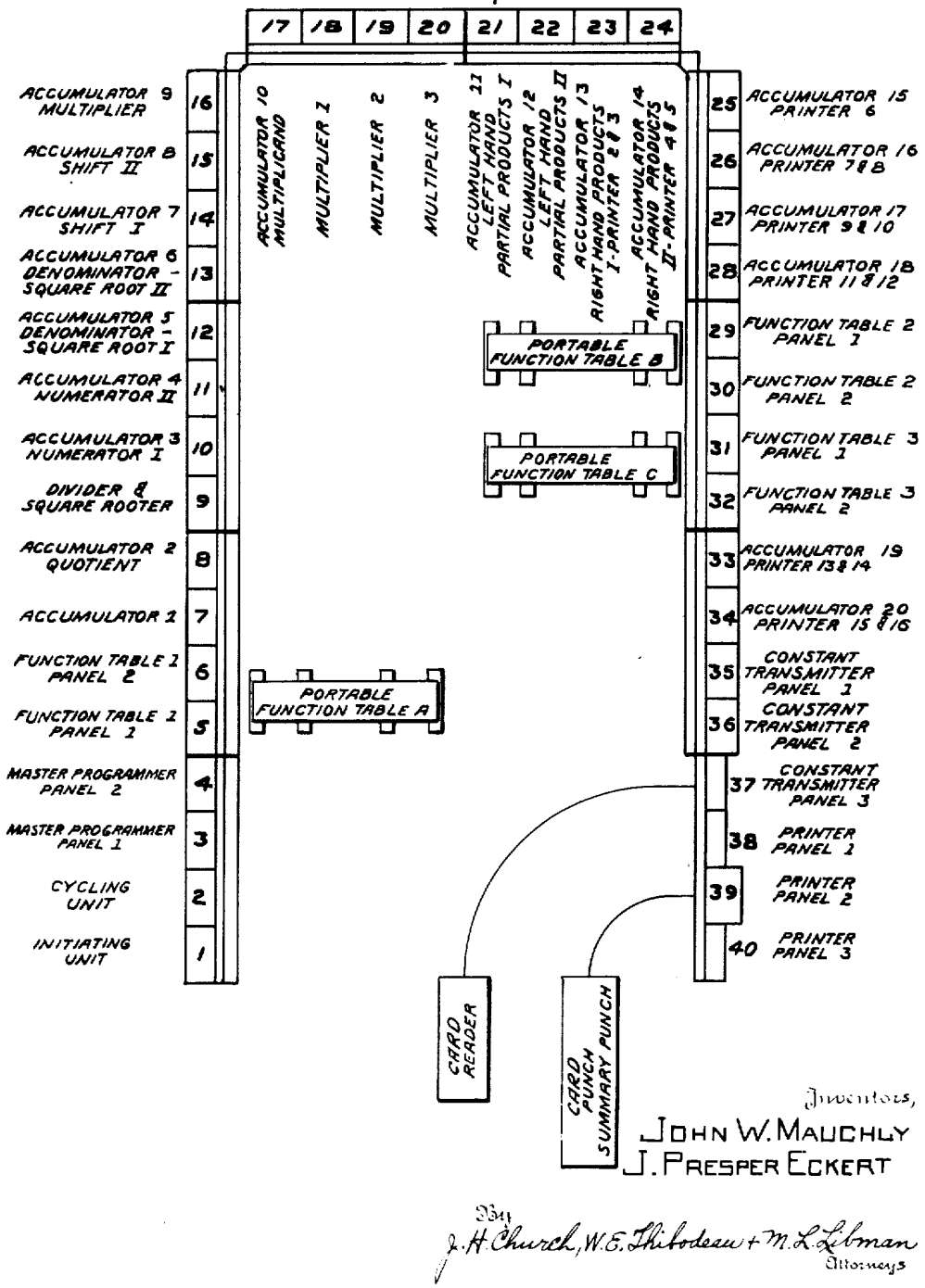

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Fig. 15A ELEMENTARY CYCLING UNIT

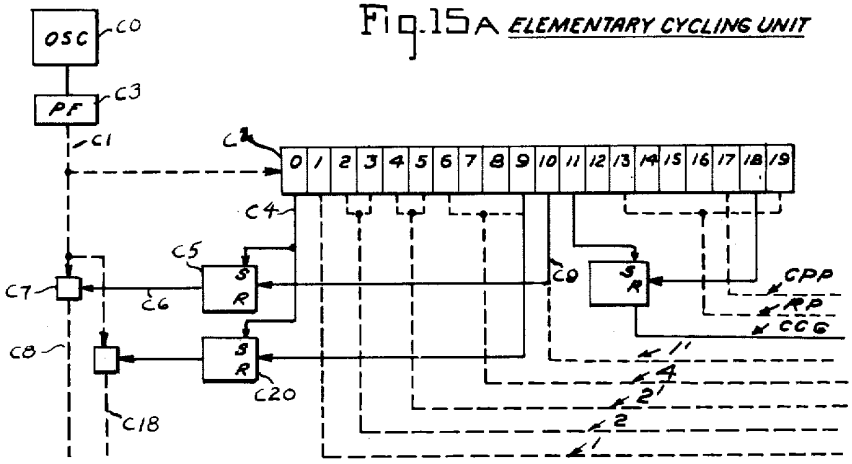

Fig. 2. CYCLING UNIT PULSES AND GATES

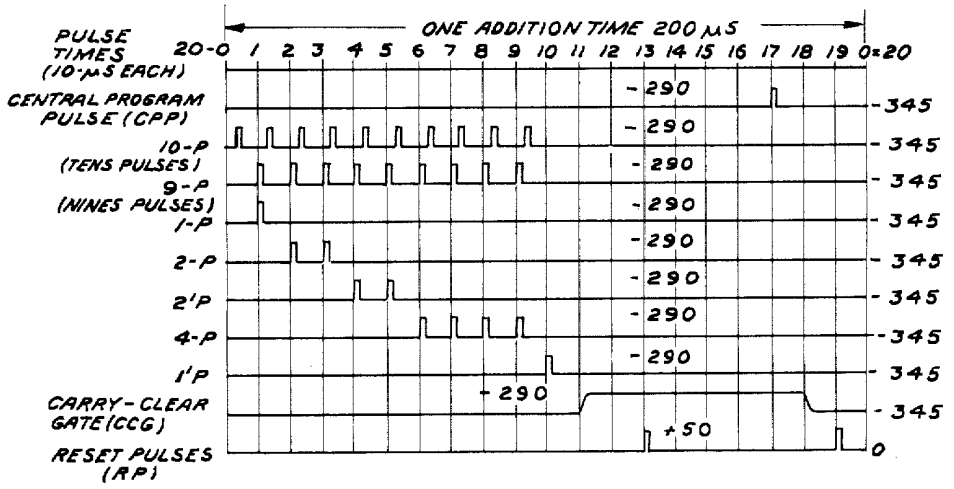

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Fig. 3. FLIP-FLOP CIRCUIT

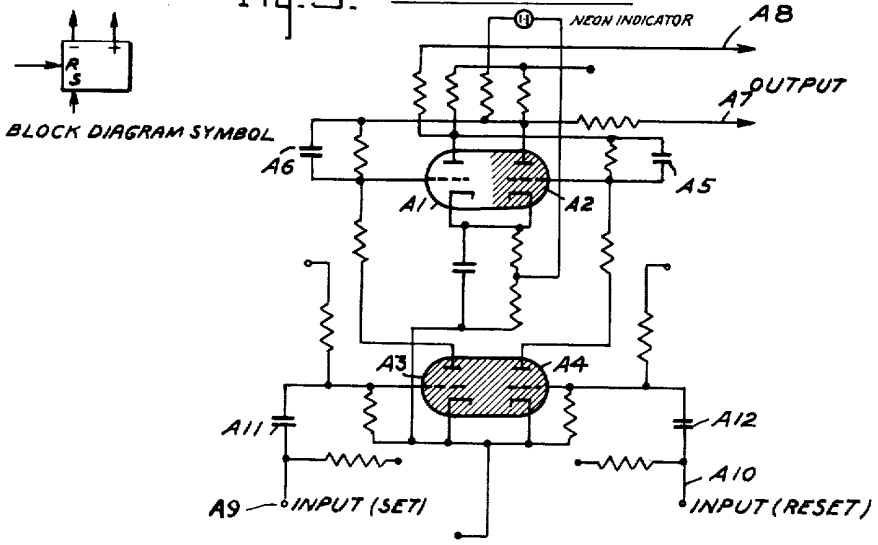
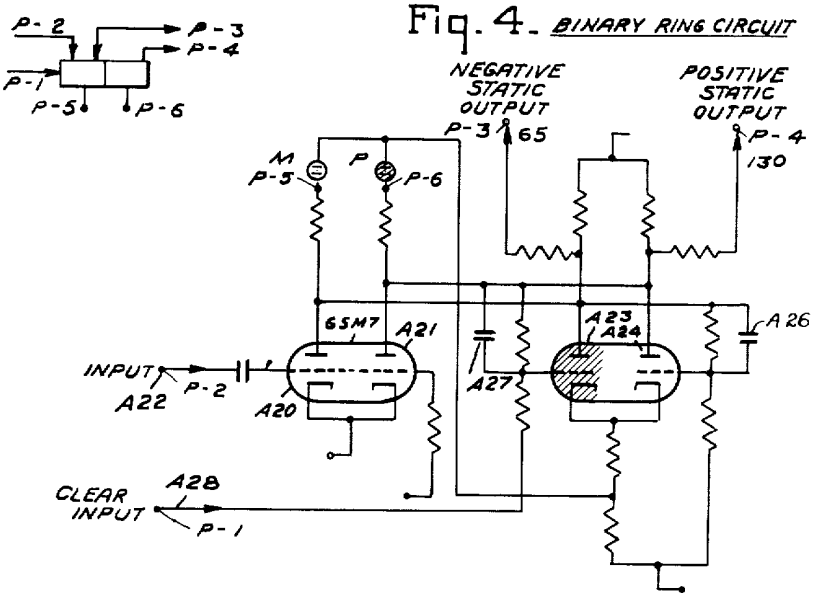


Fig. 4. BINARY RING CIRCUIT



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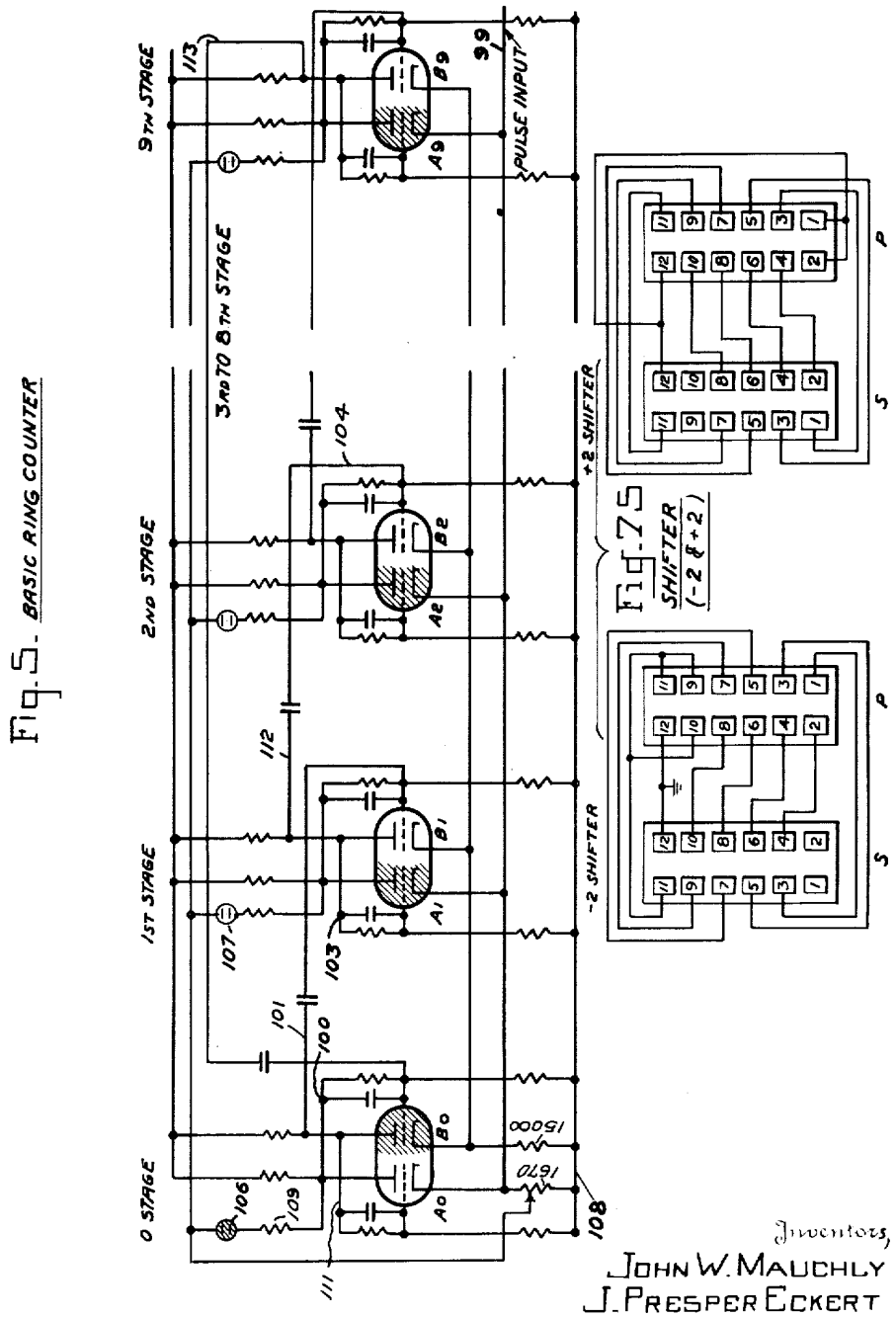

Fig. 5. BASIC RING COUNTER

Fig. 7.5 SHIFTER (-2 & +2)

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Fig. 6. GATE TUBES

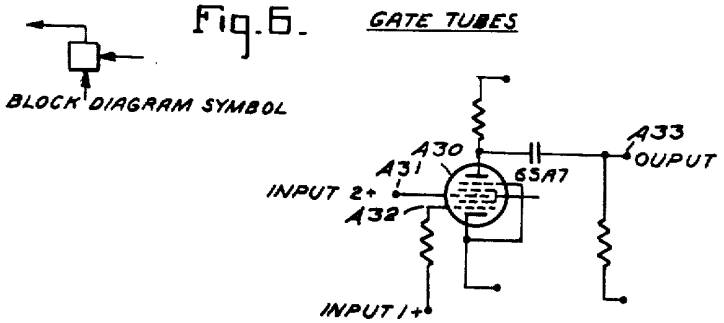


Fig. 7.

TRIPLE COINCIDENCE CIRCUIT USED IN F.T.

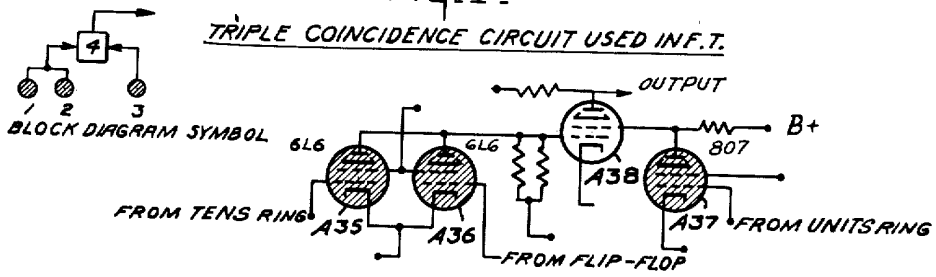
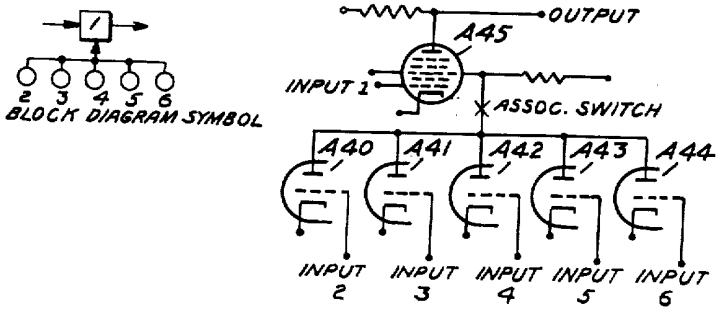


Fig. 8.

MULTIPLE COINCIDENCE CIRCUIT USED IN MASTER PROGRAM



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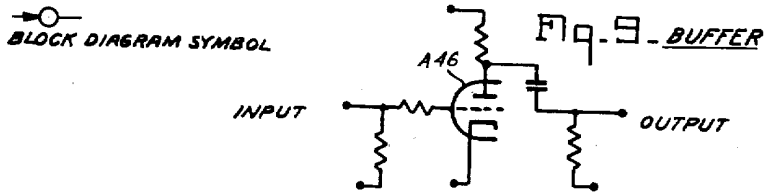


Fig. 9 - BUFFER

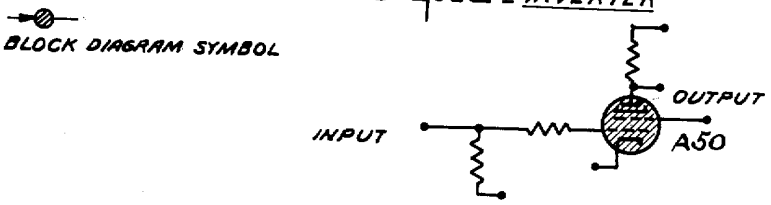
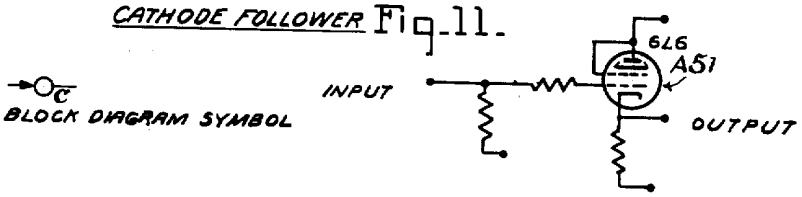


Fig. 10 - INVERTER



CATHODE FOLLOWER Fig. 11.

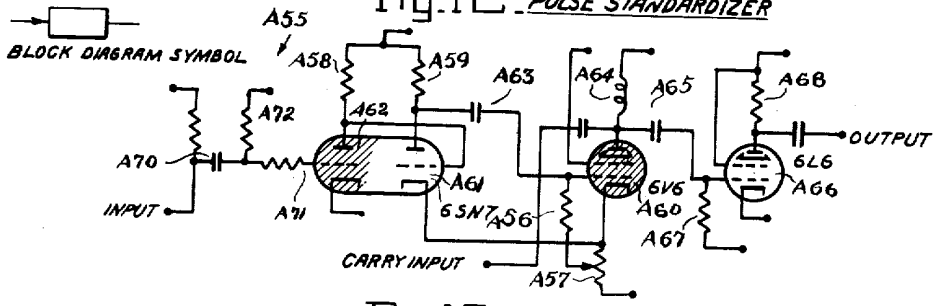


Fig. 12 - PULSE STANDARDIZER

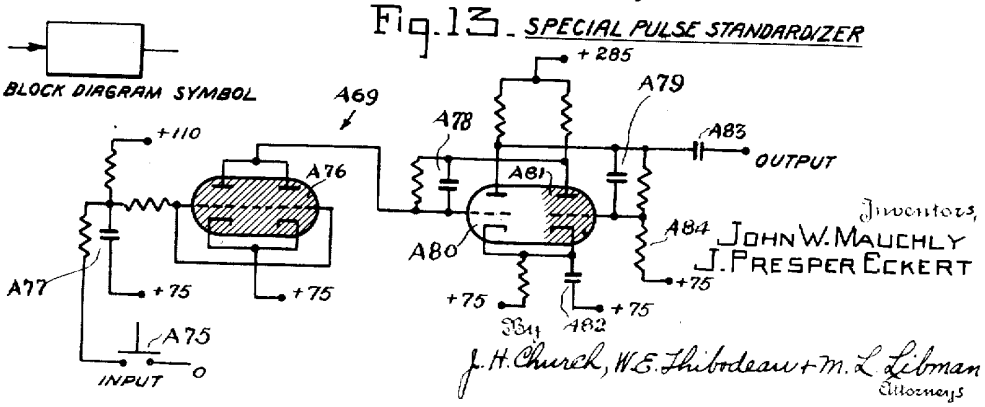


Fig. 13 - SPECIAL PULSE STANDARDIZER

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TRANSMITTER

Fig. 14

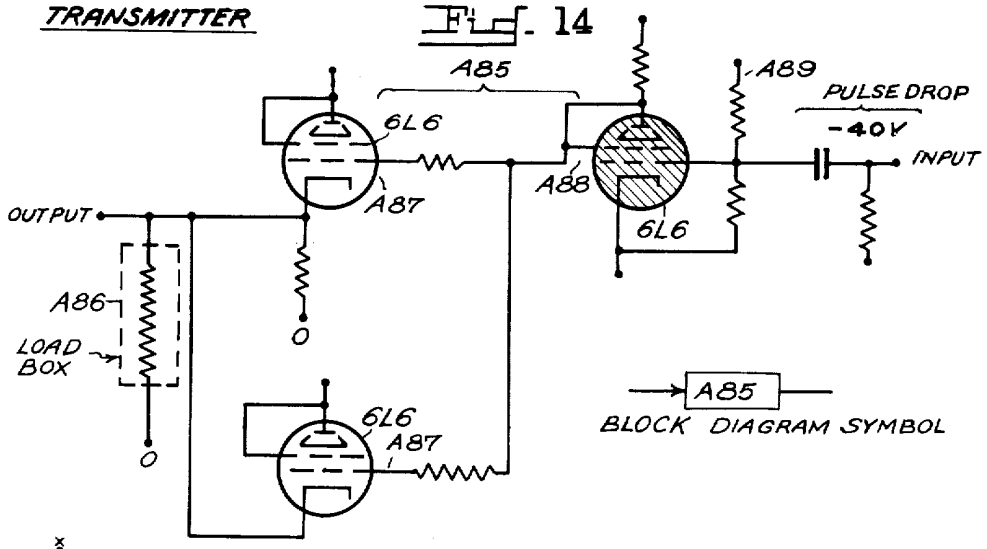
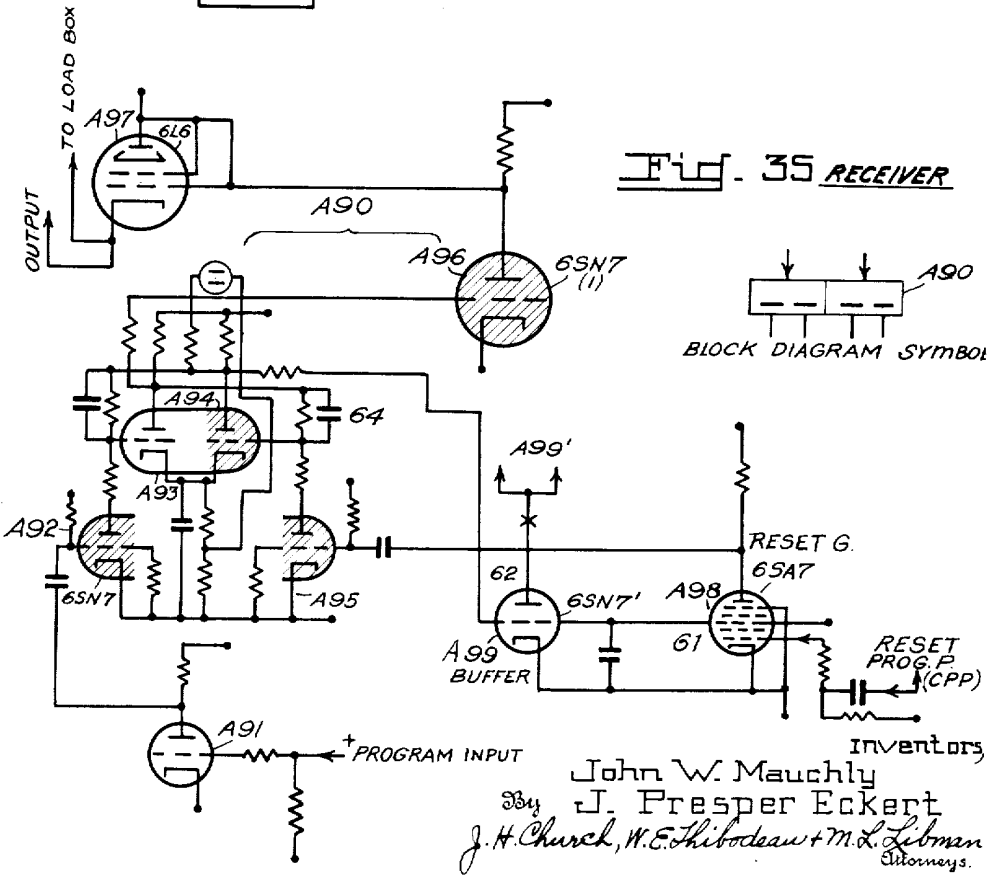


Fig. 35 RECEIVER



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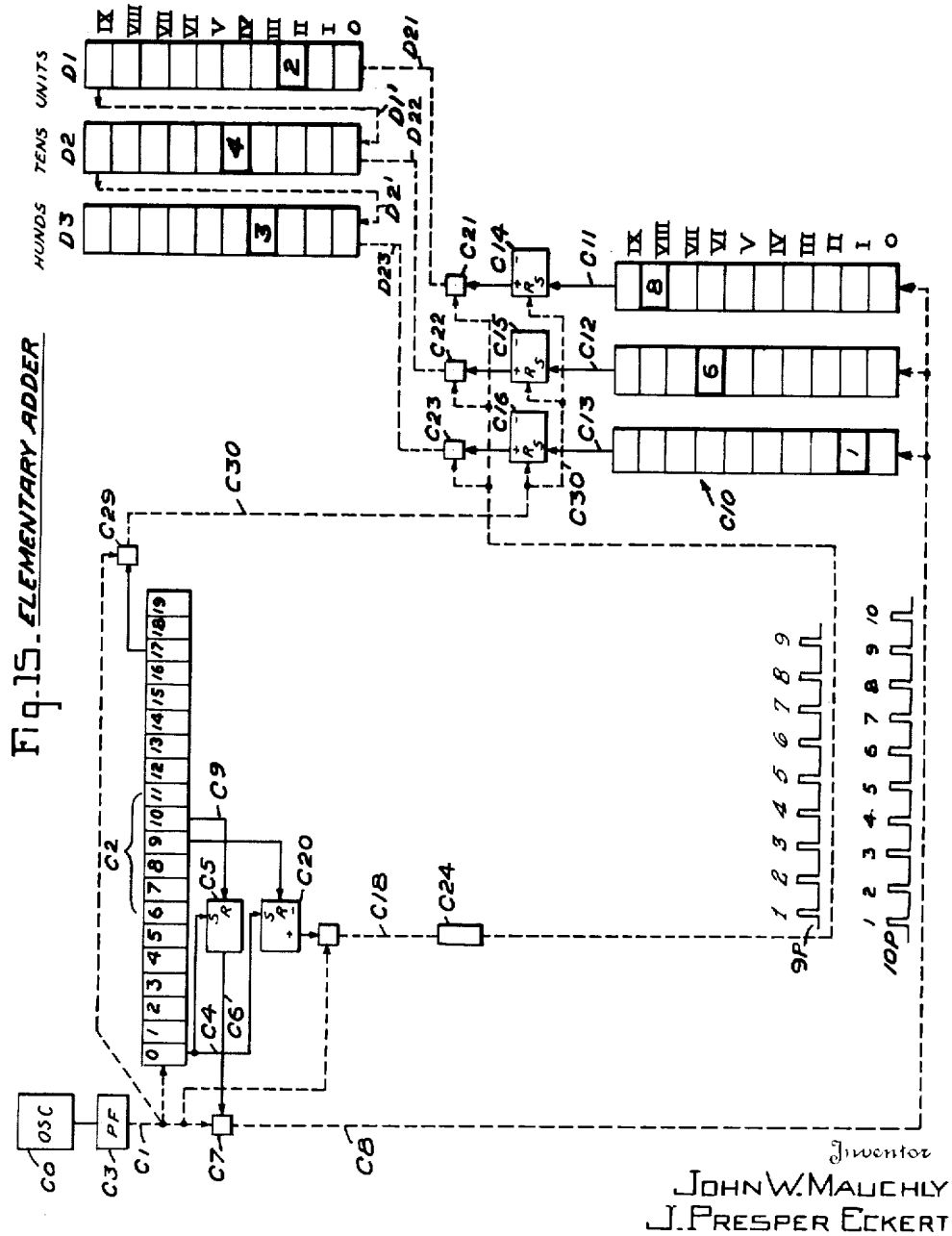

Fig. 15. ELEMENTARY ADDER

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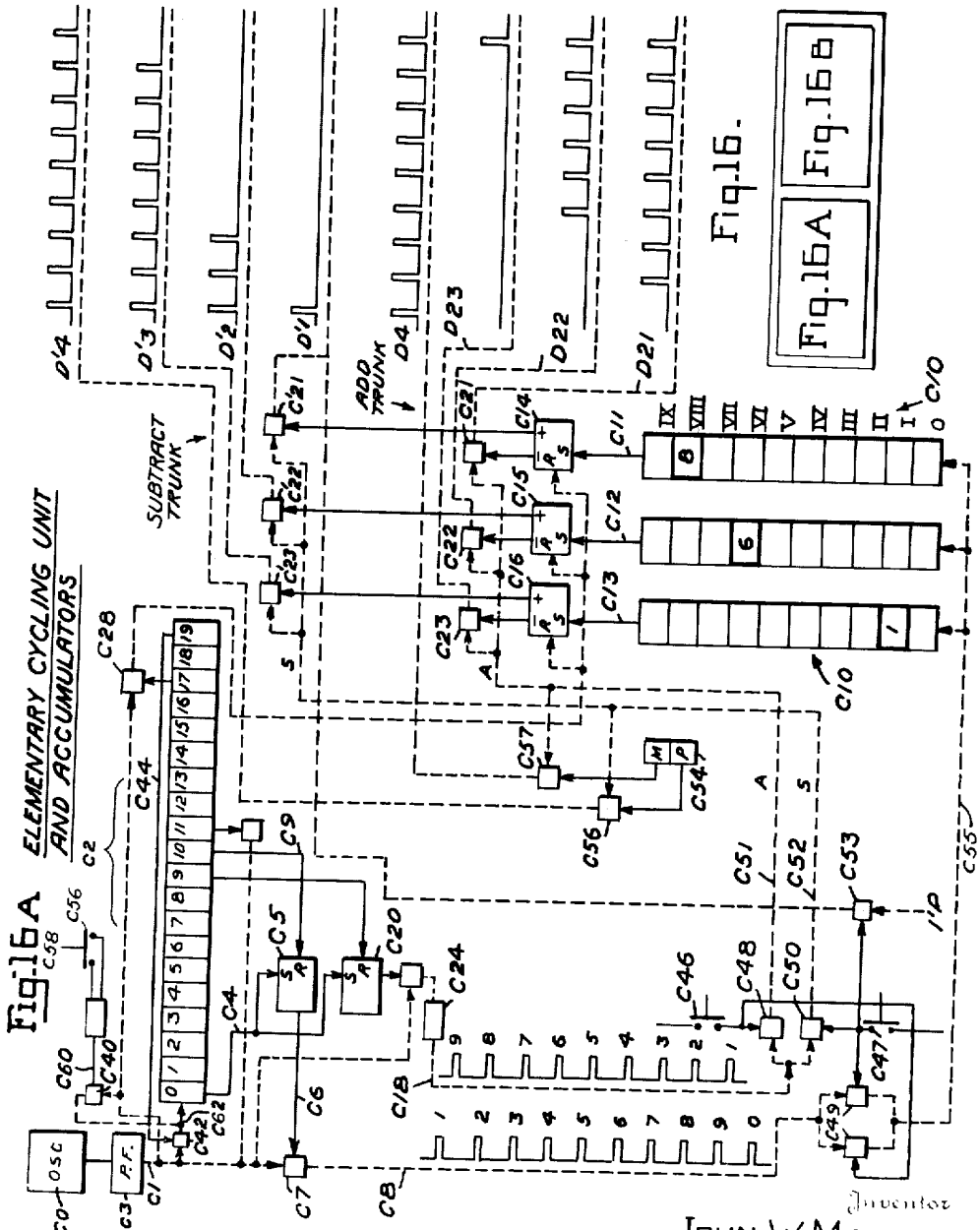

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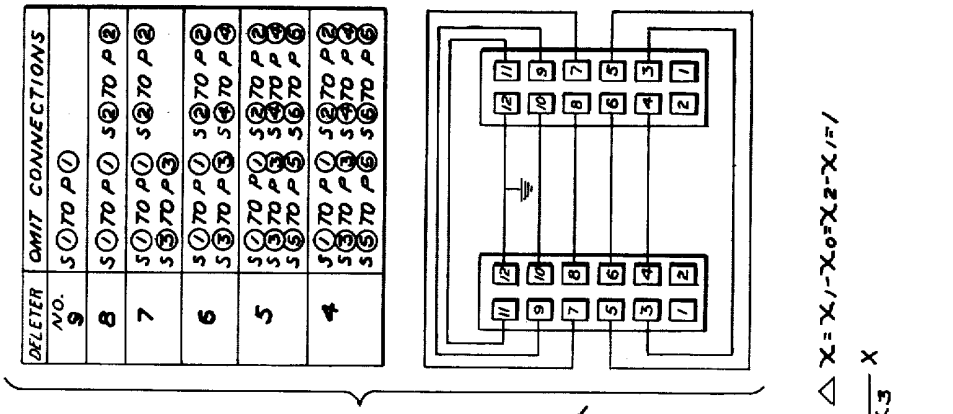

Fig.74 DELETERS

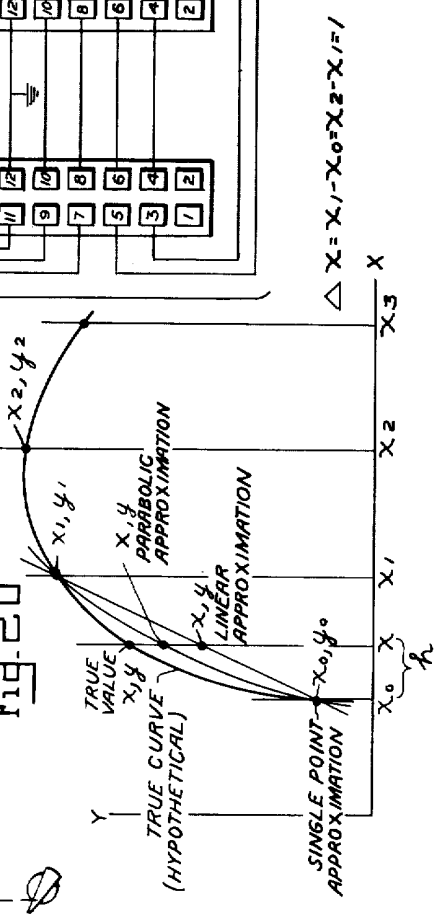

Fig.20

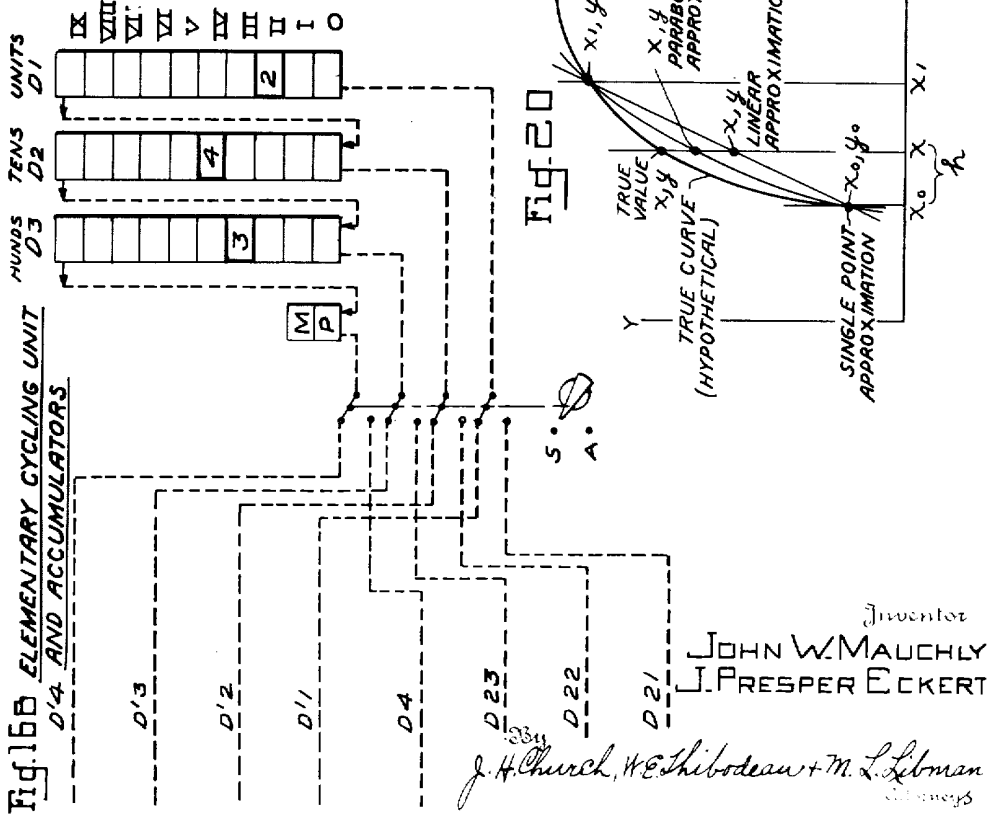

Fig.16B ELEMENTARY CYCLING UNIT D'4 AND ACCUMULATORS

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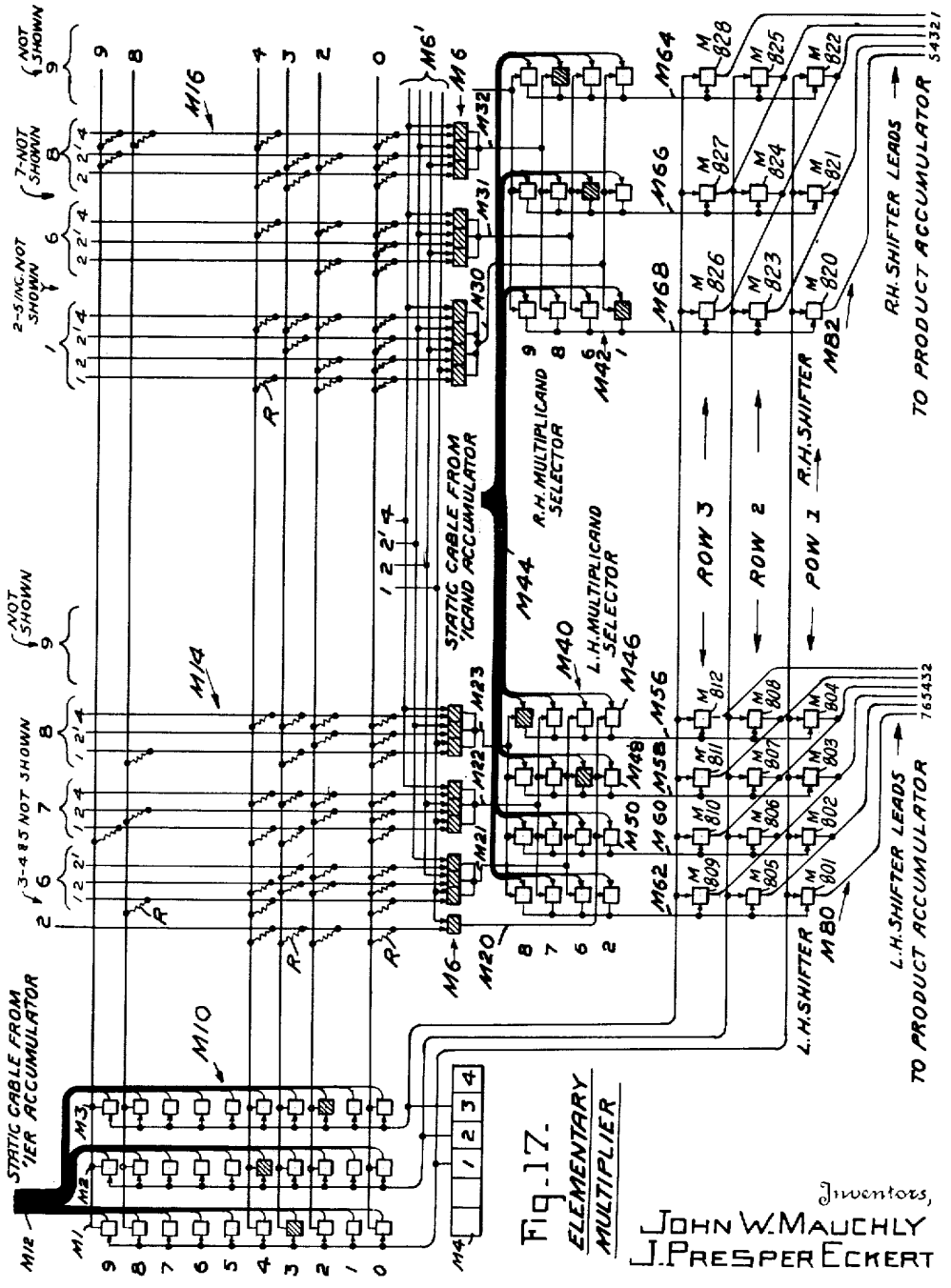

Fig. 17.
ELEMENTARY MULTIPLIER

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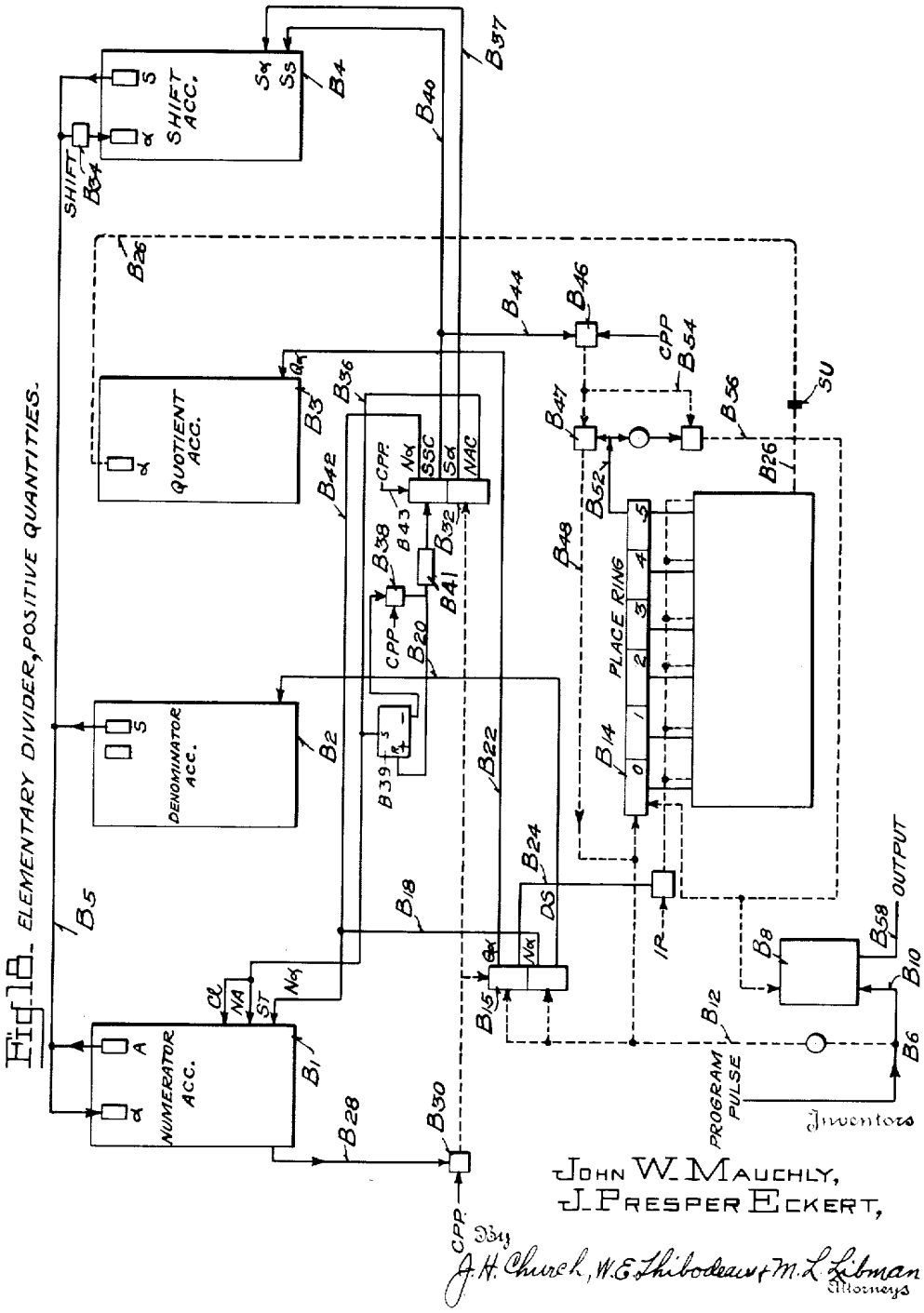

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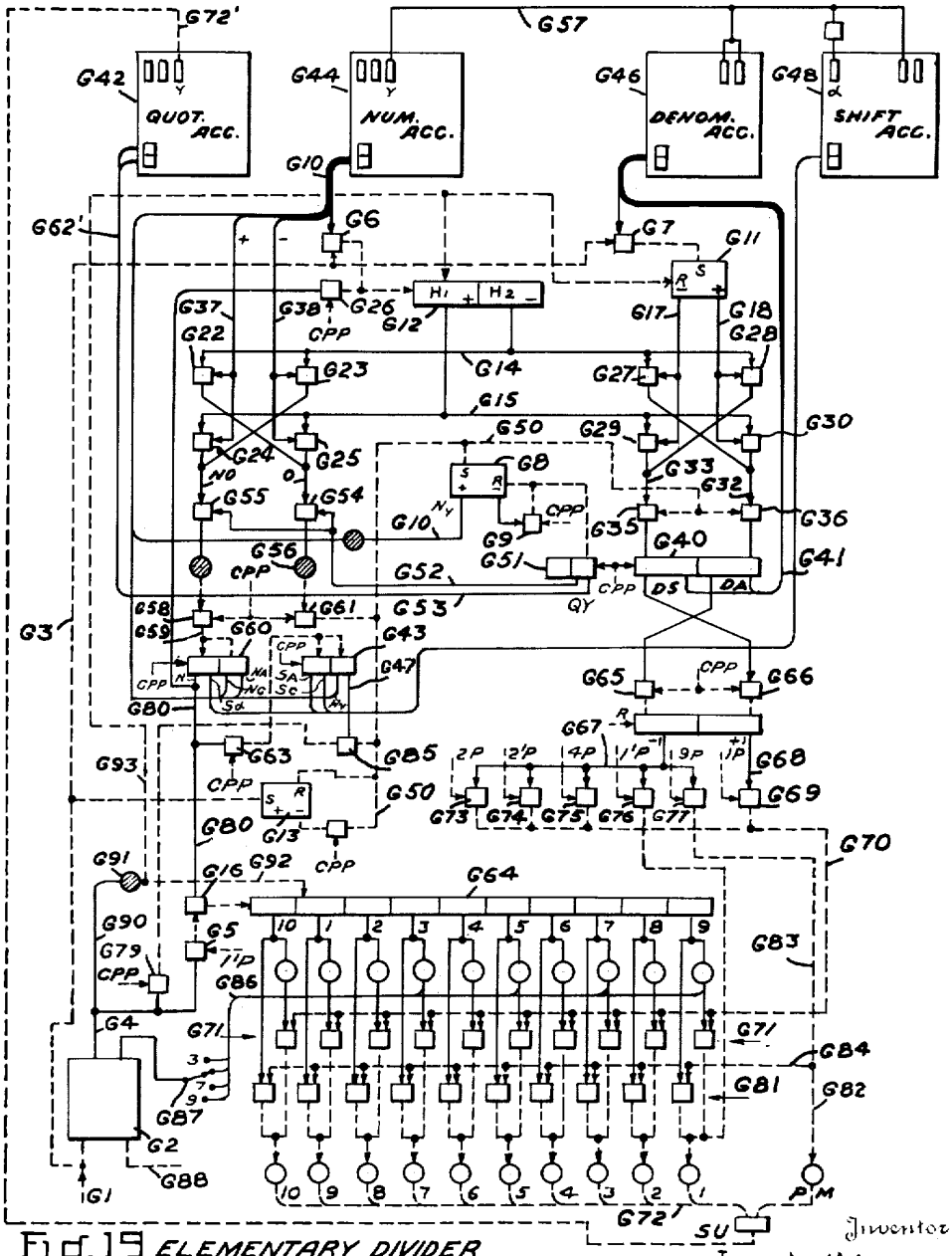

Fig. 19 ELEMENTARY DIVIDER SIGNED QUANTITIES

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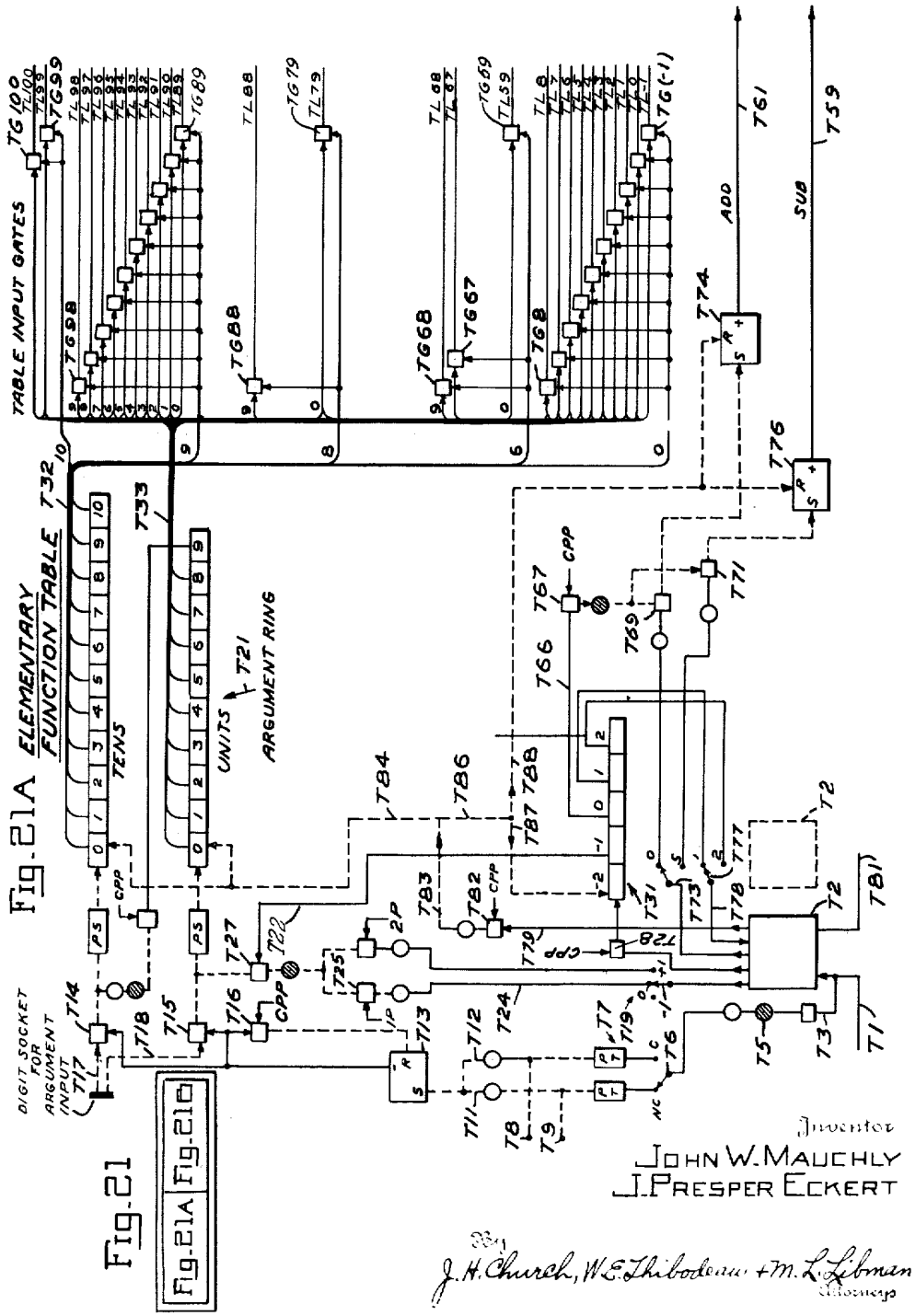

Fig. 21A

Fig. 21

Fig. 21A | Fig. 21B

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Fig. 21b
ELEMENTARY FUNCTION TABLE

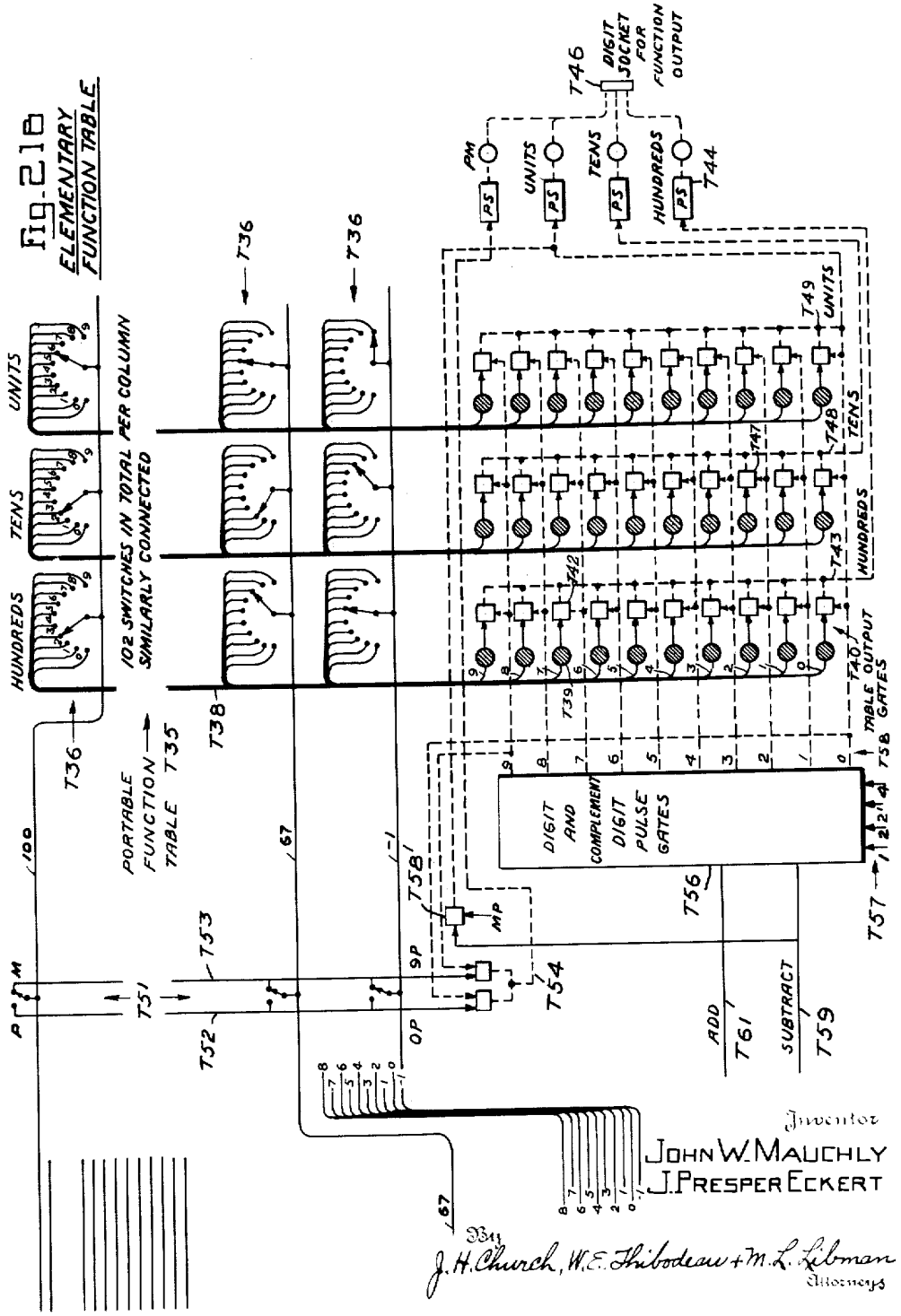

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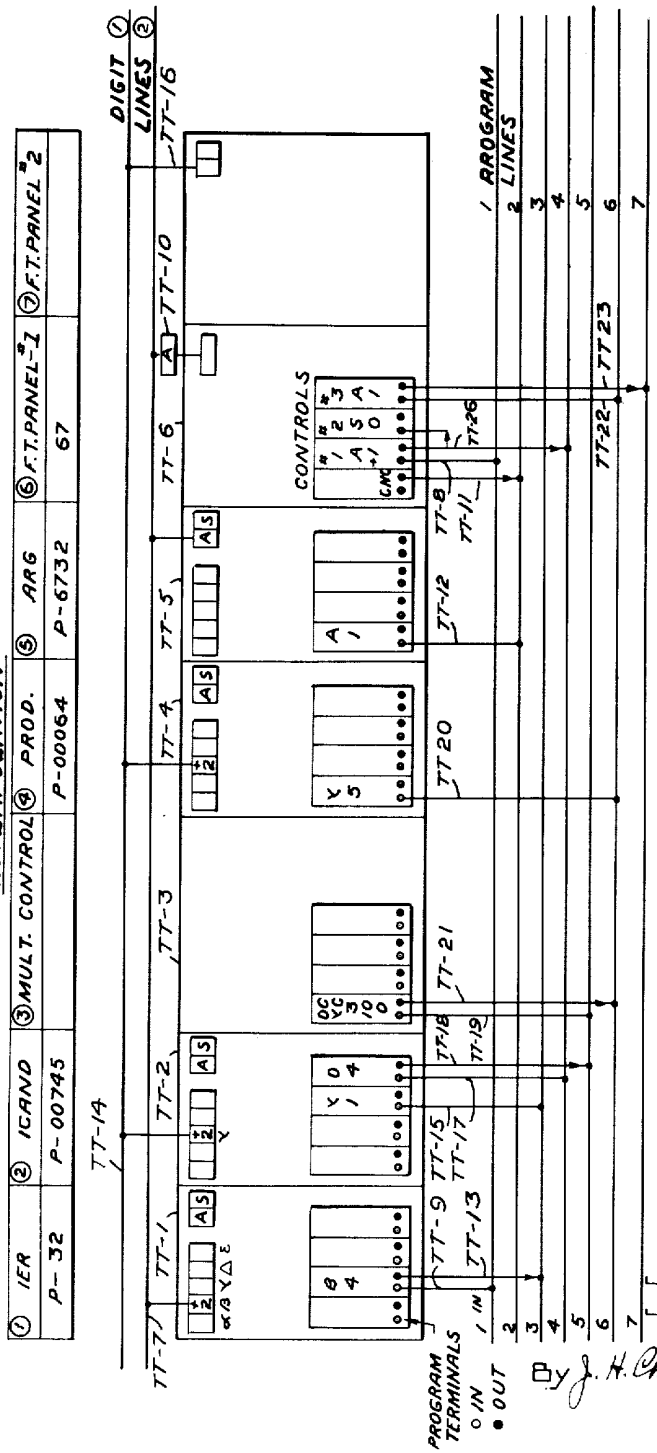
Fig. 22 ELEMENTARY LINEAR INTERPOLATION



① IER	② ICAND	③ MULT. CONTROL	④ PROD.	⑤ ARG	⑥ F.T. PANEL #1	⑦ F.T. PANEL #2
P-32	P-00745		P-00064	P-6732	67	

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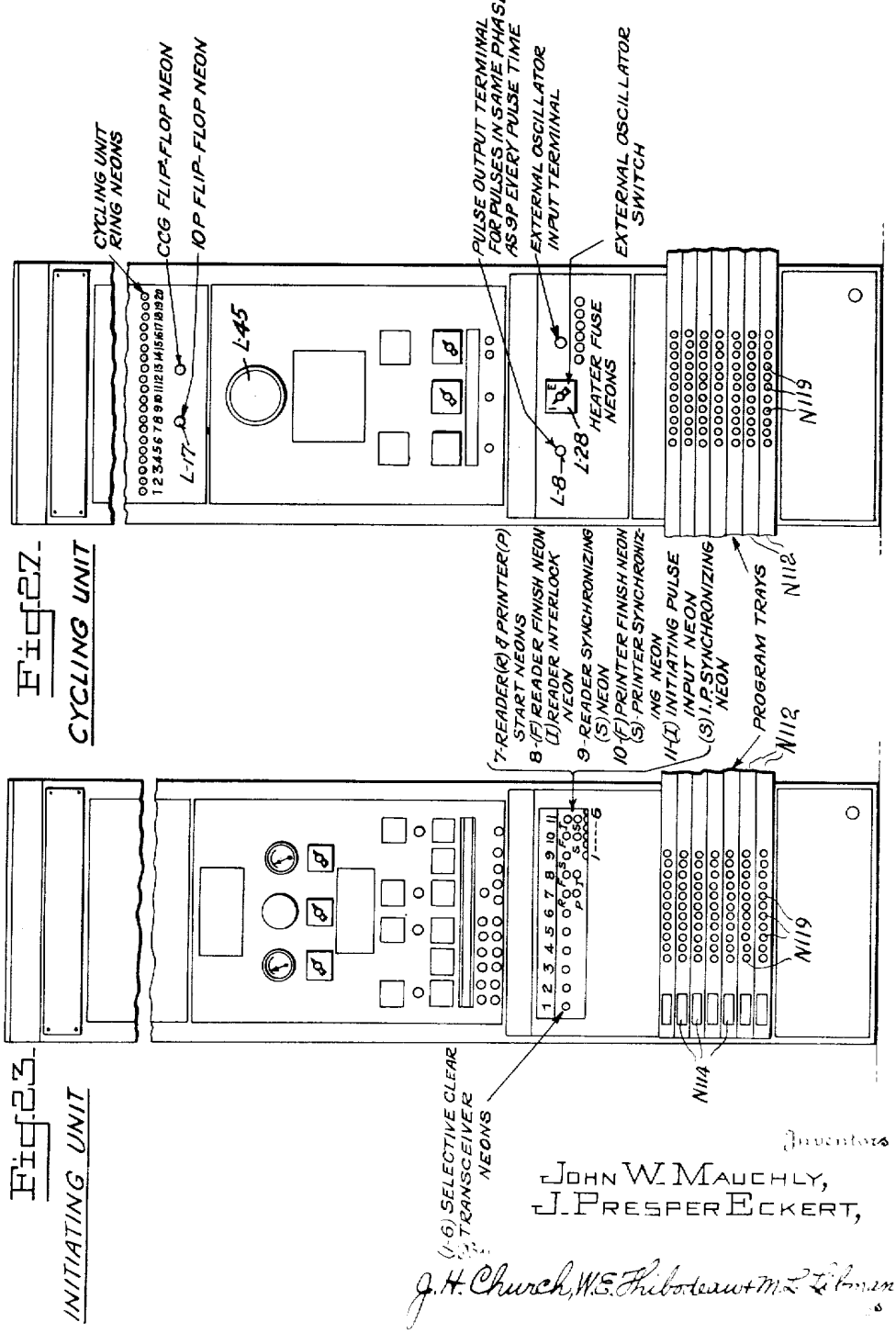

Fig 27. CYCLING UNIT

Fig 23. INITIATING UNIT

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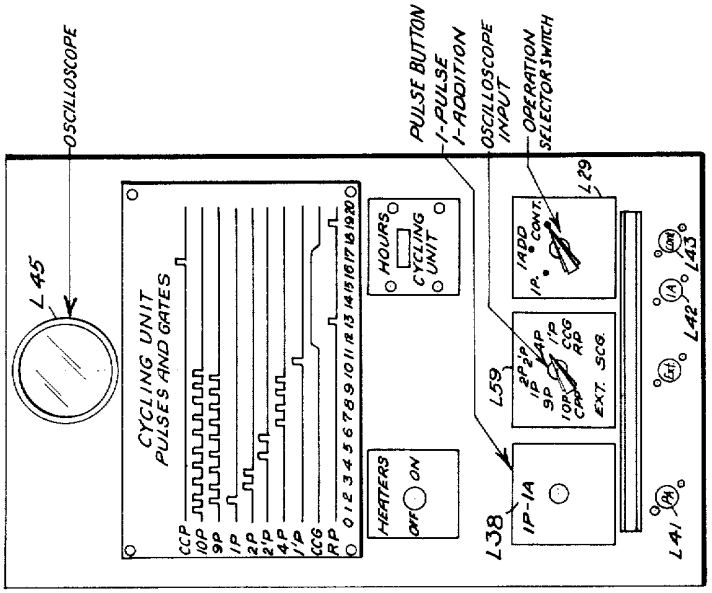

Fig. 28.
CYCLING UNIT

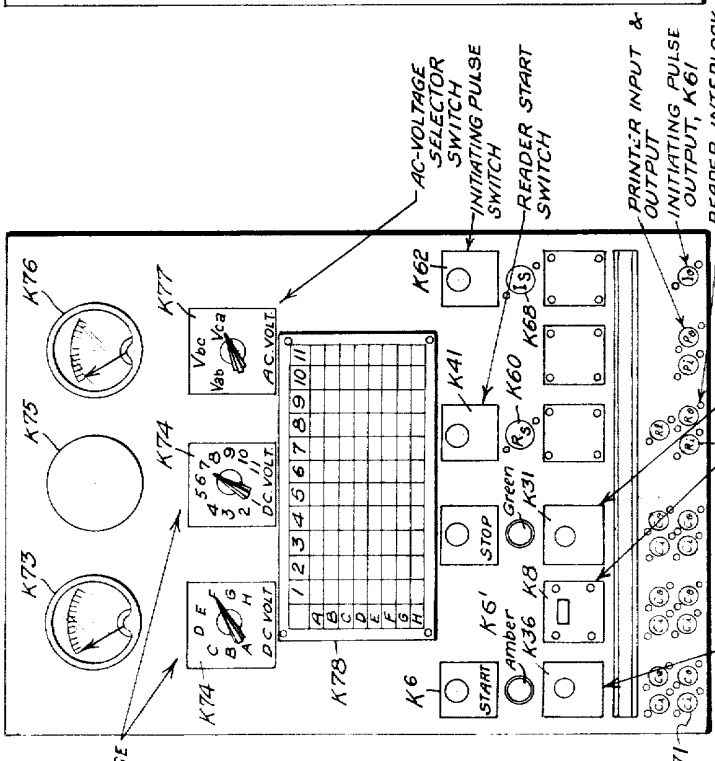

Fig. 24.
INITIATING UNIT

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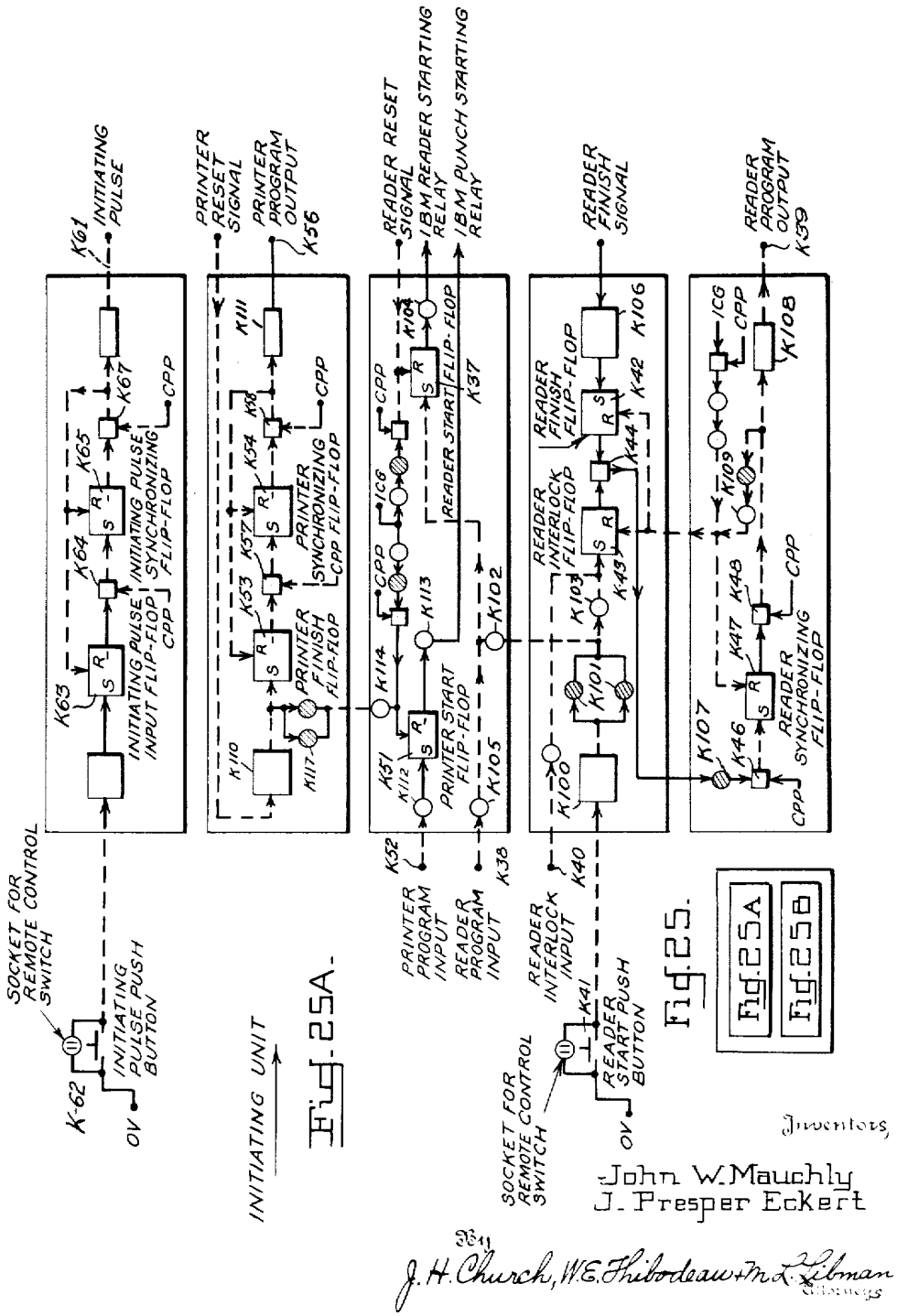

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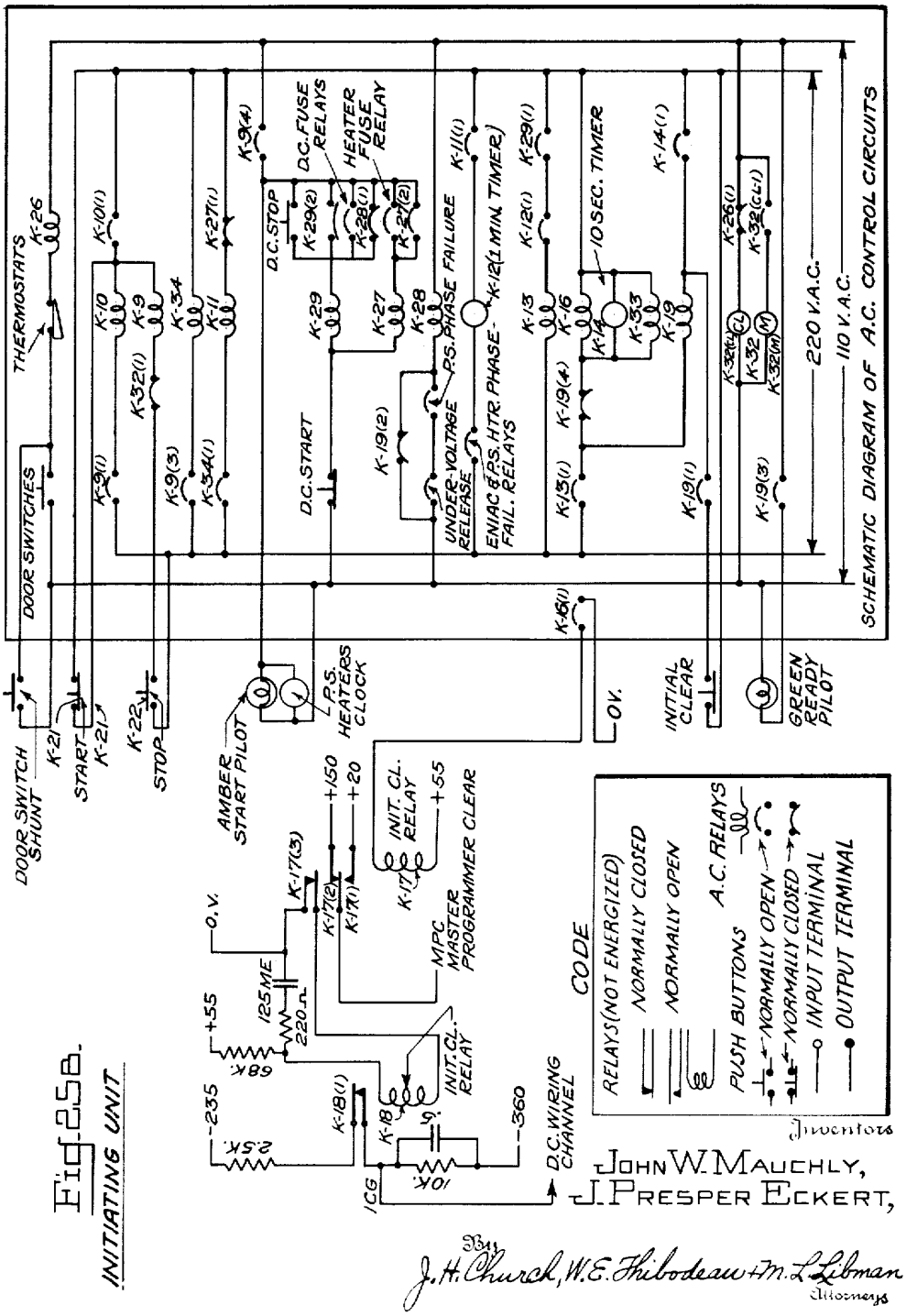

Fig. 25B.

INITIATING UNIT

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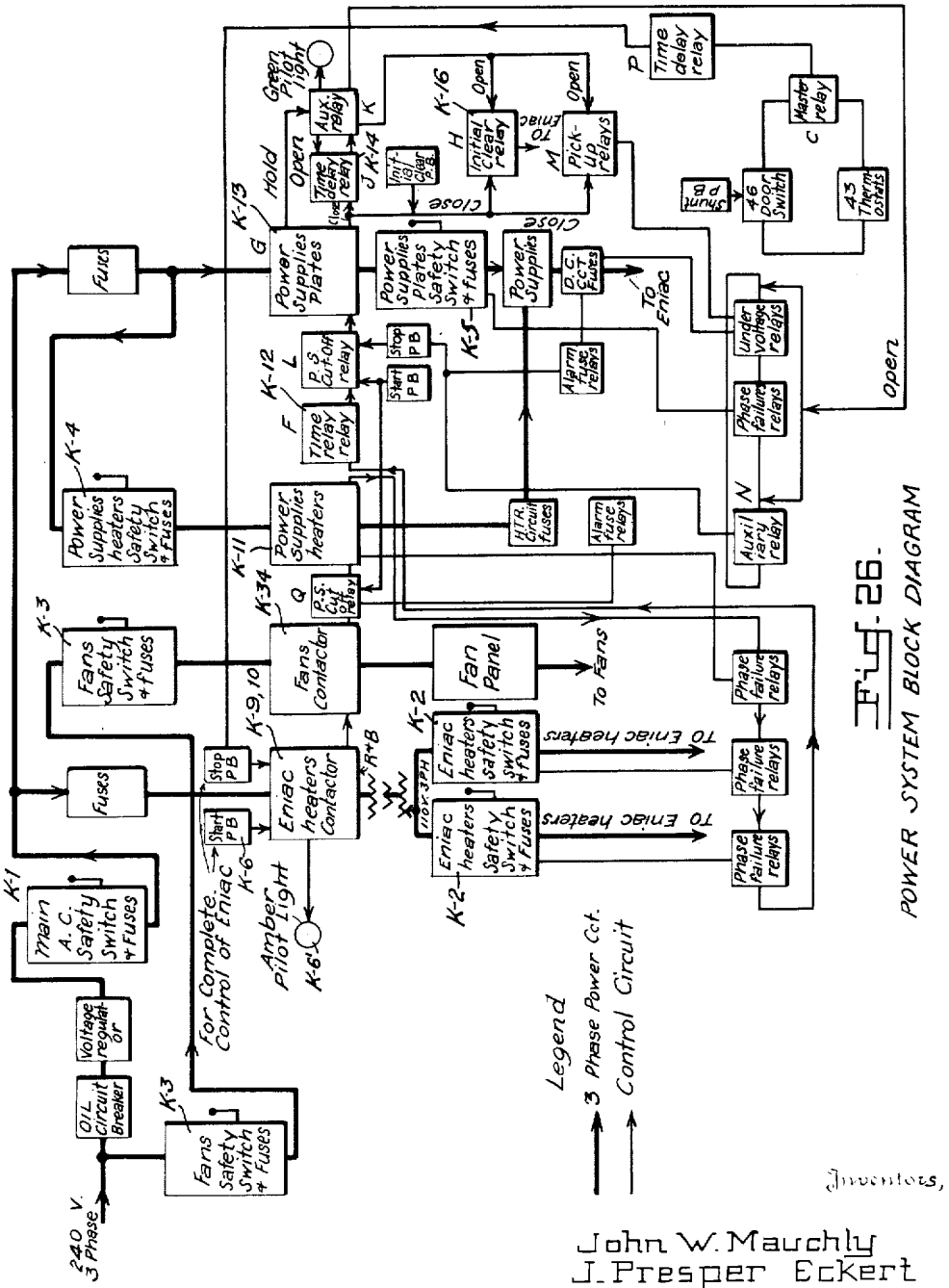

Fig. 26.

POWER SYSTEM BLOCK DIAGRAM

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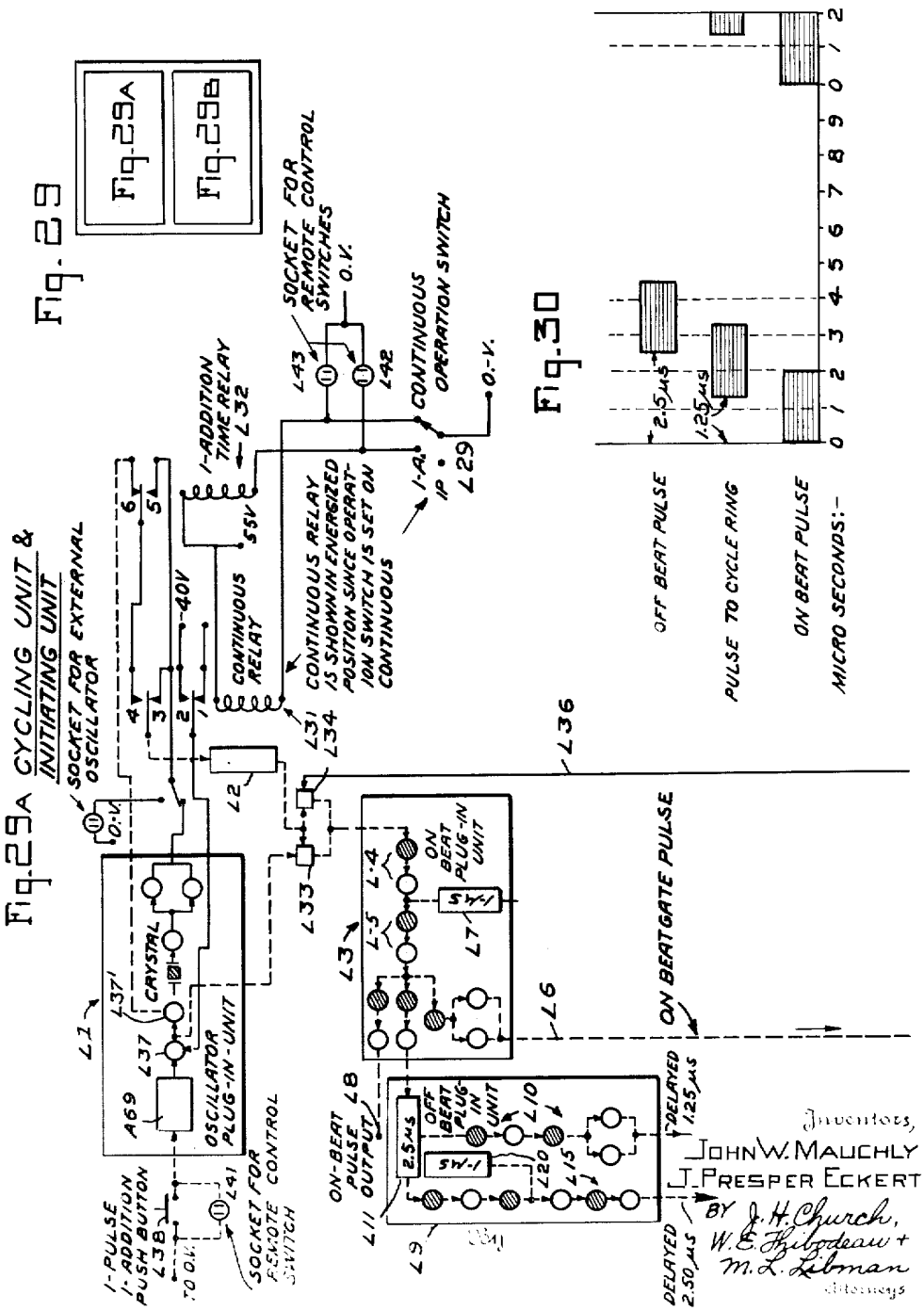

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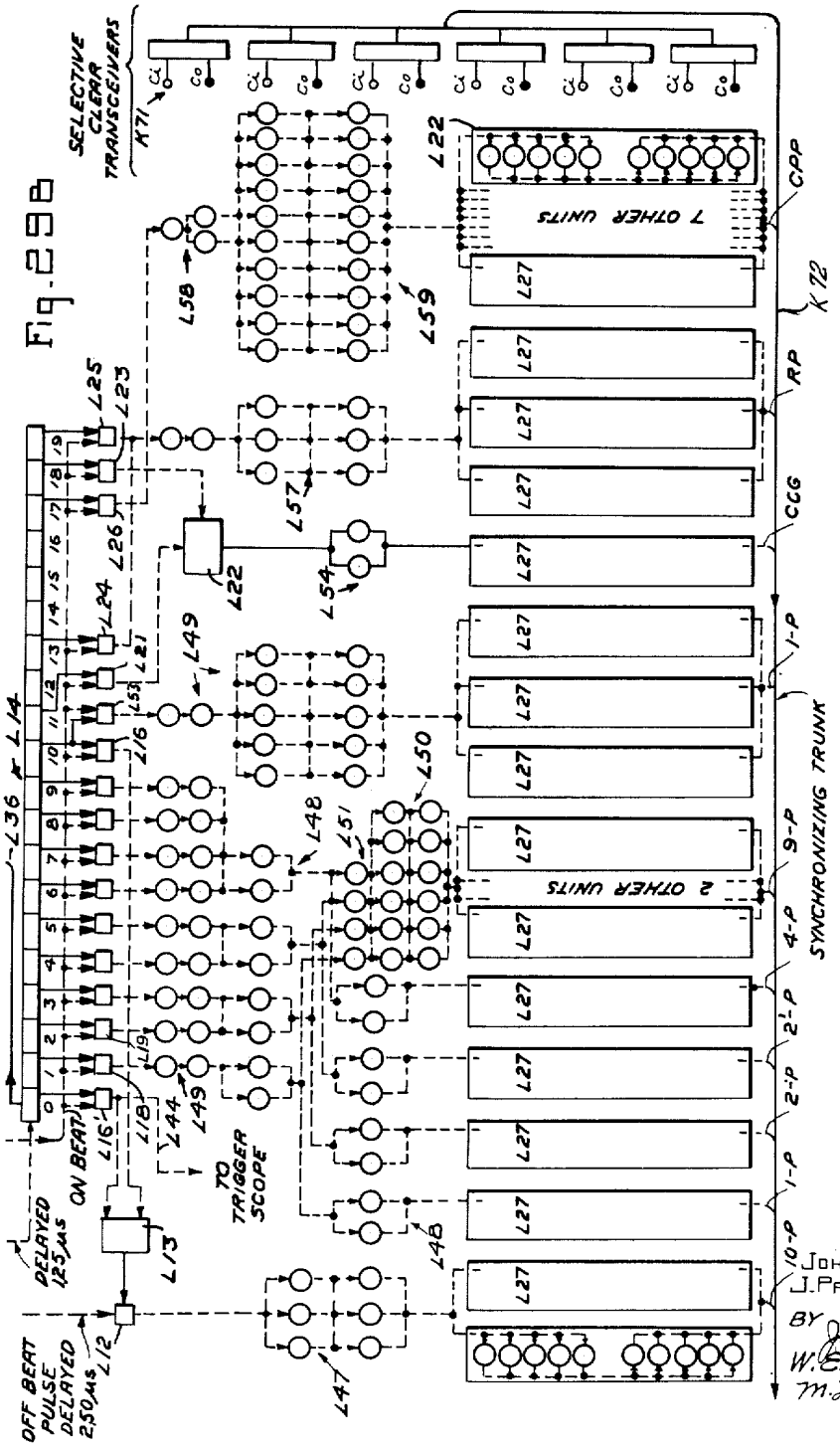
Fig. 29B



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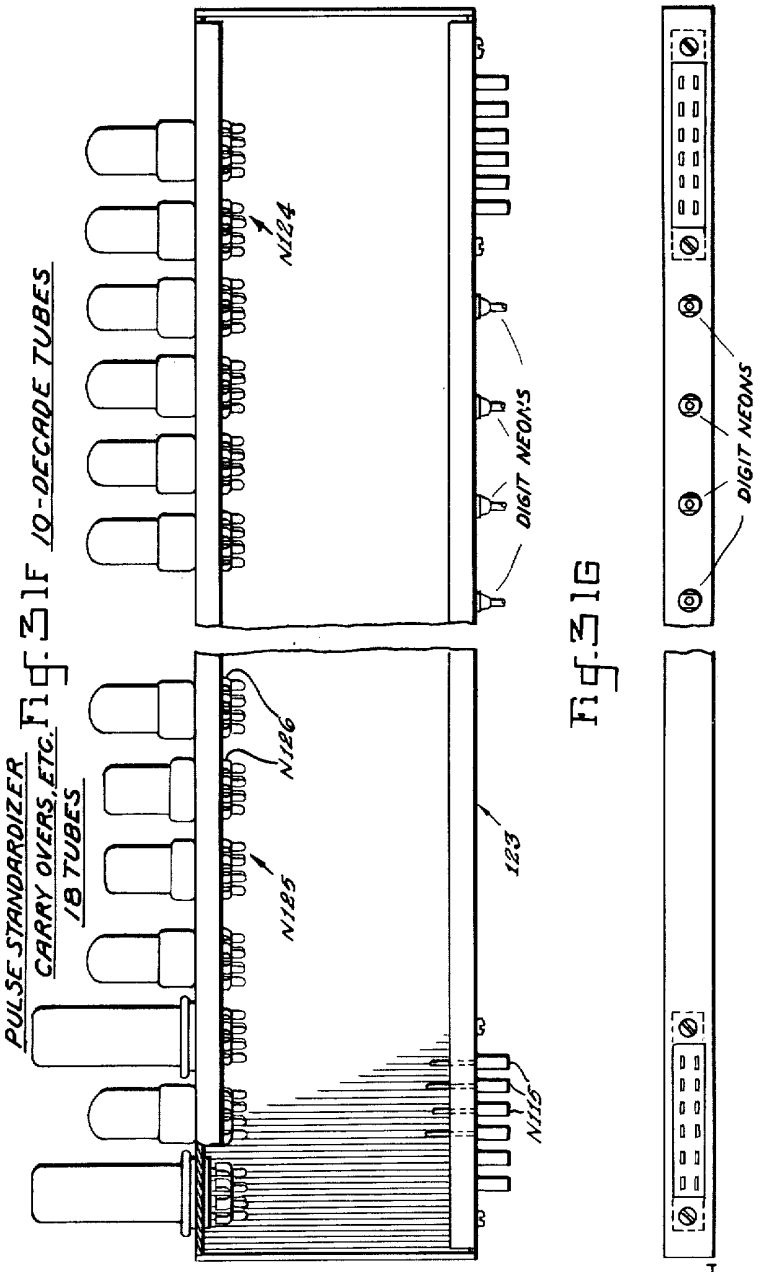

Fig. 3 1F

Fig. 3 1G

ACCUMULATOR
DECADE PLUG-IN UNIT

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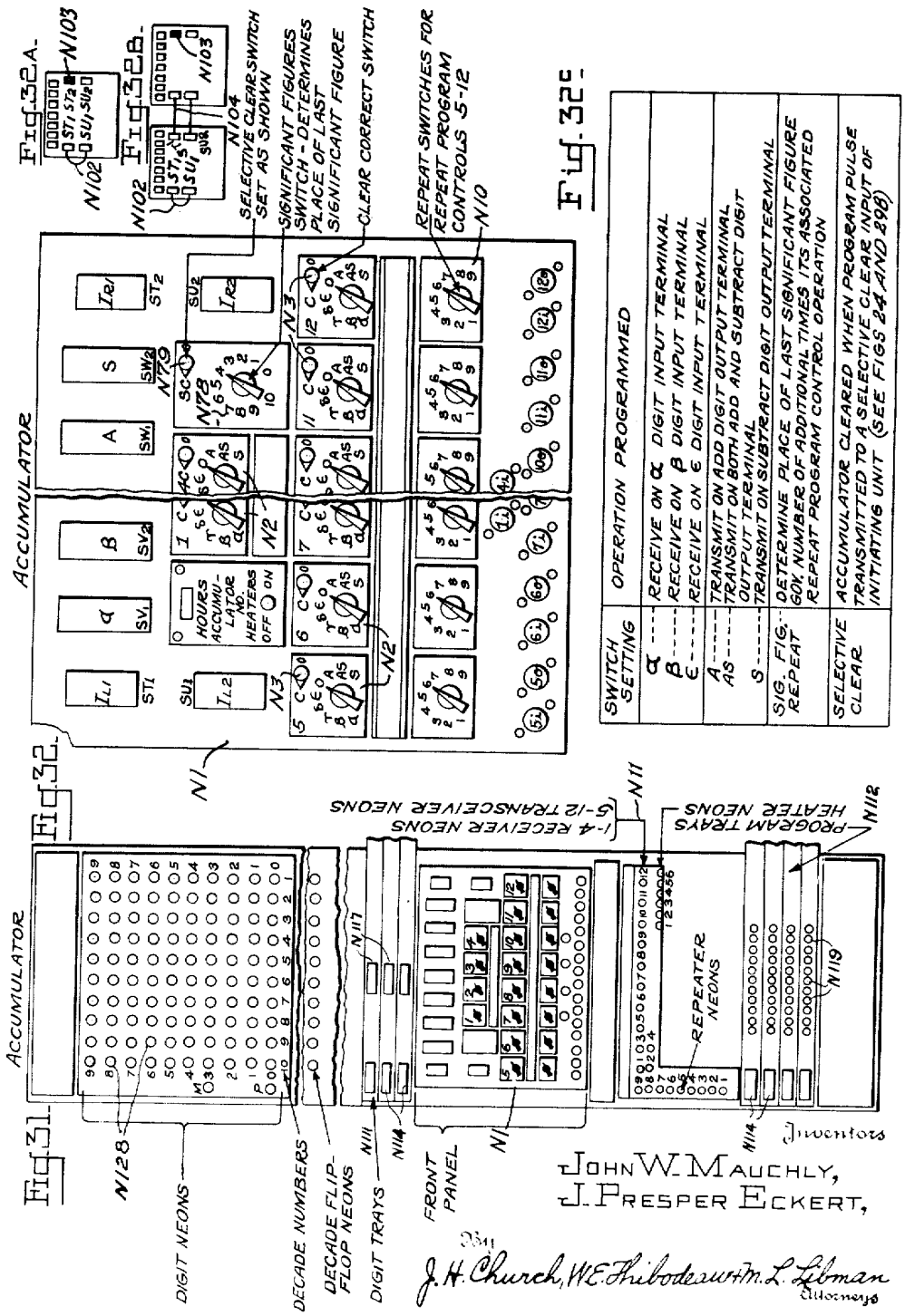

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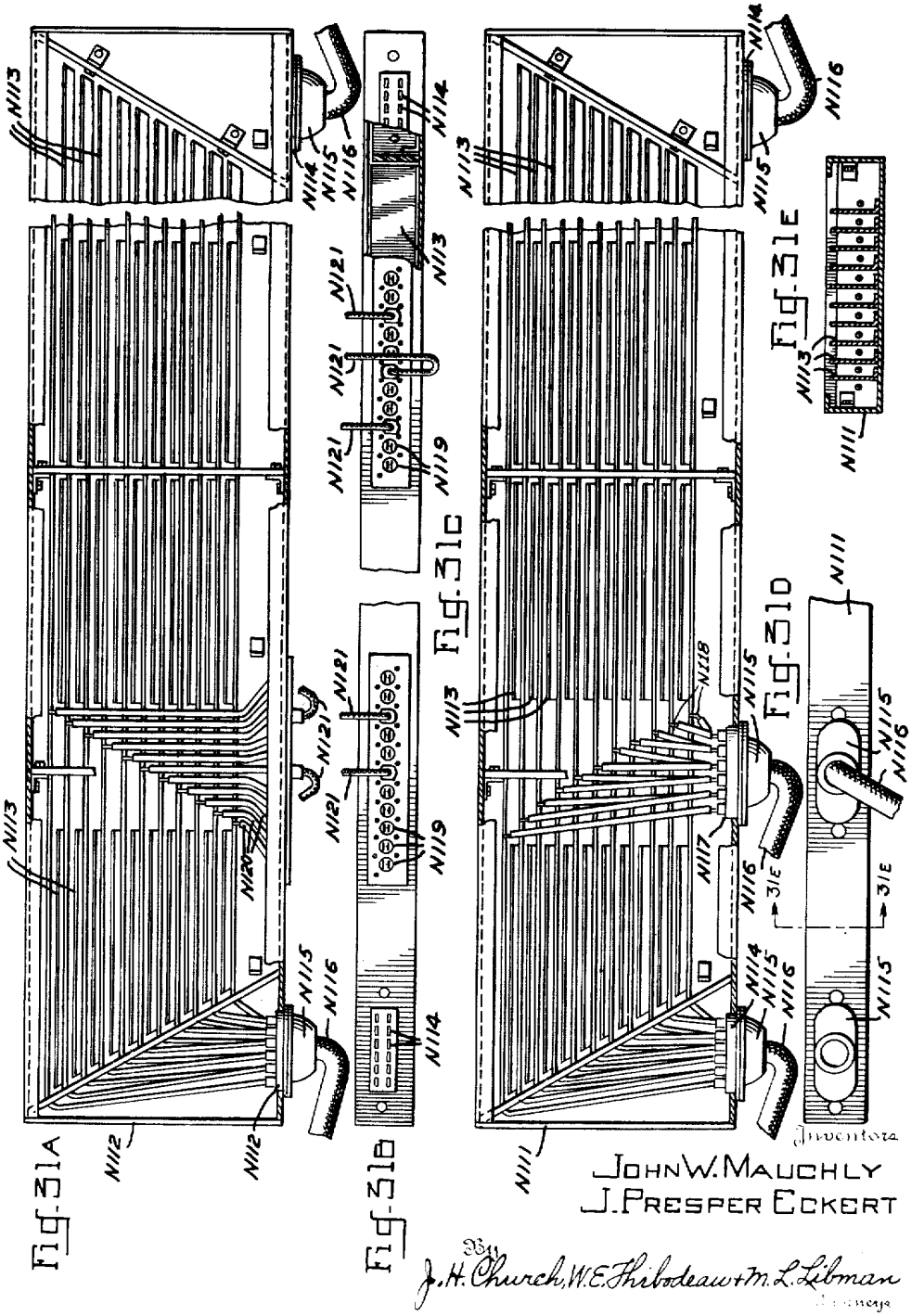

Fig. 31A

Fig. 31B

Fig. 31C

Fig. 31D

Fig. 31E

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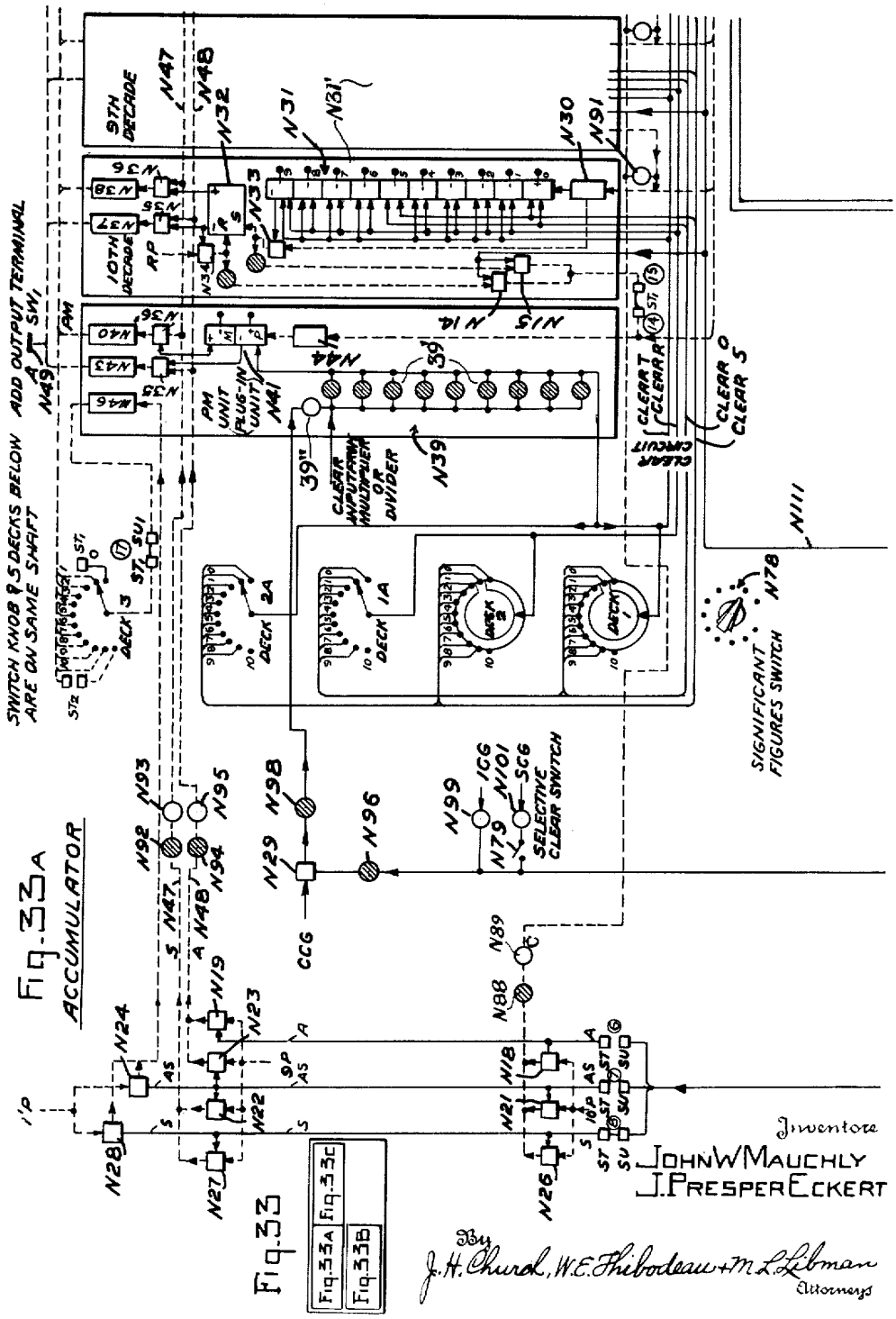

Fig. 33A

Fig. 33

Fig. 33A	Fig. 33C
Fig. 33B	

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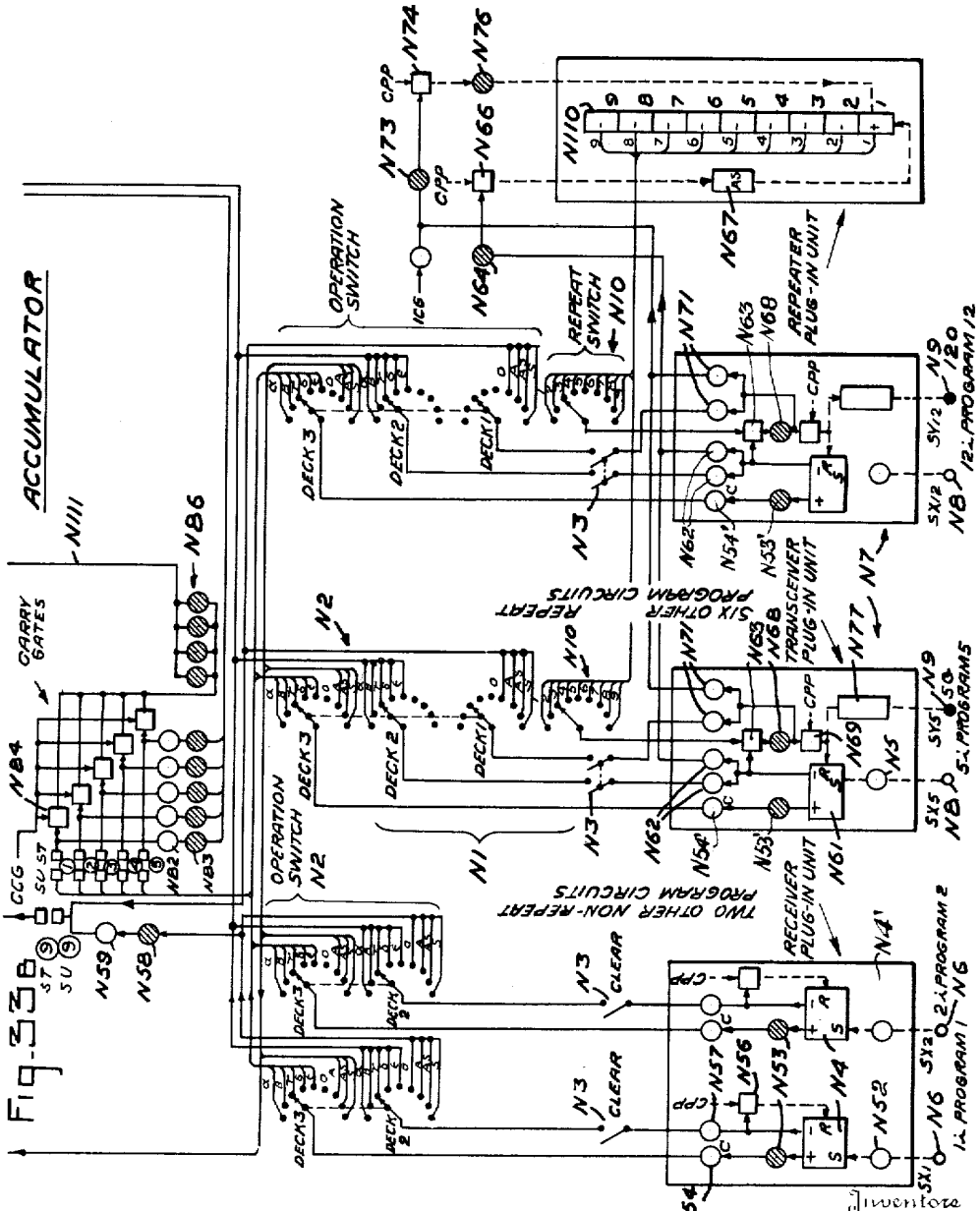

Fig. 23B

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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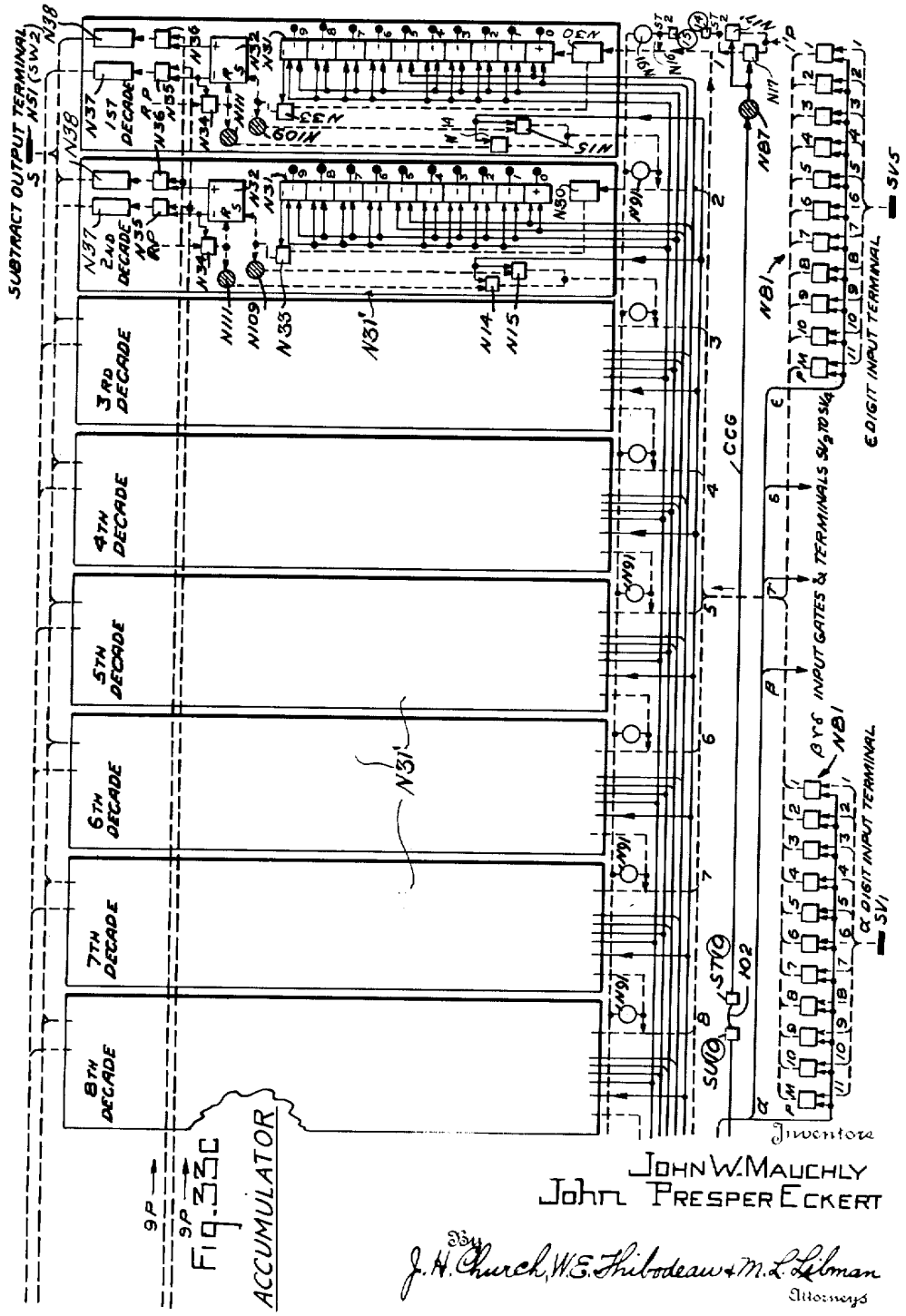

Fig. 33c

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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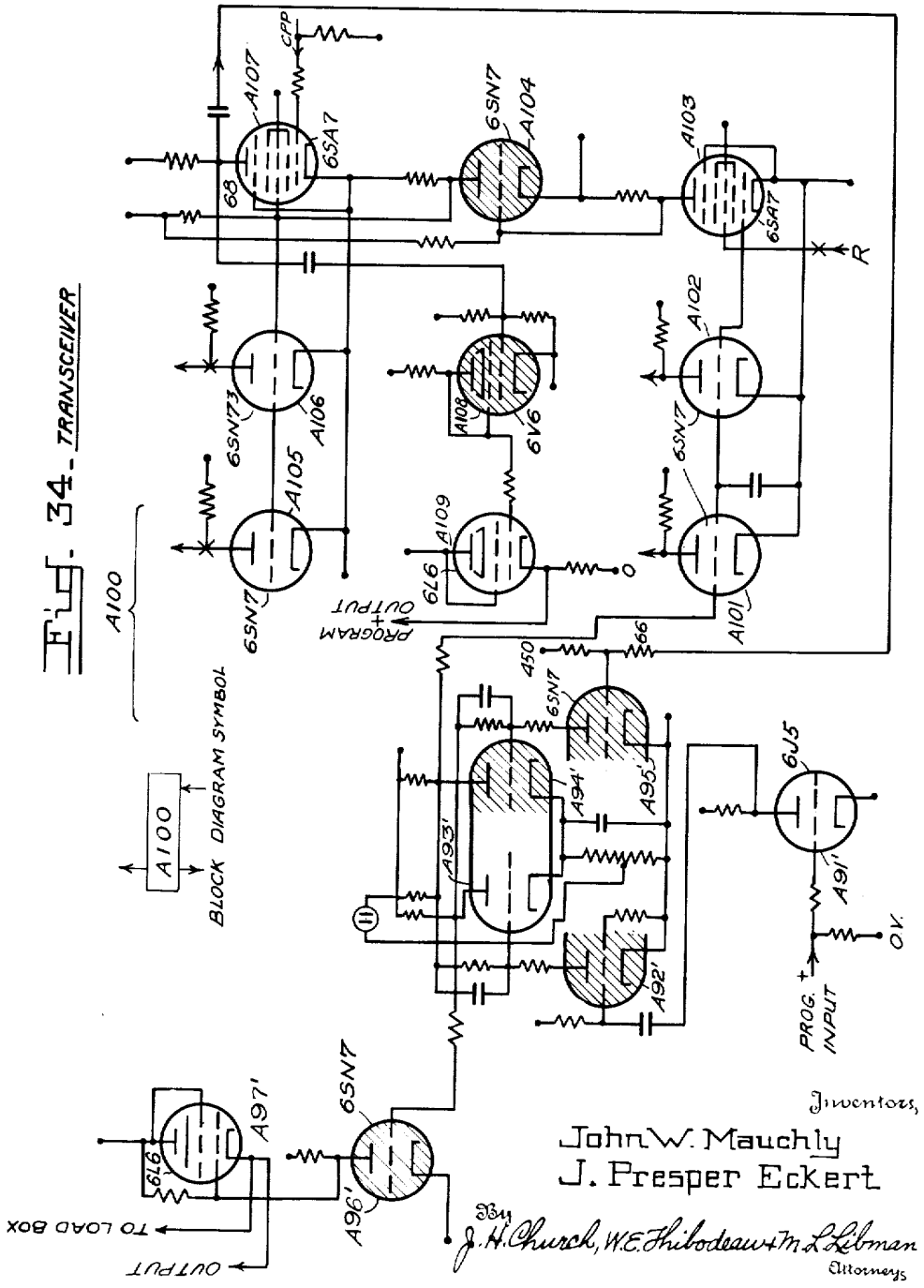

Fig. 34.- TRANSCEIVER

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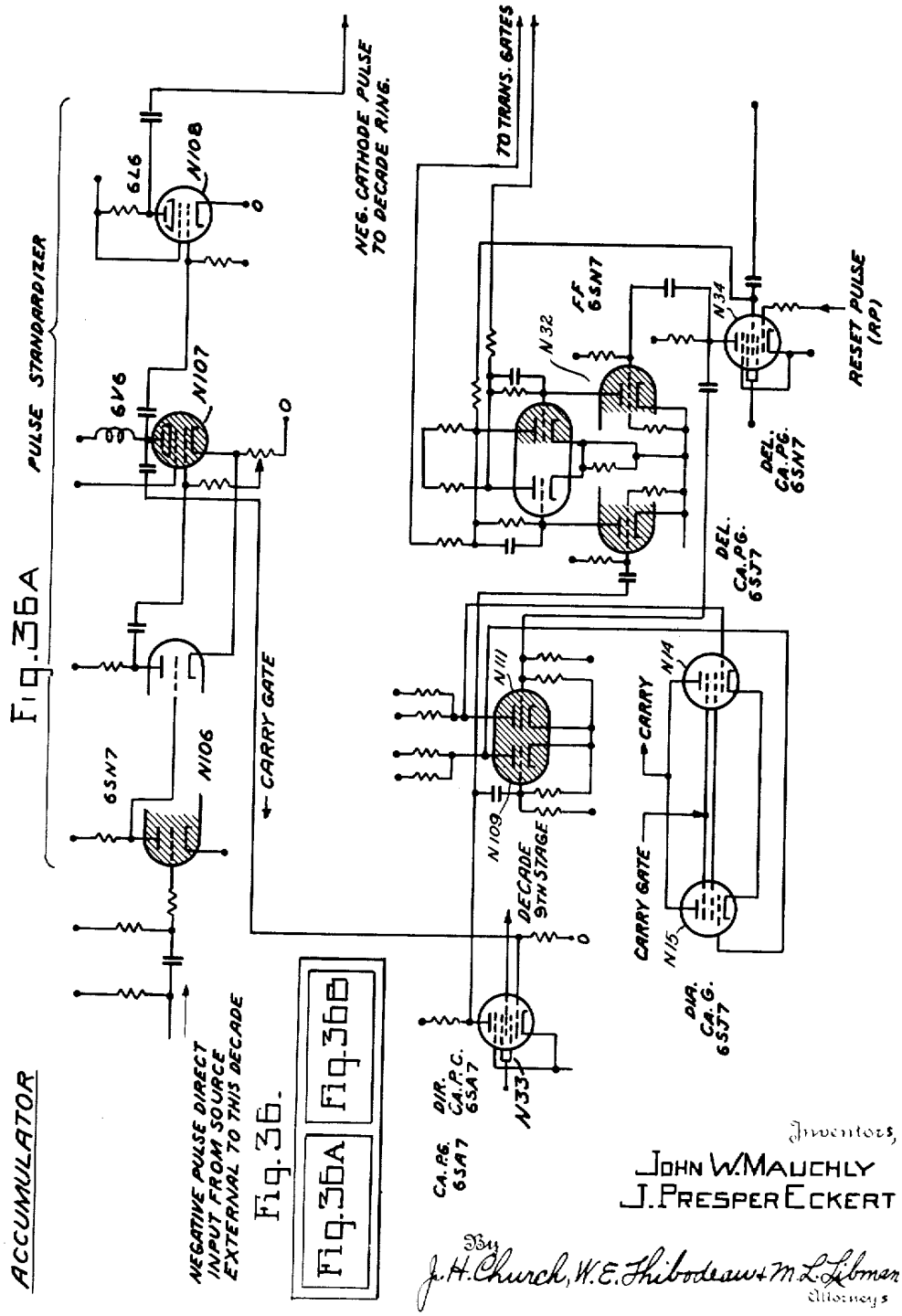

Fig. 36A

Fig. 36B

Fig. 36.

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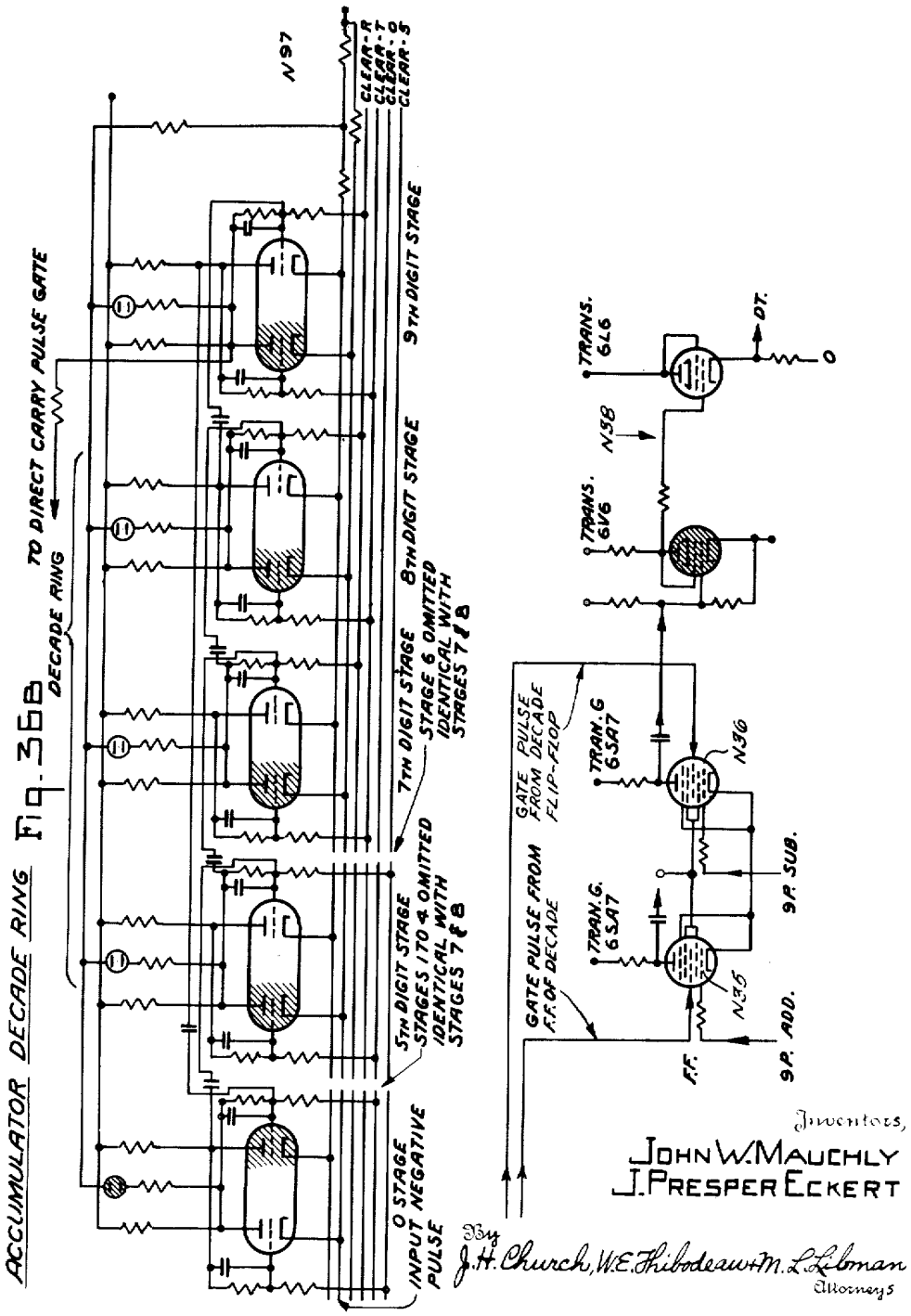

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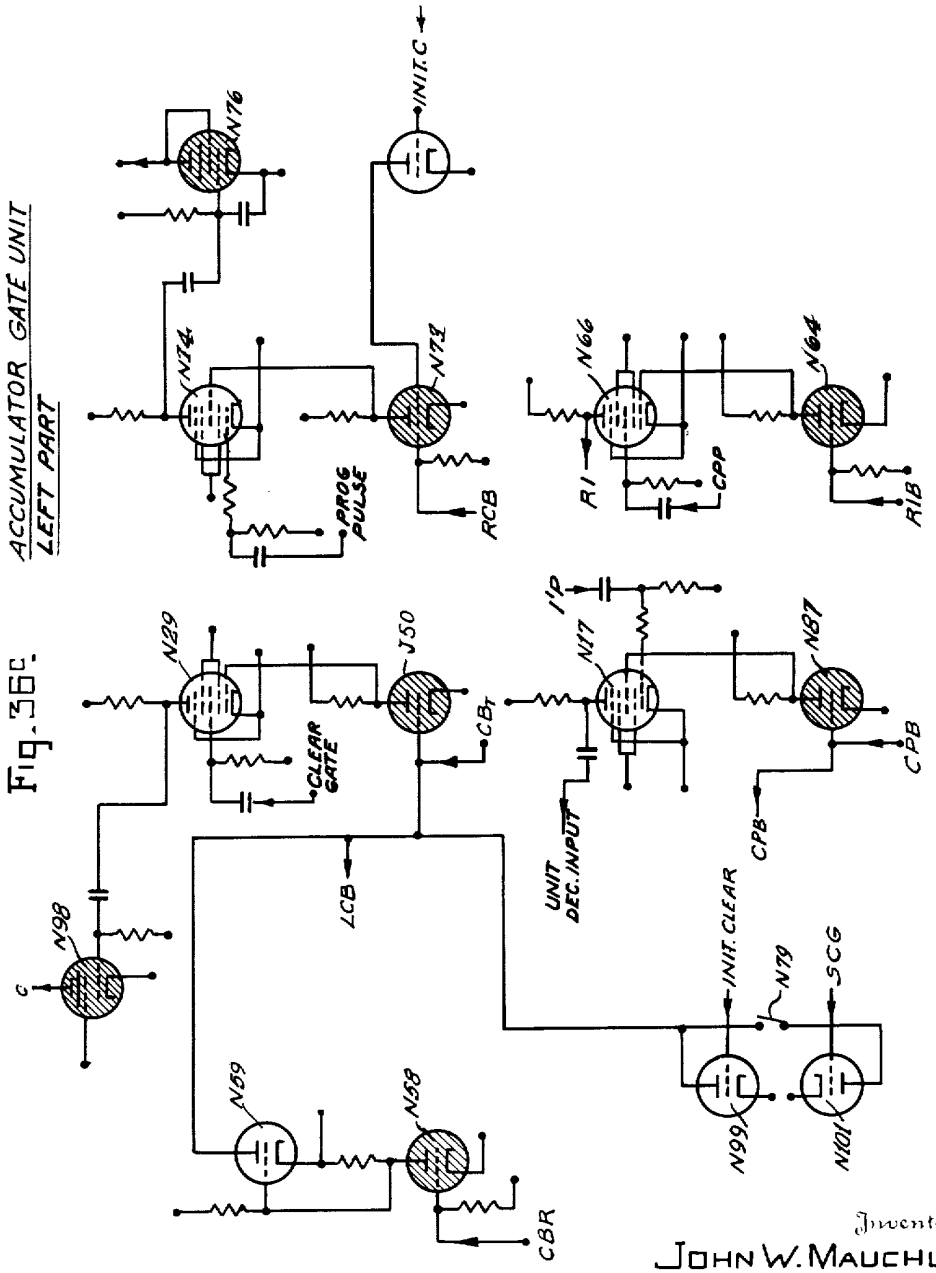

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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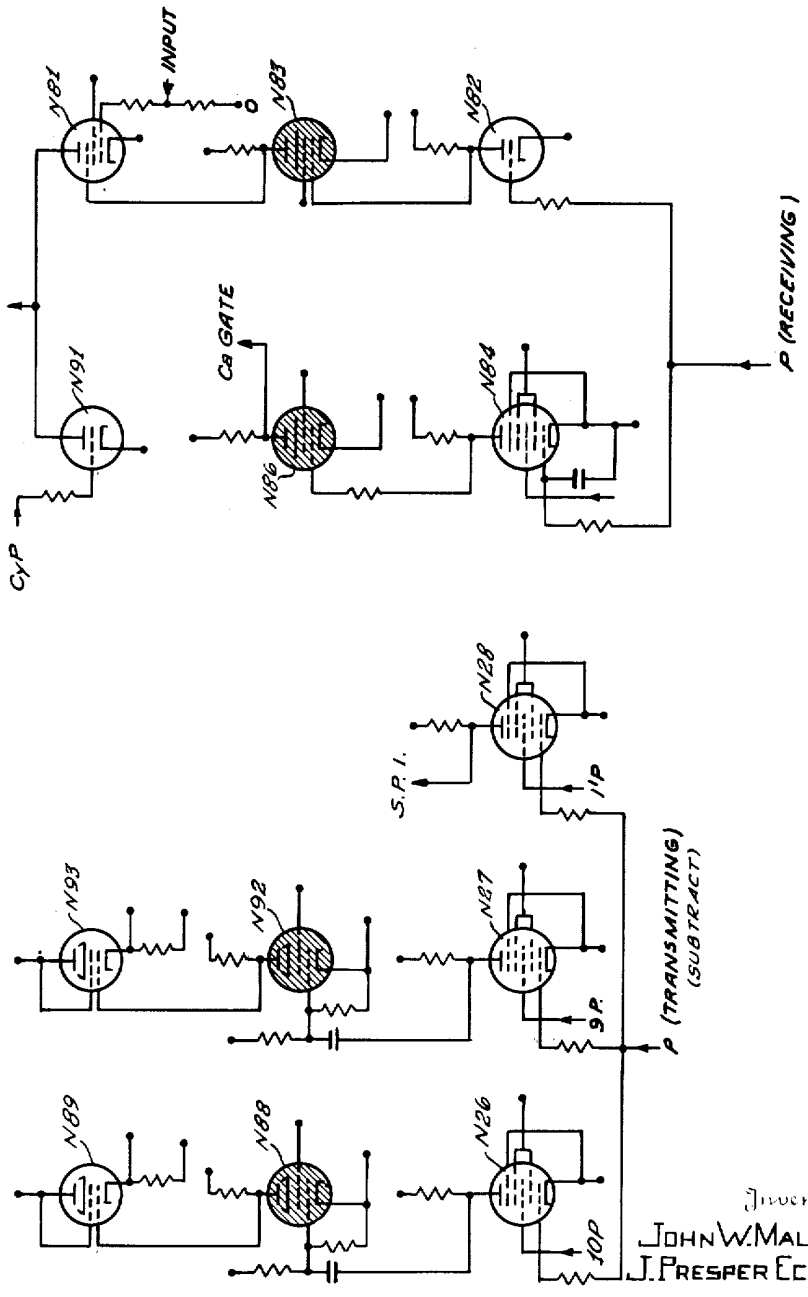
Fig. 36D. ACCUMULATOR GATE UNIT RIGHT PART



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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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Fig. 36E ACCUMULATOR REPEATER

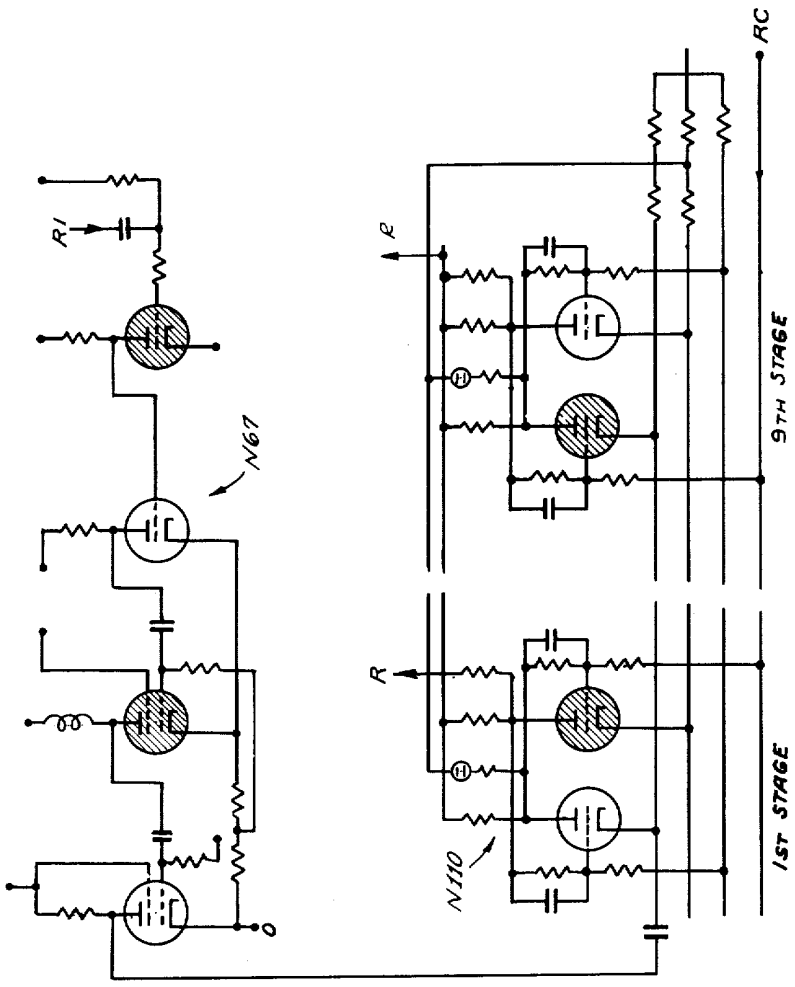

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Fig. 37.

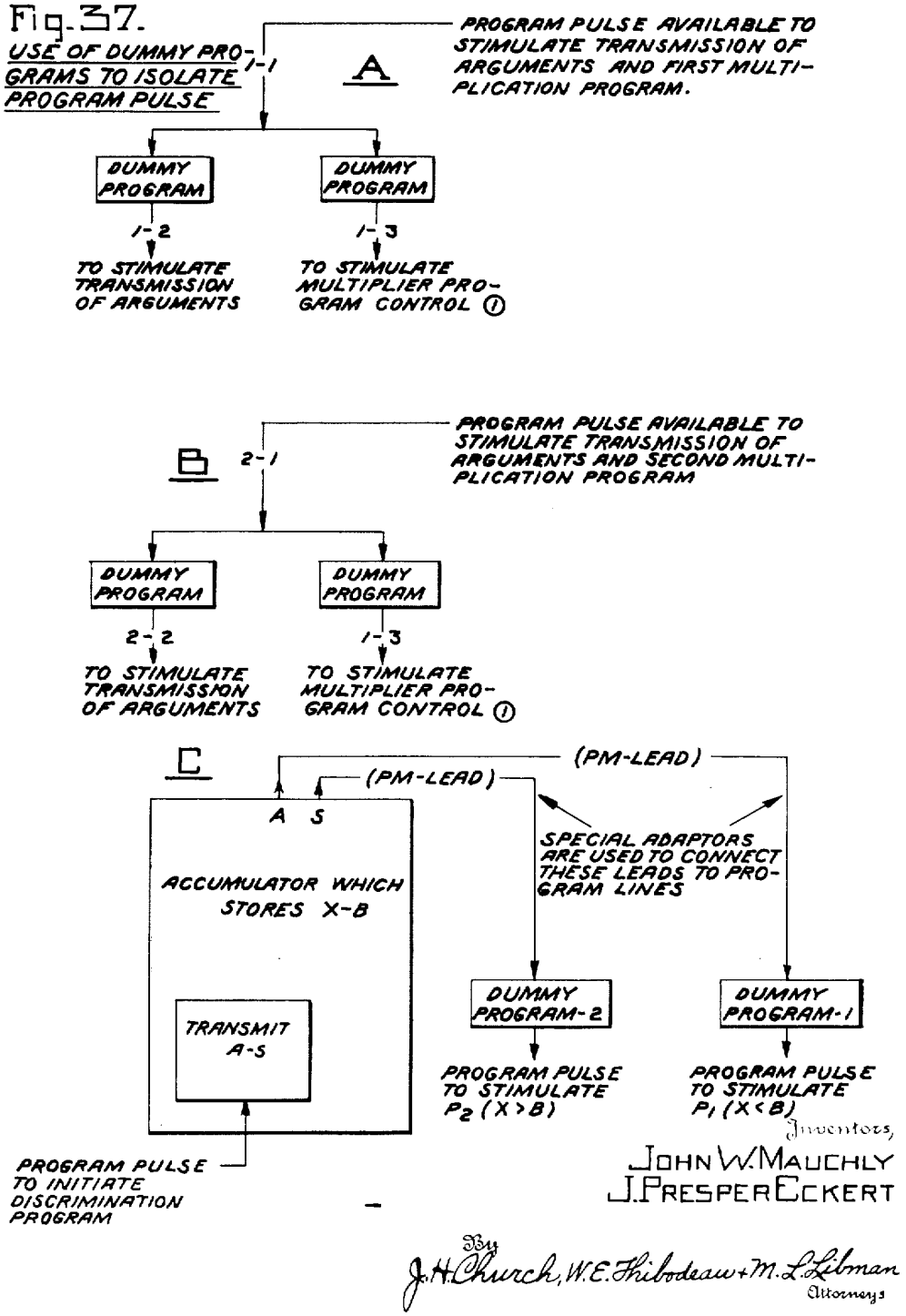

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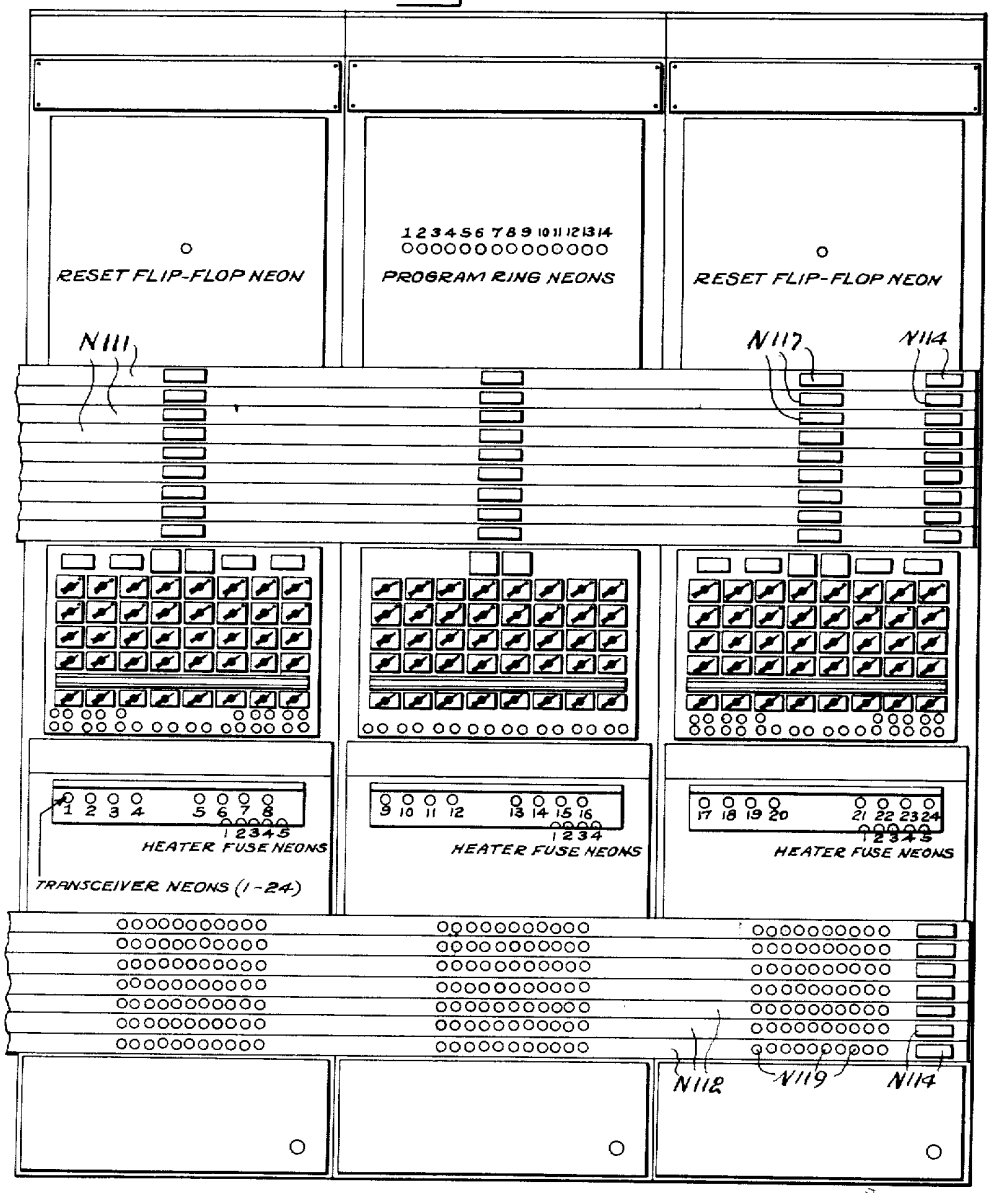
Fig. 38.



HIGH SPEED MULTIPLIER

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Fig. 39

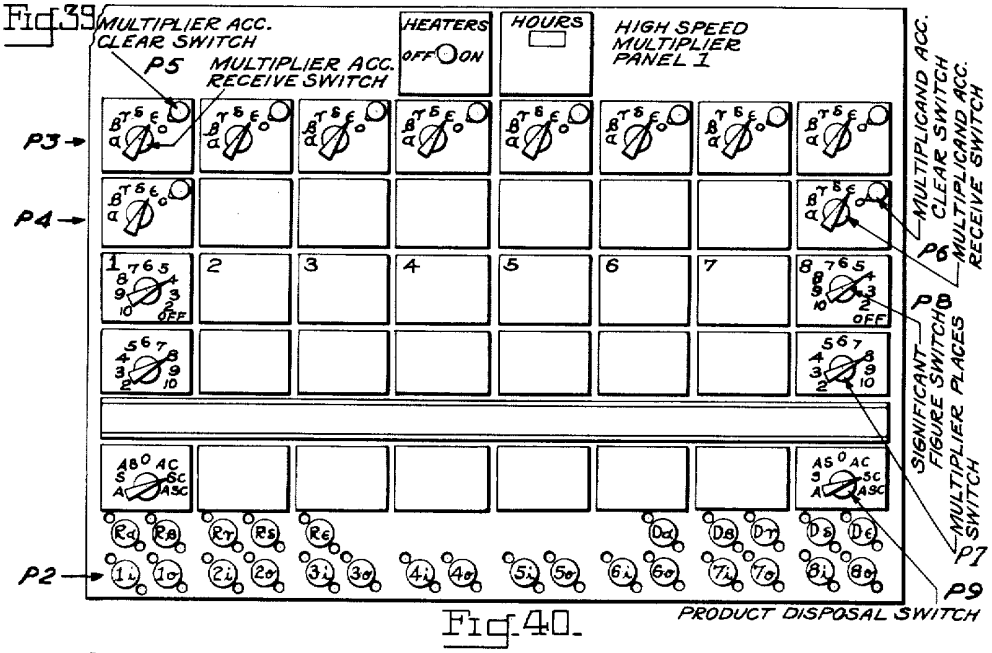
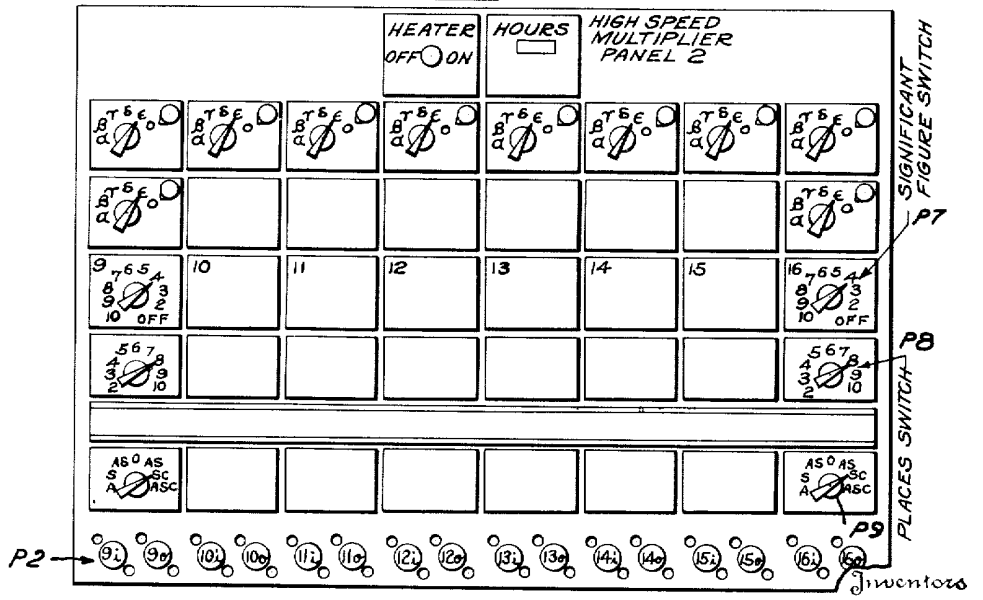


Fig. 40.



HIGH SPEED MULTIPLIER

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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Fig. 41.

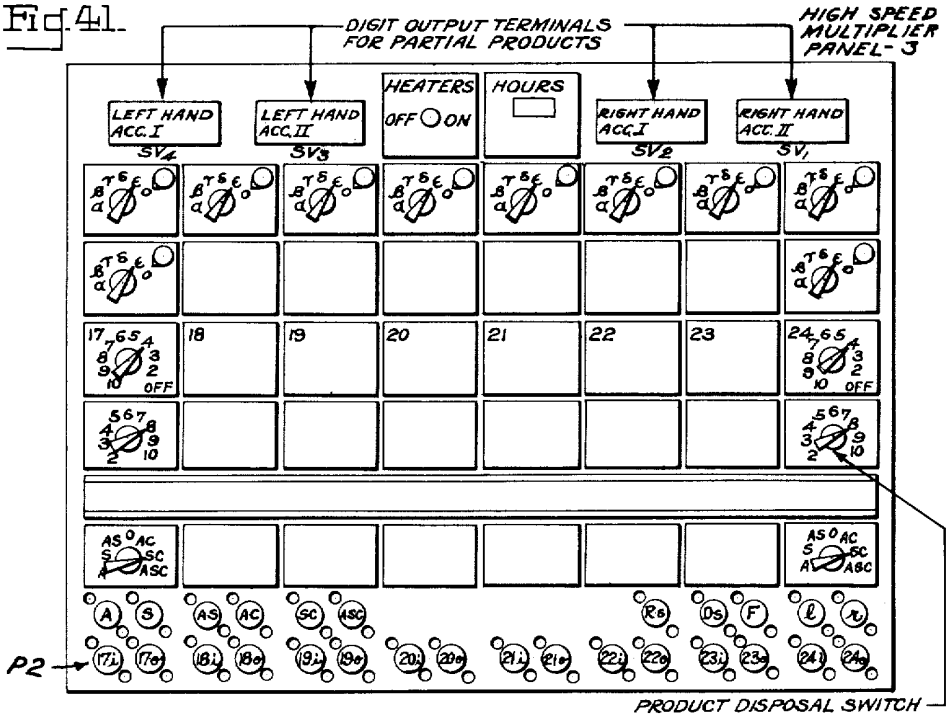


Fig. 43A.

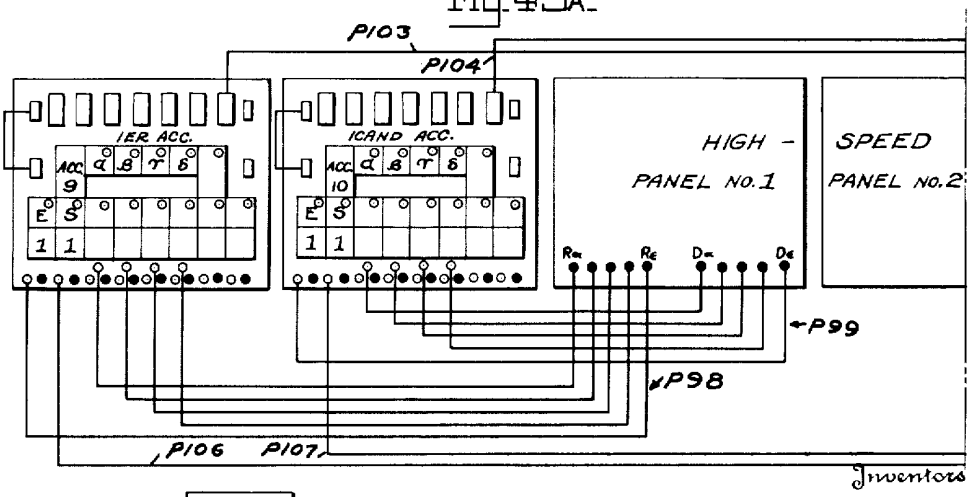
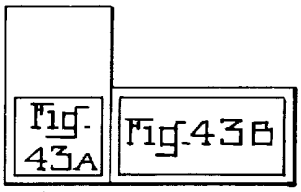


Fig. 43



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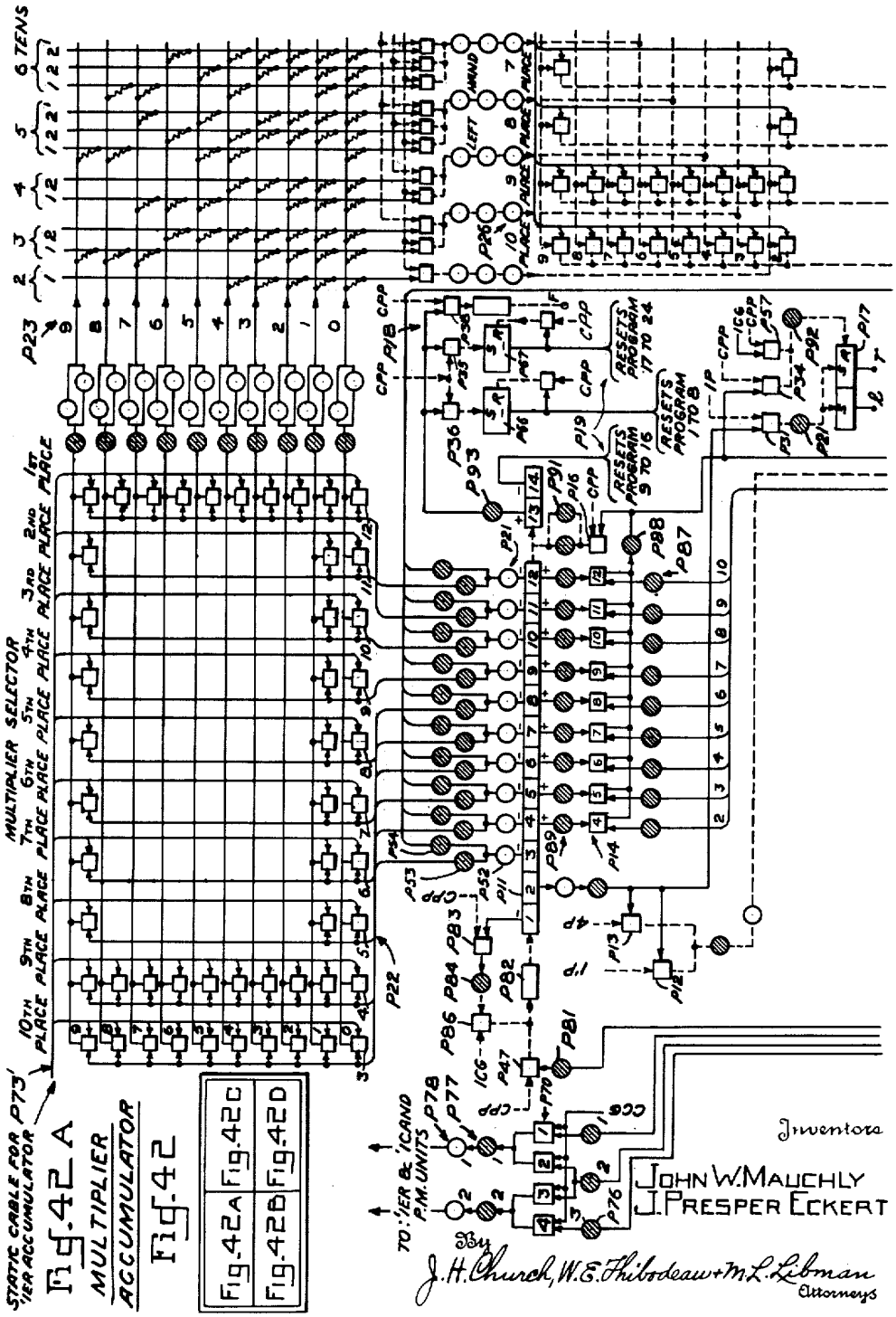

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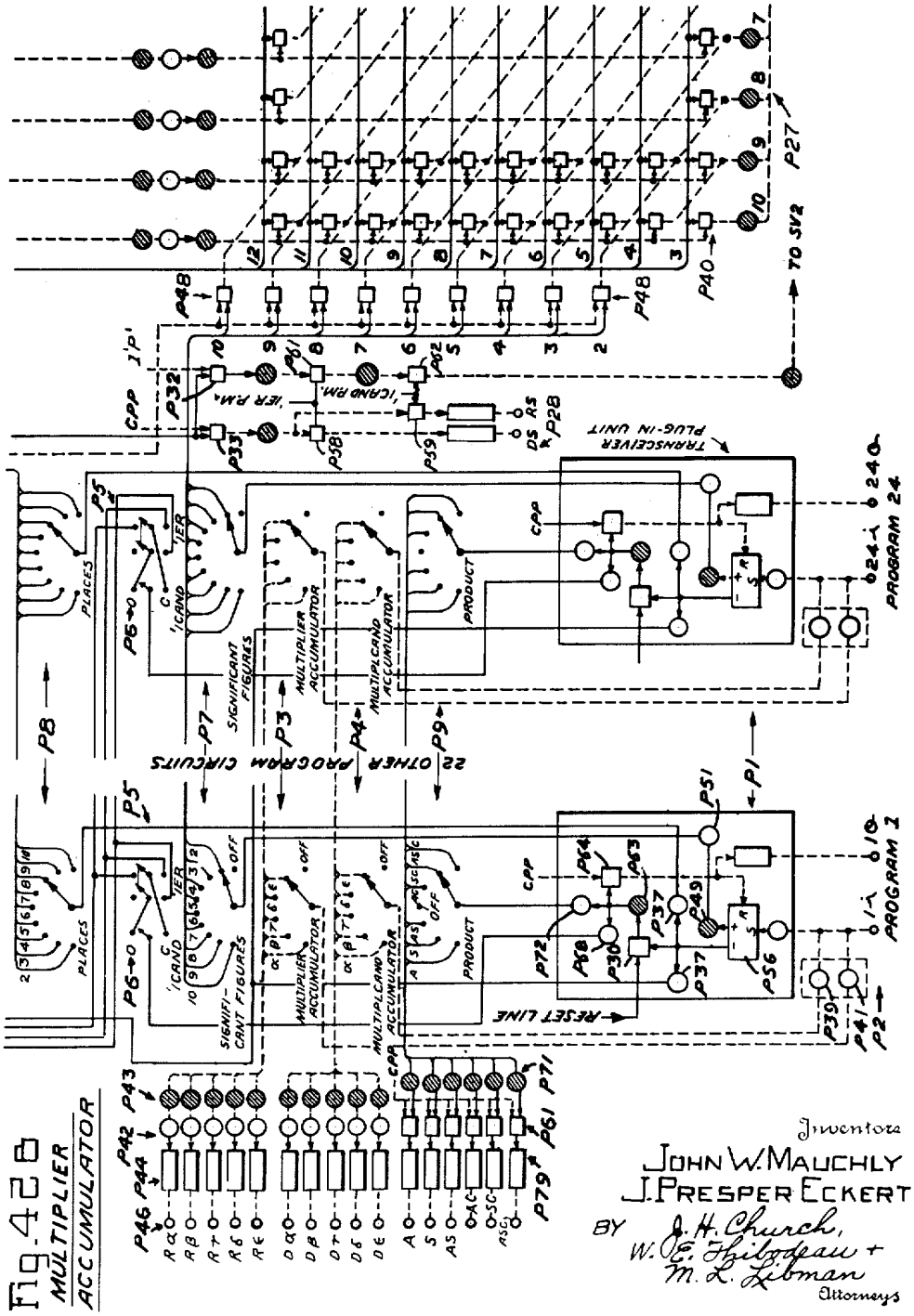

Fig. 42B
MULTIPLIER ACCUMULATOR

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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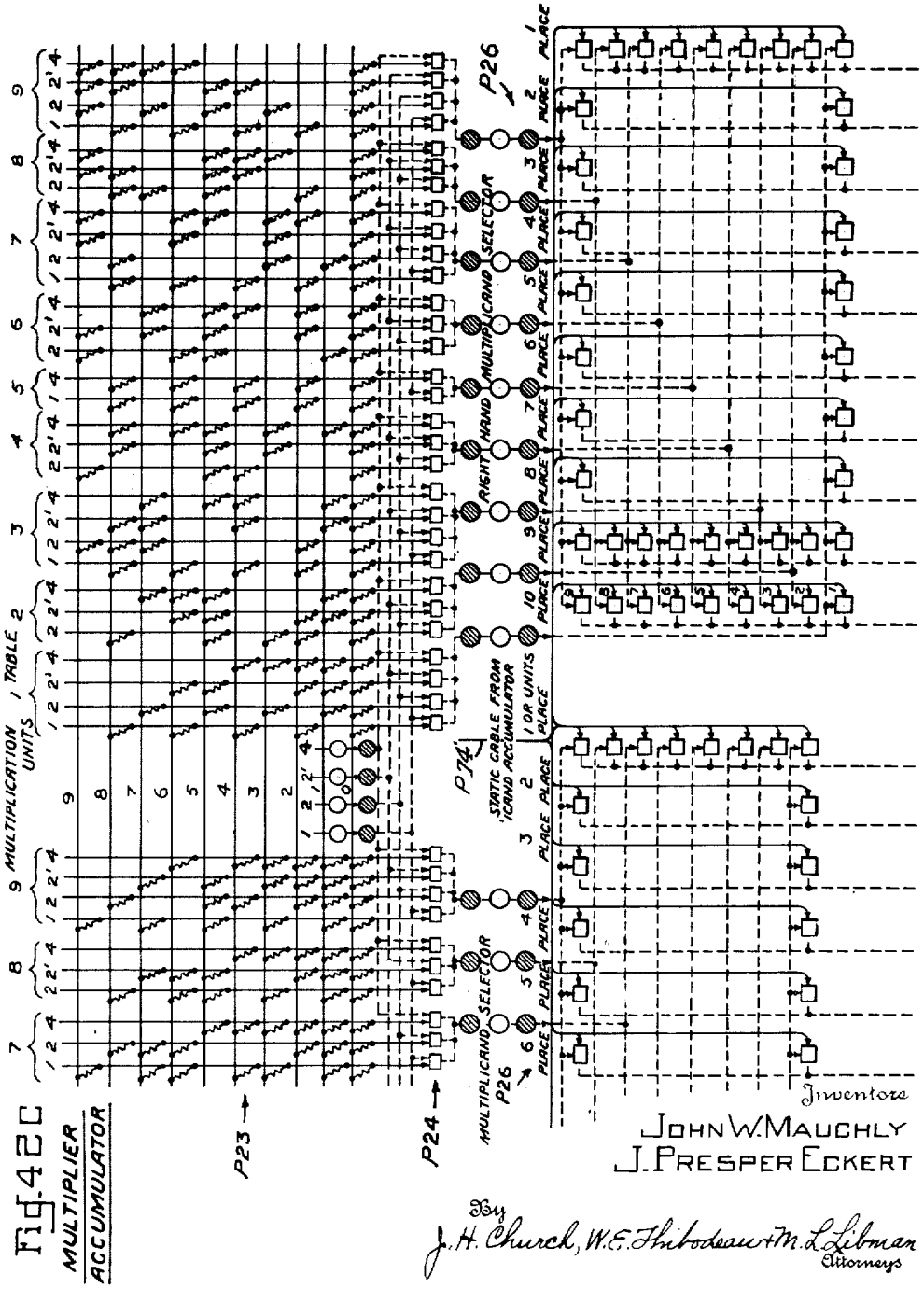

Fig. 42C

MULTIPLIER ACCUMULATOR

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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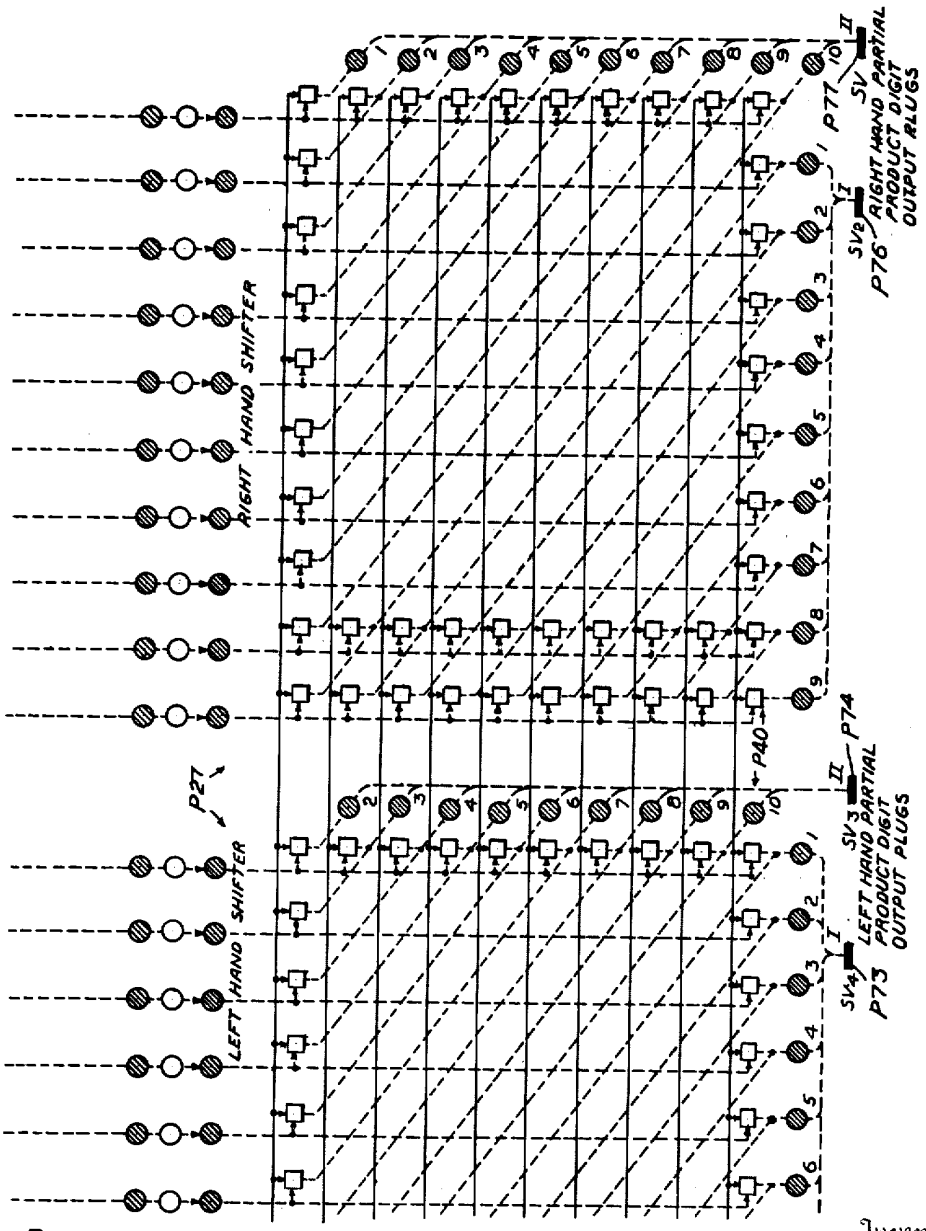

Fig. 42D
MULTIPLIER ACCUMULATOR

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

Filed June 26, 1947 91 Sheets-Sheet 44

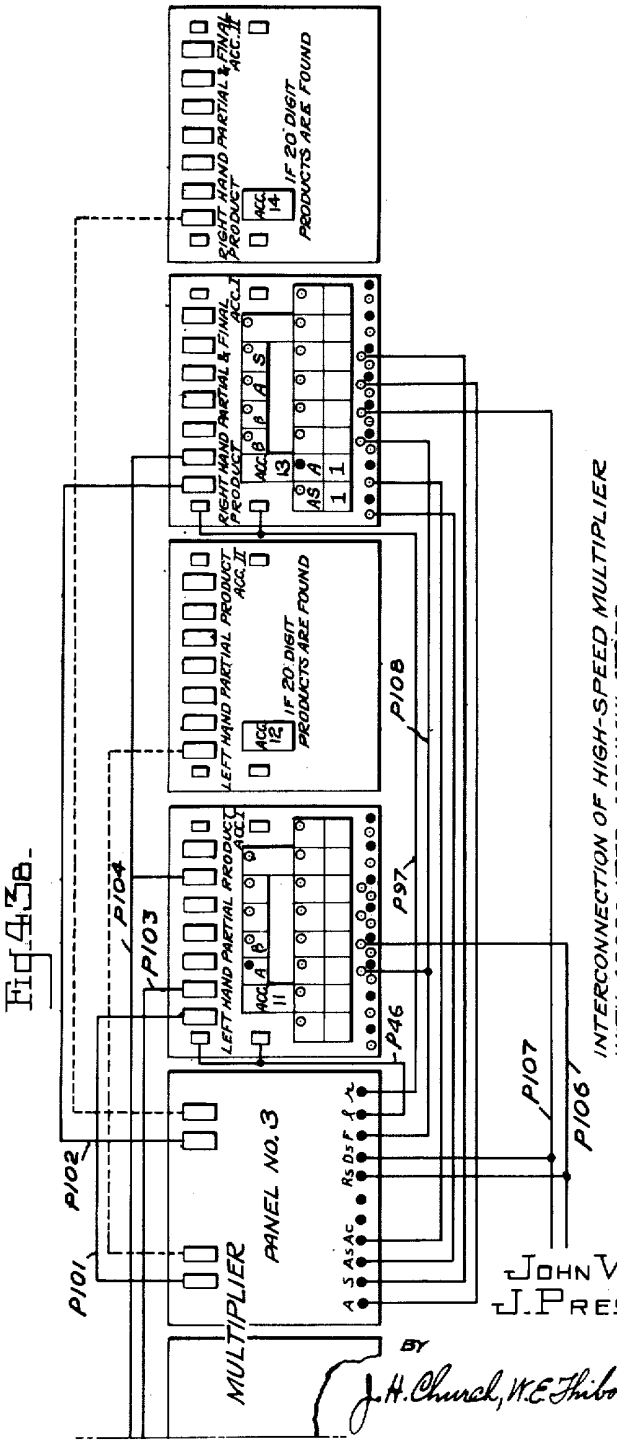

Fig. 43b.

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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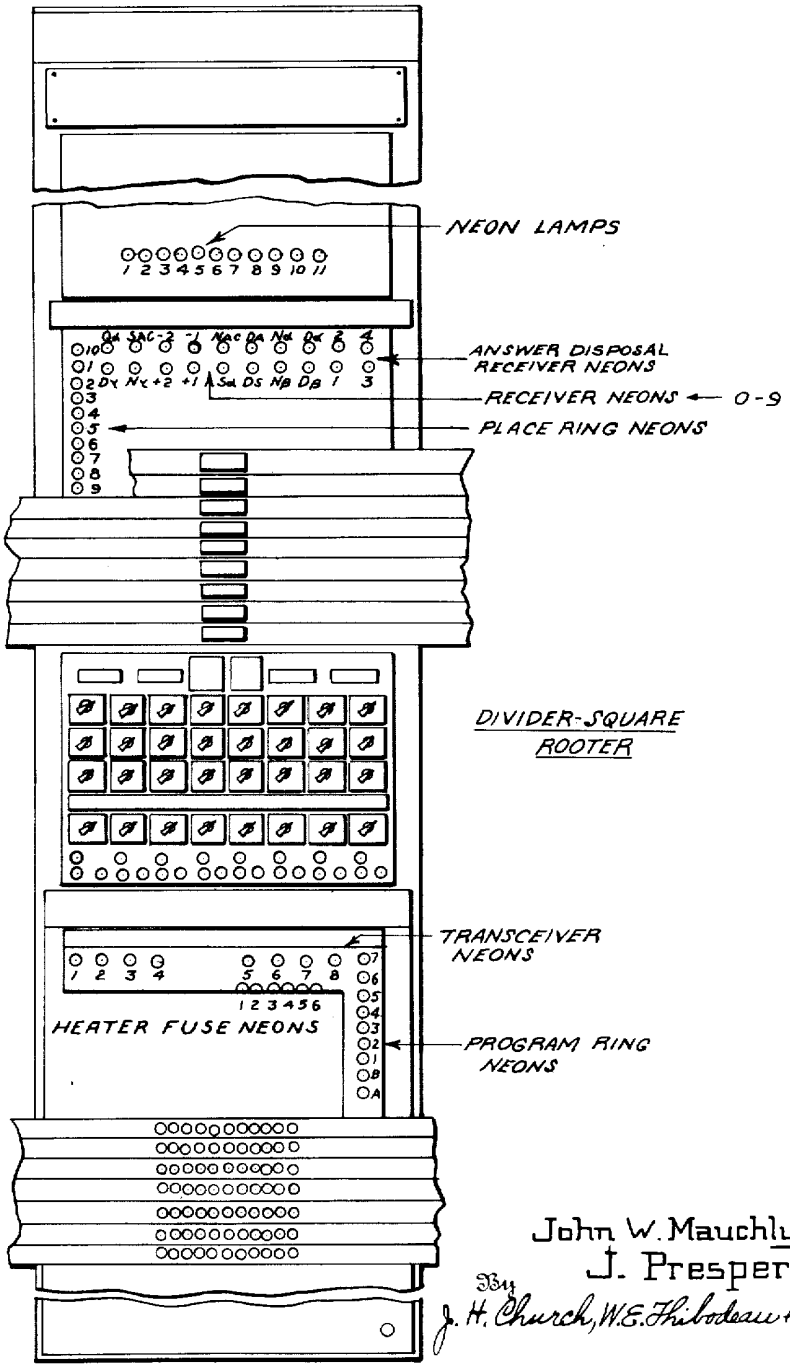
Fig. 44.



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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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Fig. 45

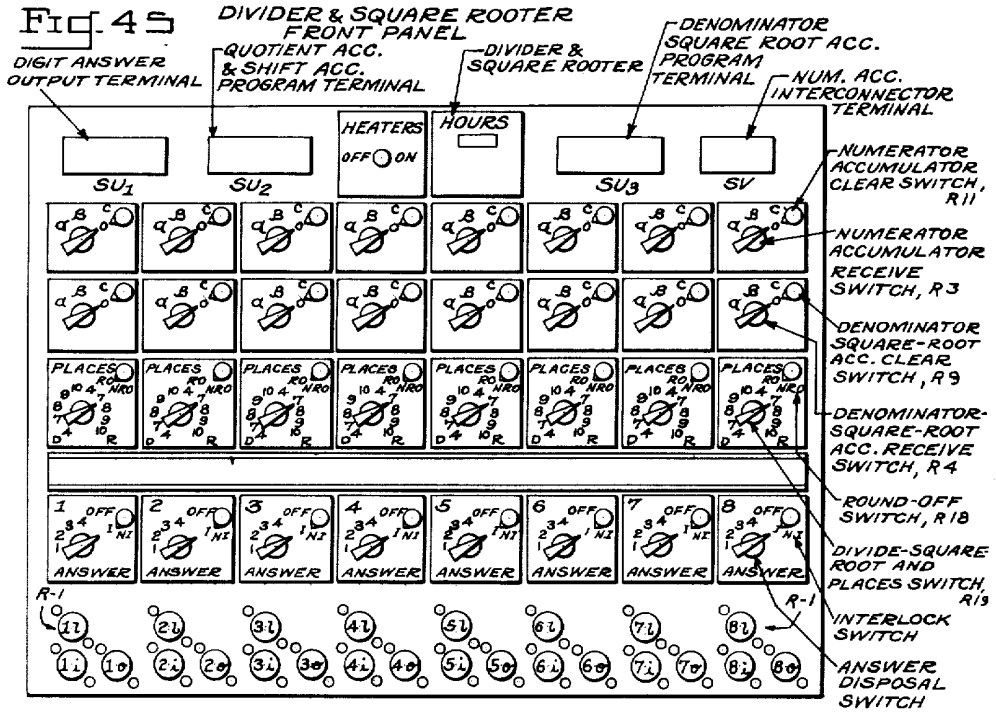

Fig. 47A

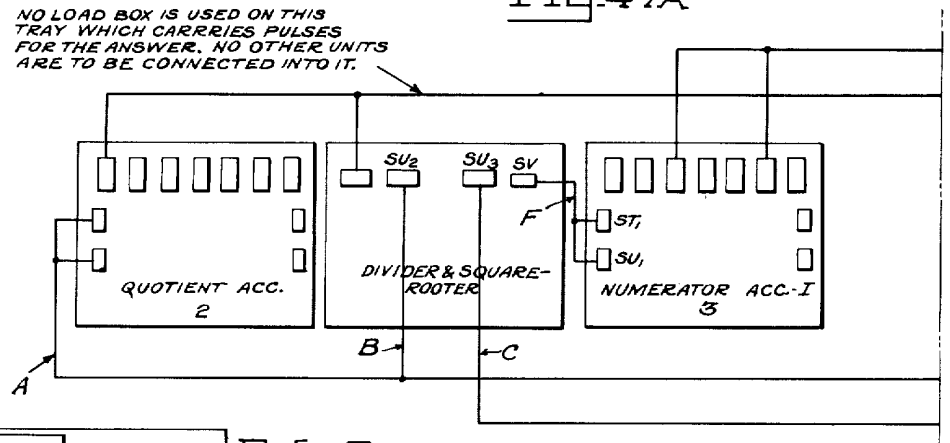

Fig. 47

Fig. 47A | Fig. 47B

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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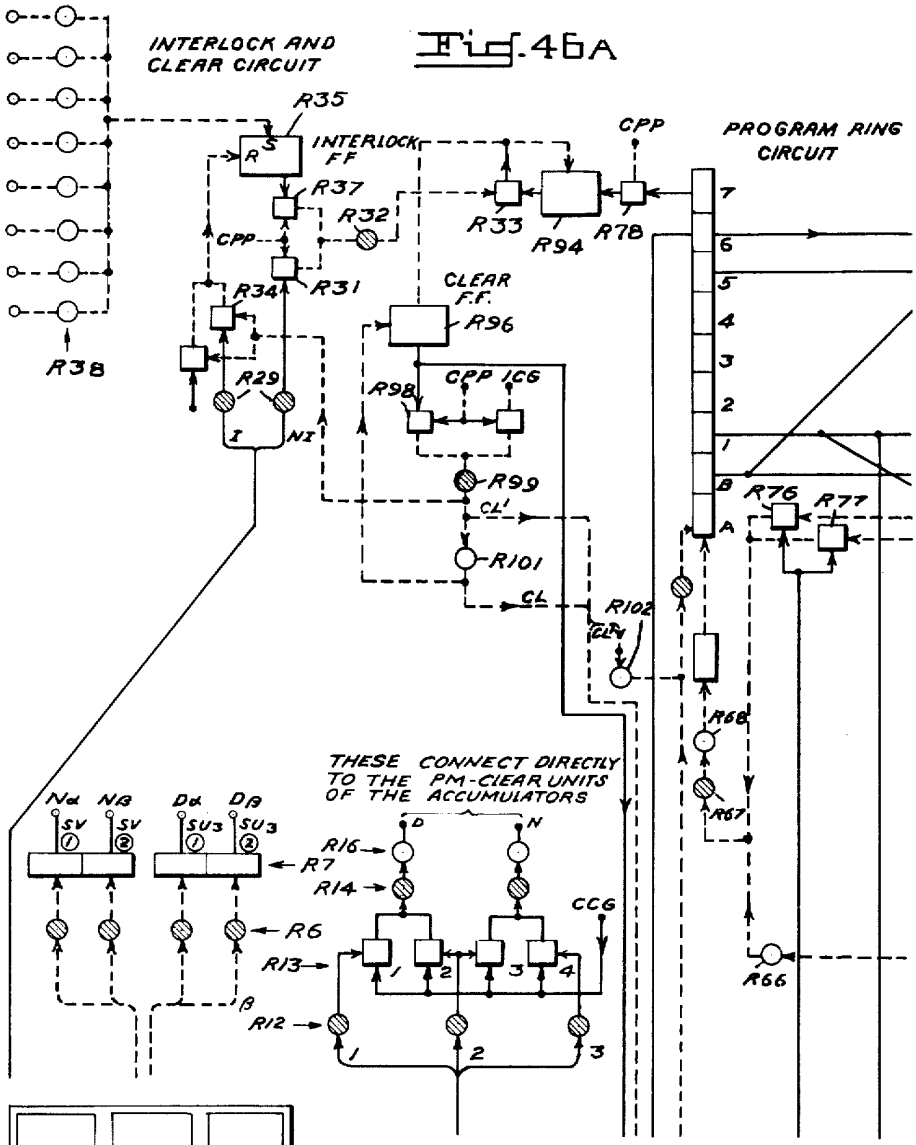
Fig. 46A



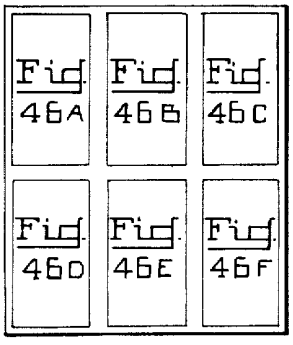


Fig. 46

Inventors
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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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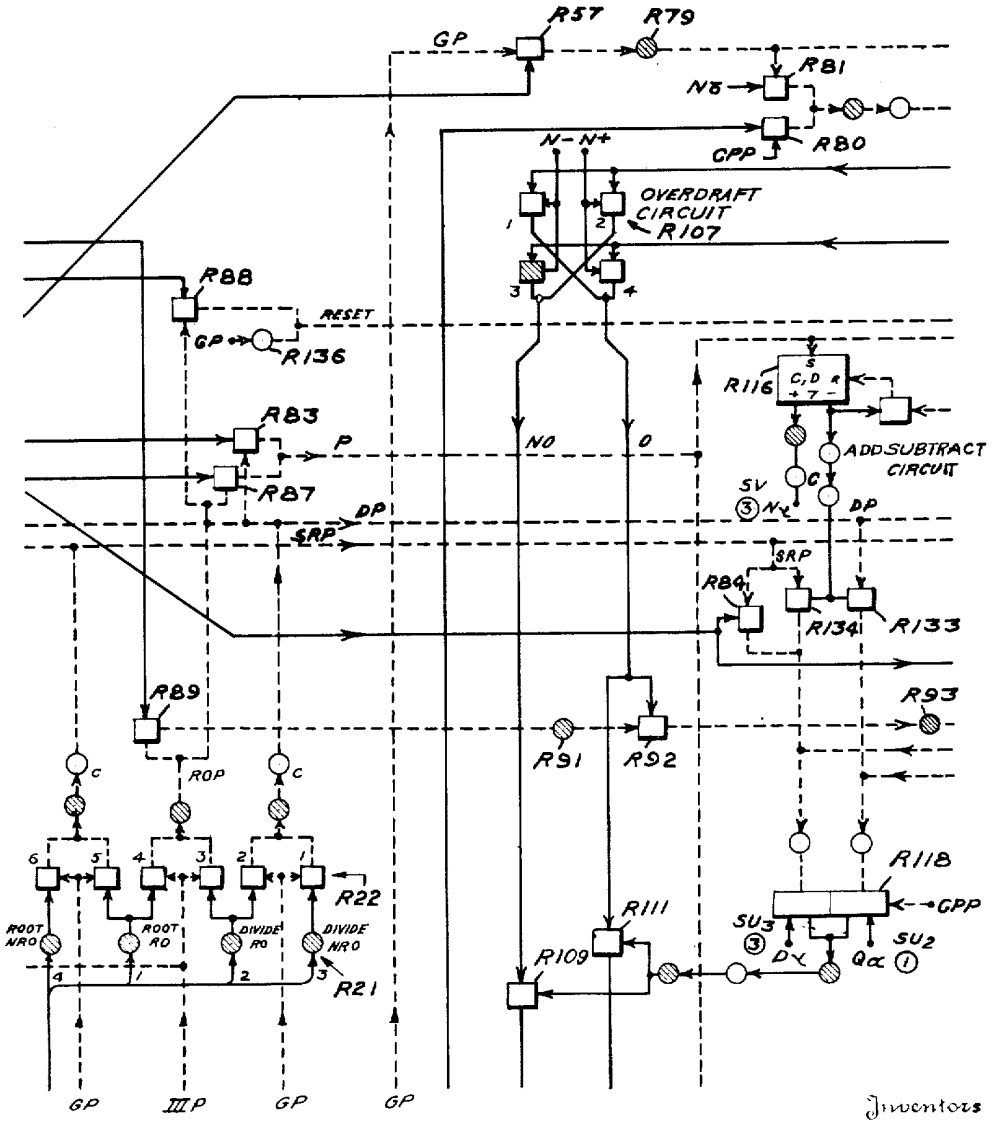
Fig. 46B



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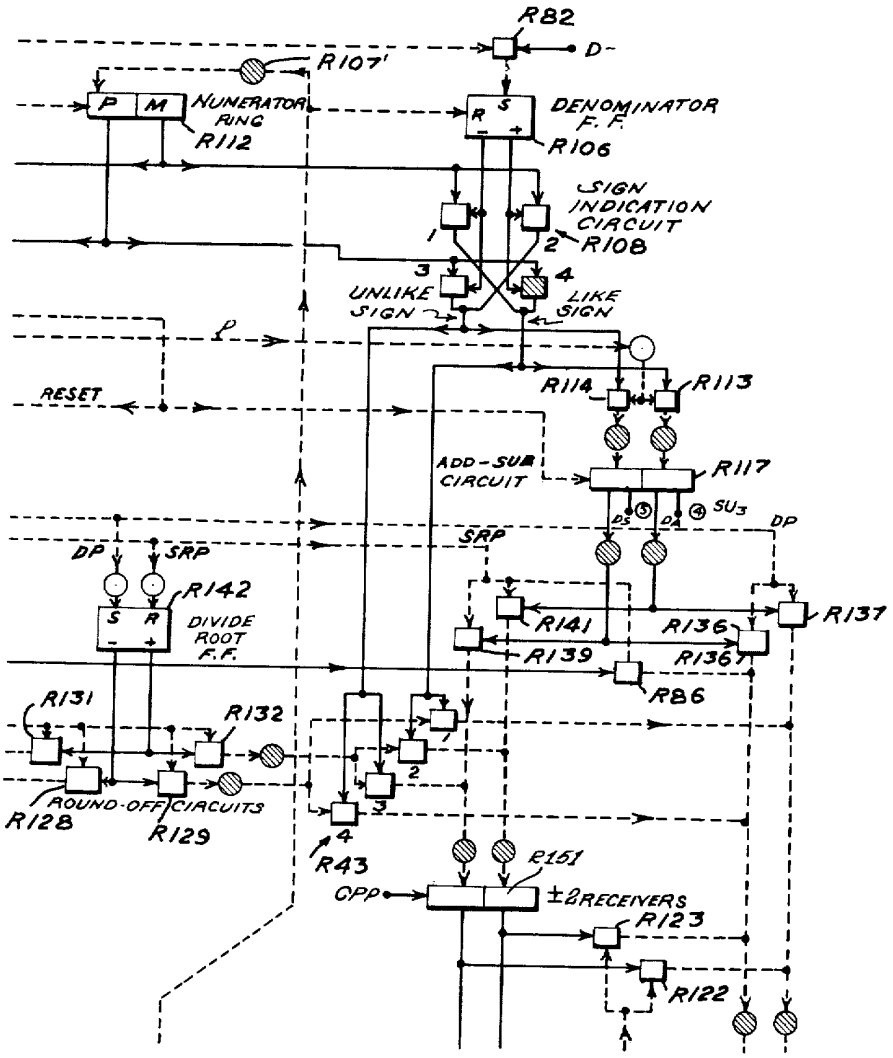
ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

Filed June 26, 1947 91 Sheets-Sheet 49

Fig. 46 C



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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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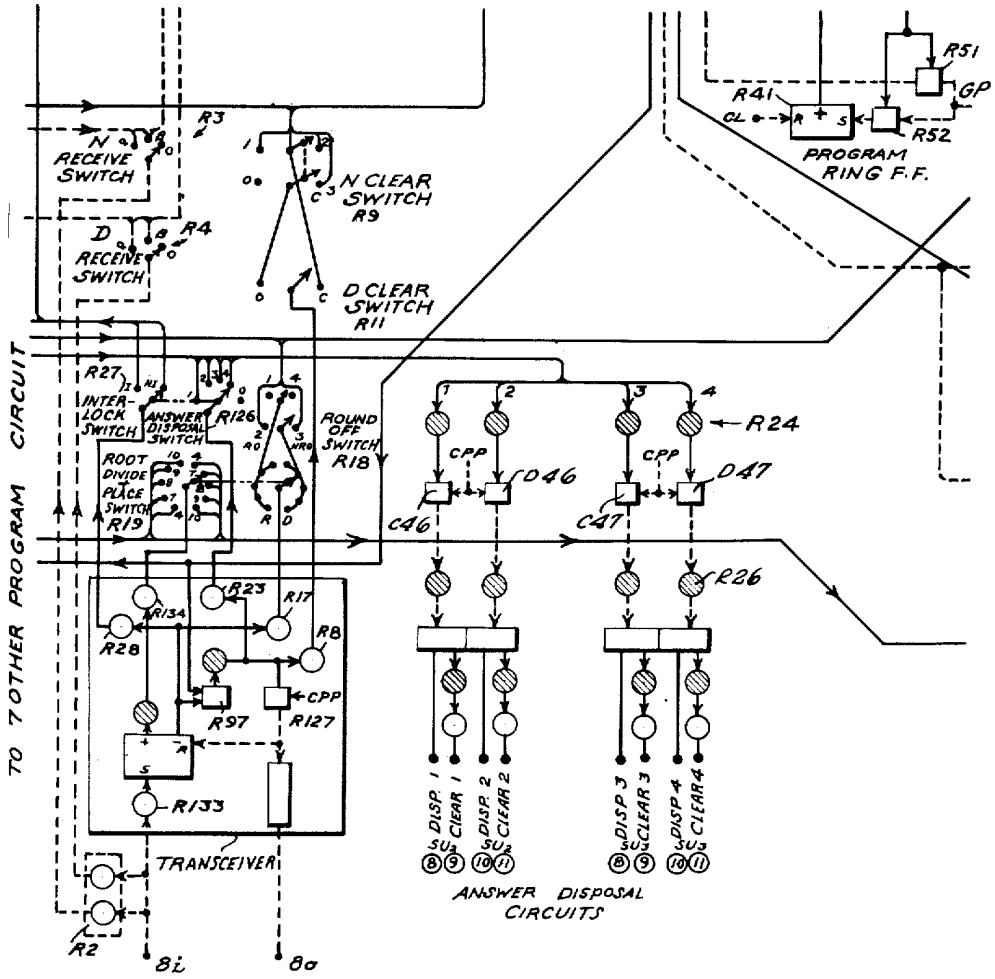
Fig. 46D



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Feb. 4, 1964 J. P. ECKERT, JR., ETAL 3,120,606

ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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Fig. 46E

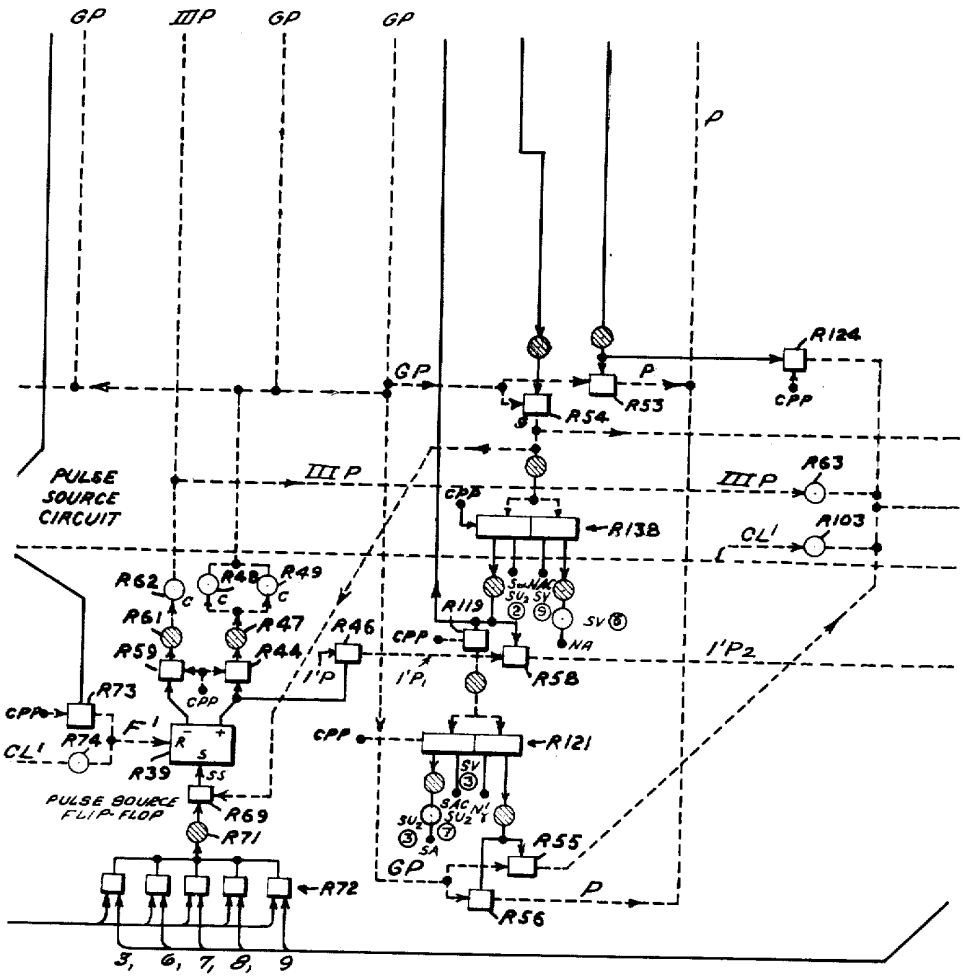

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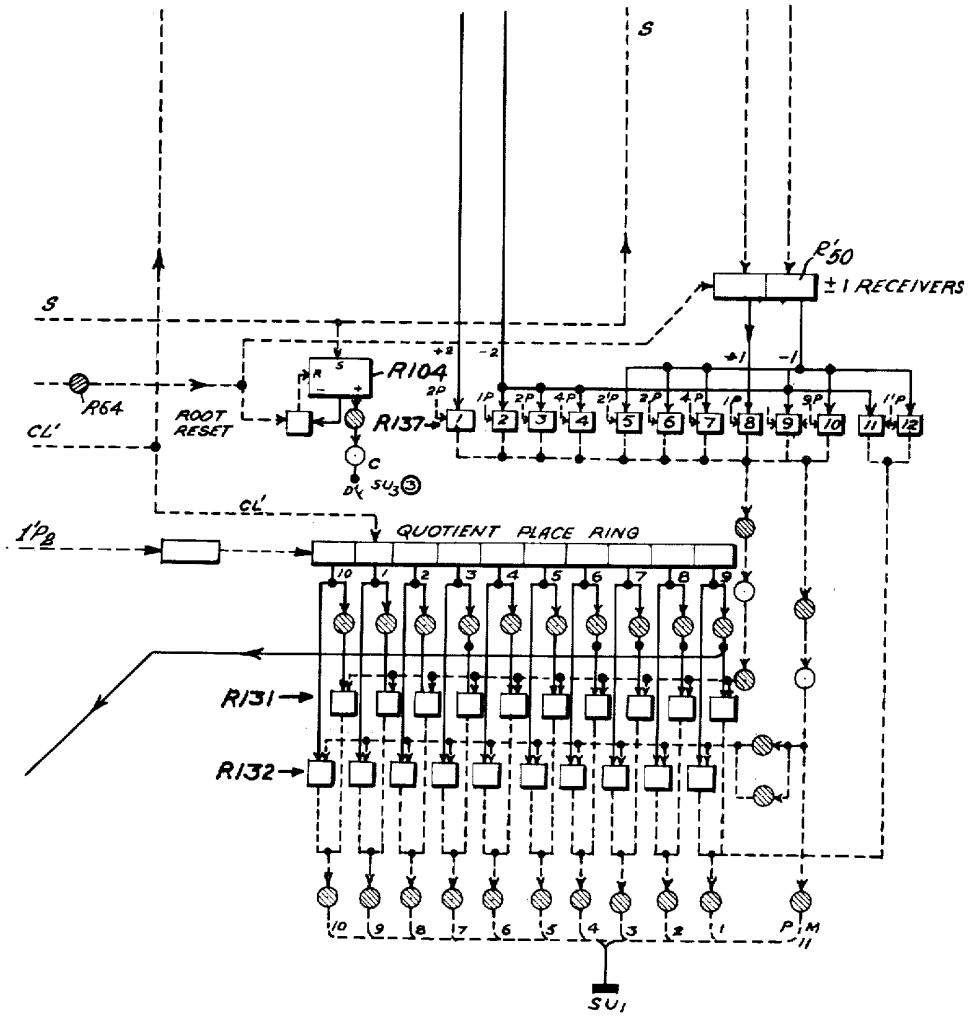
Fig. 46F



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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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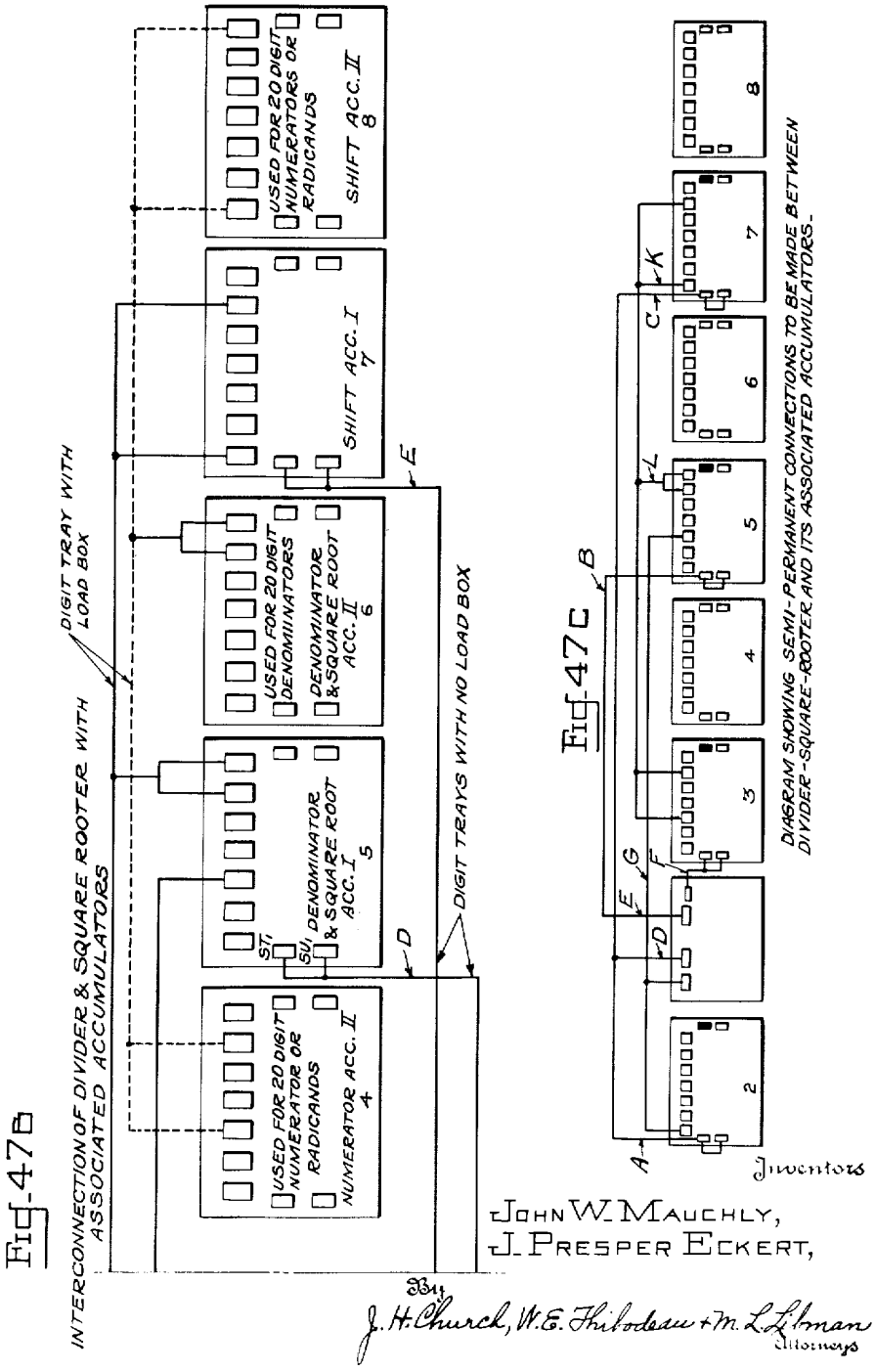

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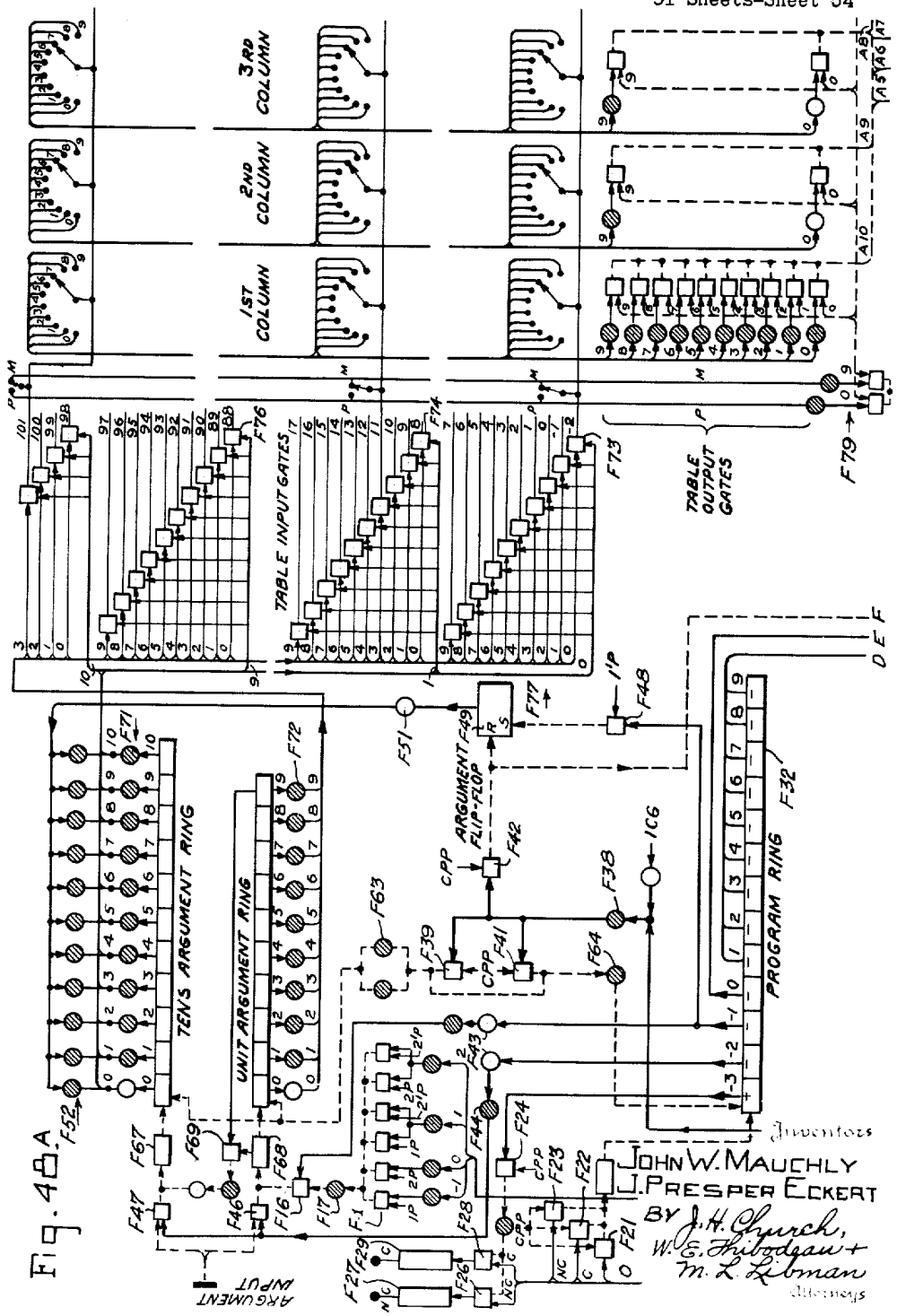

Fig. 48A

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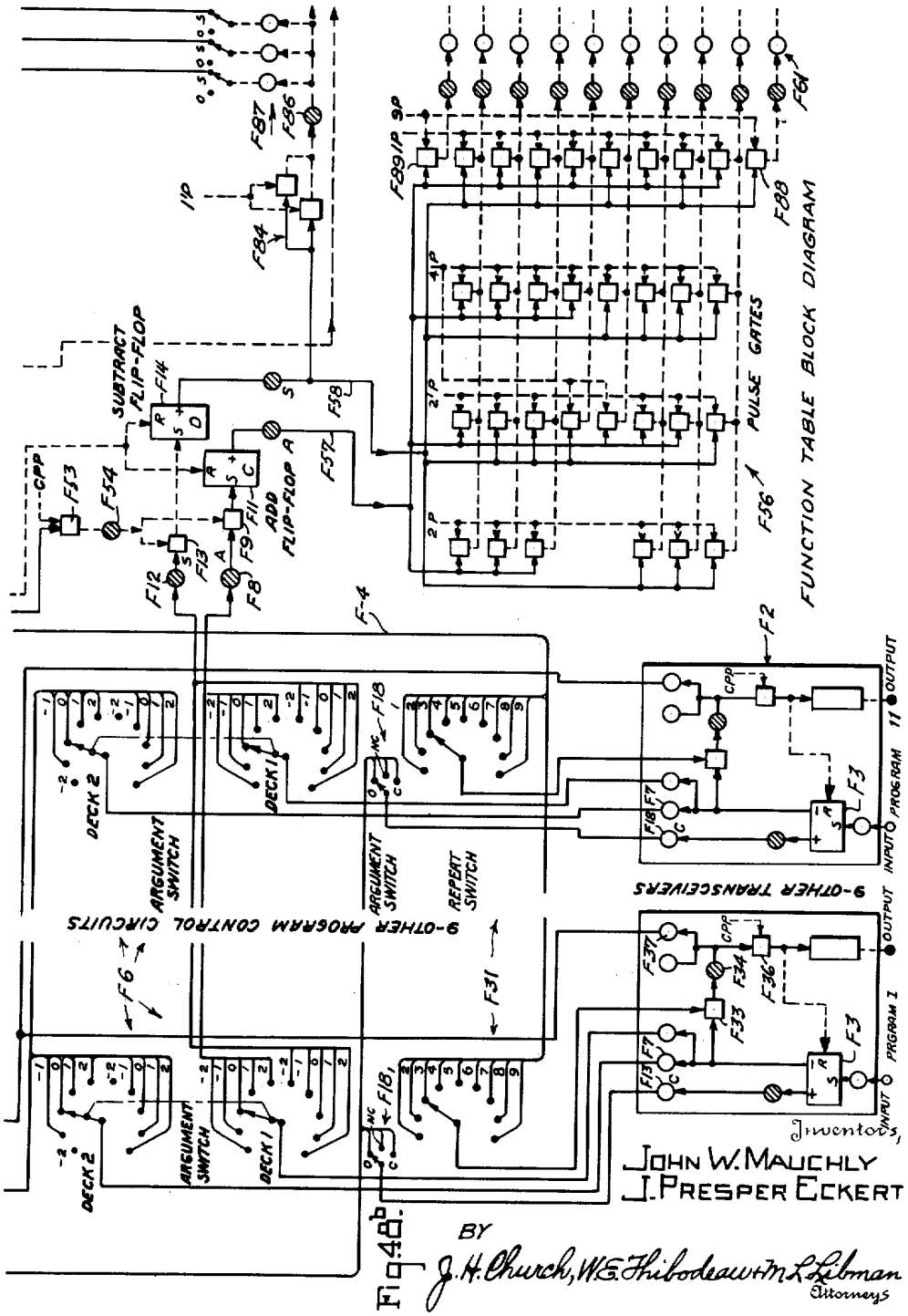

Fig. 48b.

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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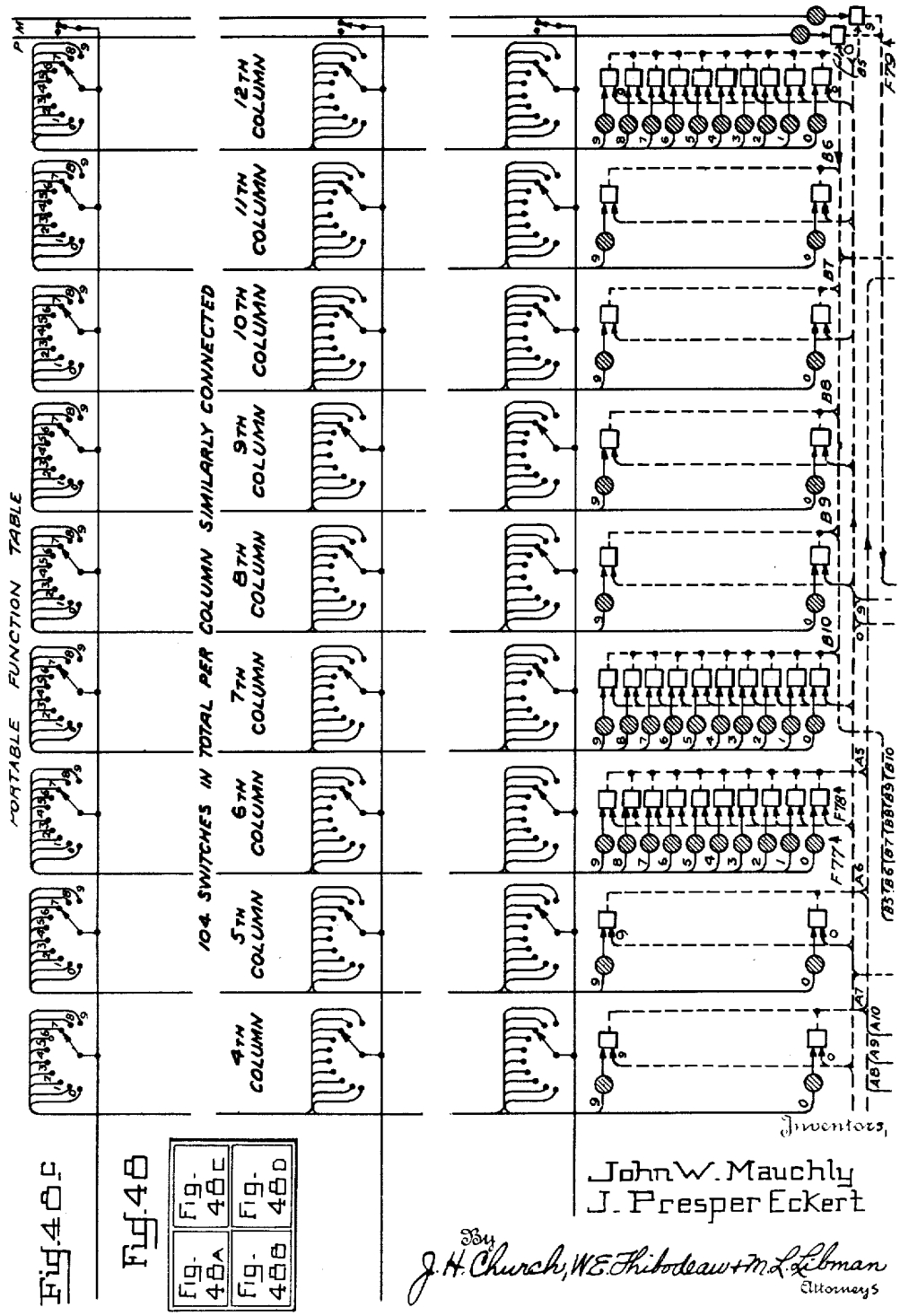

Fig. 48c

Fig. 48

Fig. 48A	Fig. 48C
Fig. 48B	Fig. 48D

ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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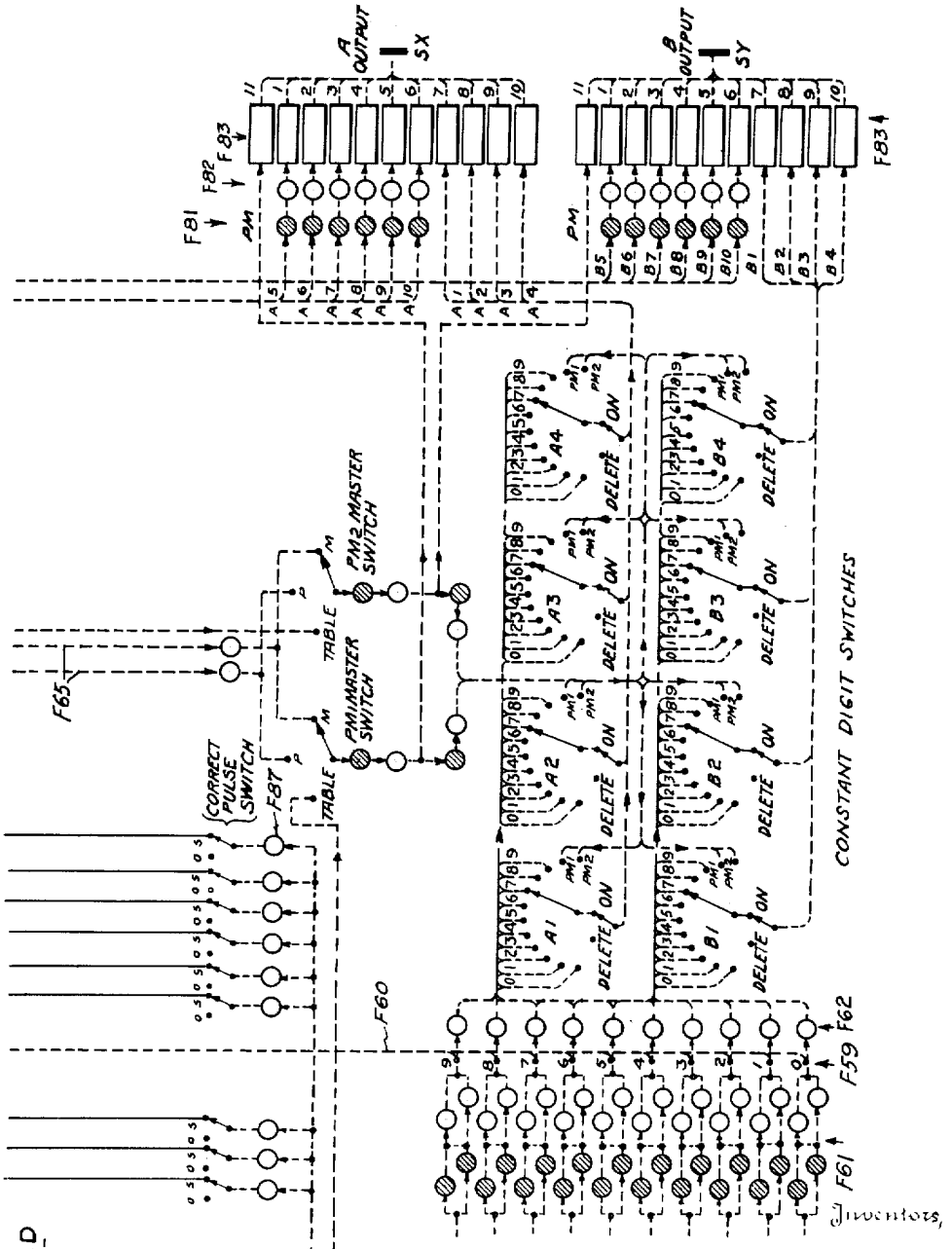

Fig 48D

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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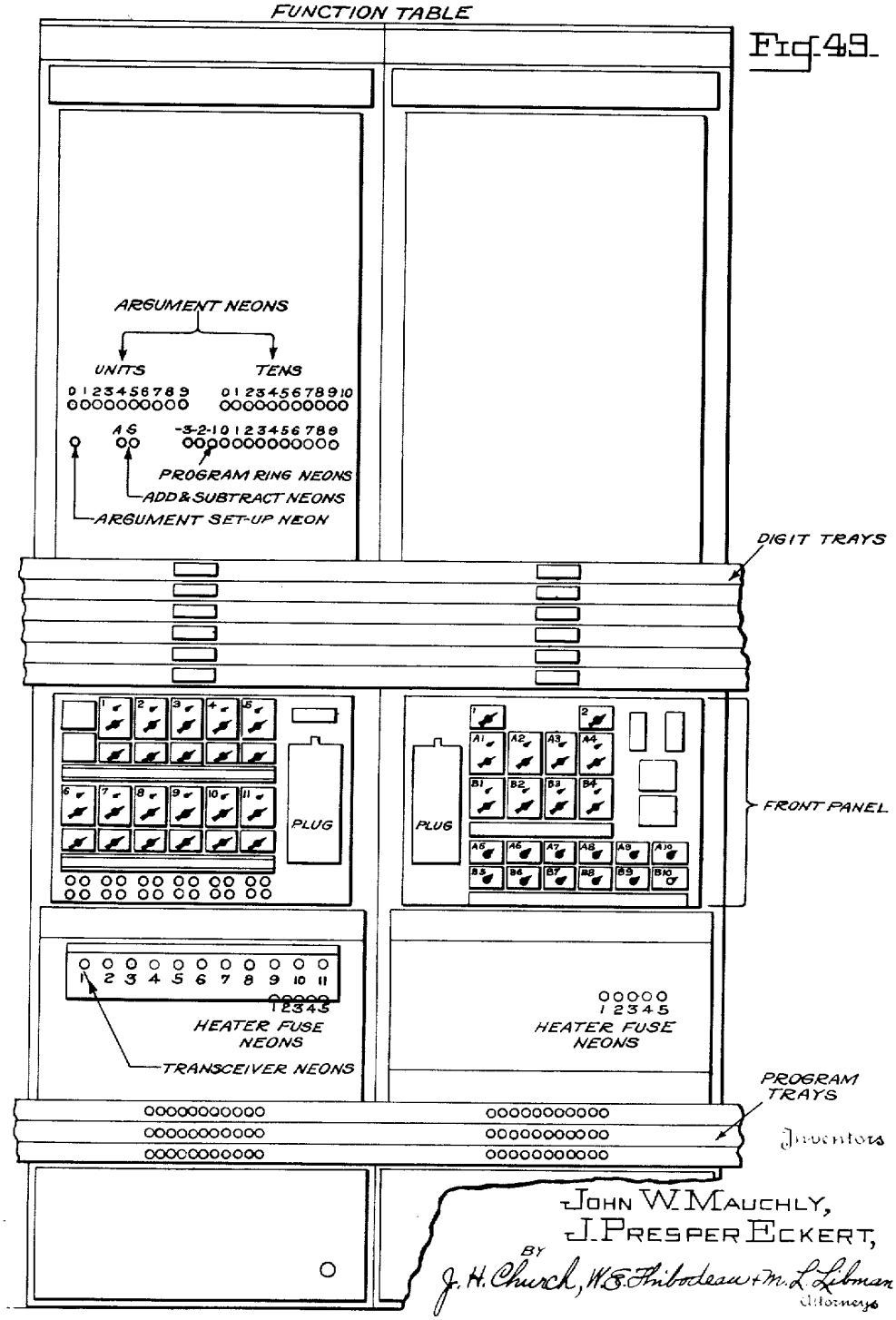
FUNCTION TABLE

Fig. 49.



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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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Fig. 50.

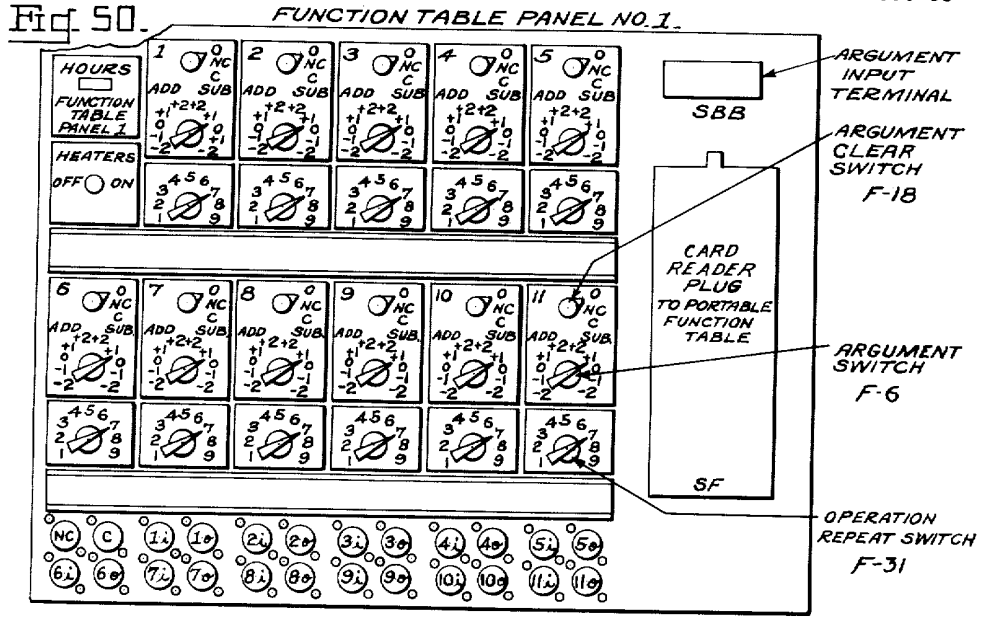

Fig. 51.

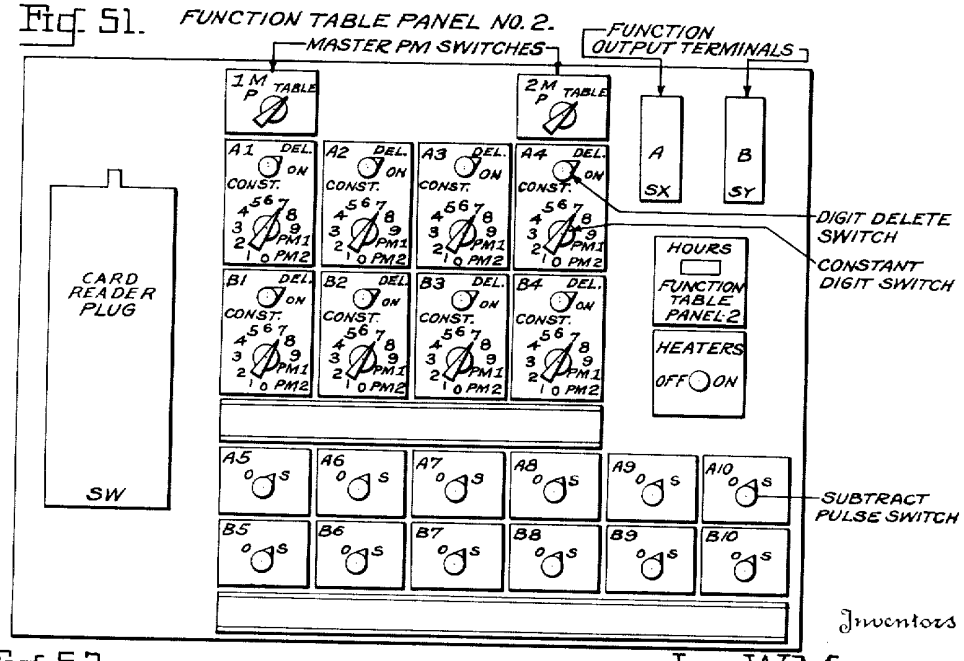

Fig. 52.

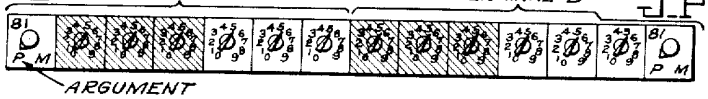

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Fig. 53.

USE OF UNMODIFIED FUNCTION TABLE TO STORE PROGRAMMING INFORMATION.

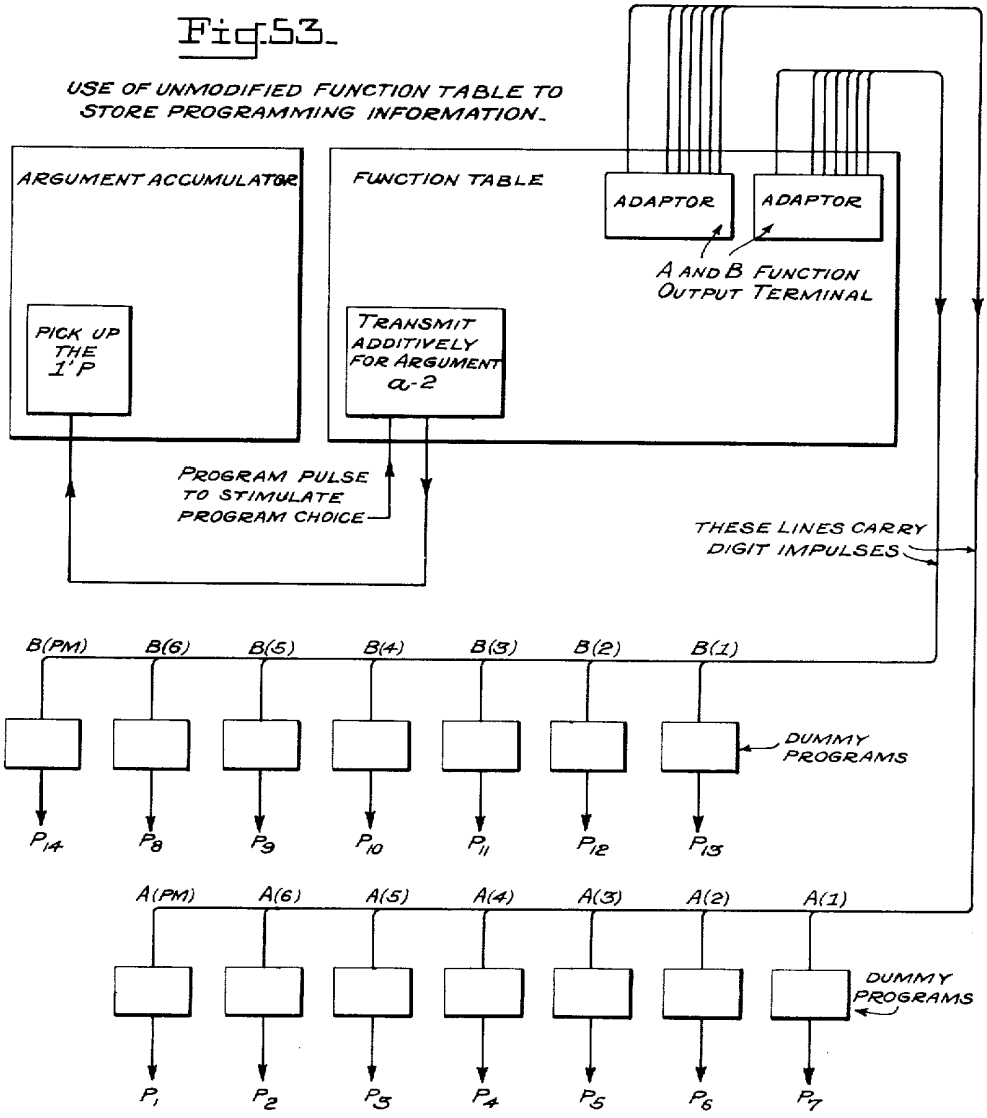

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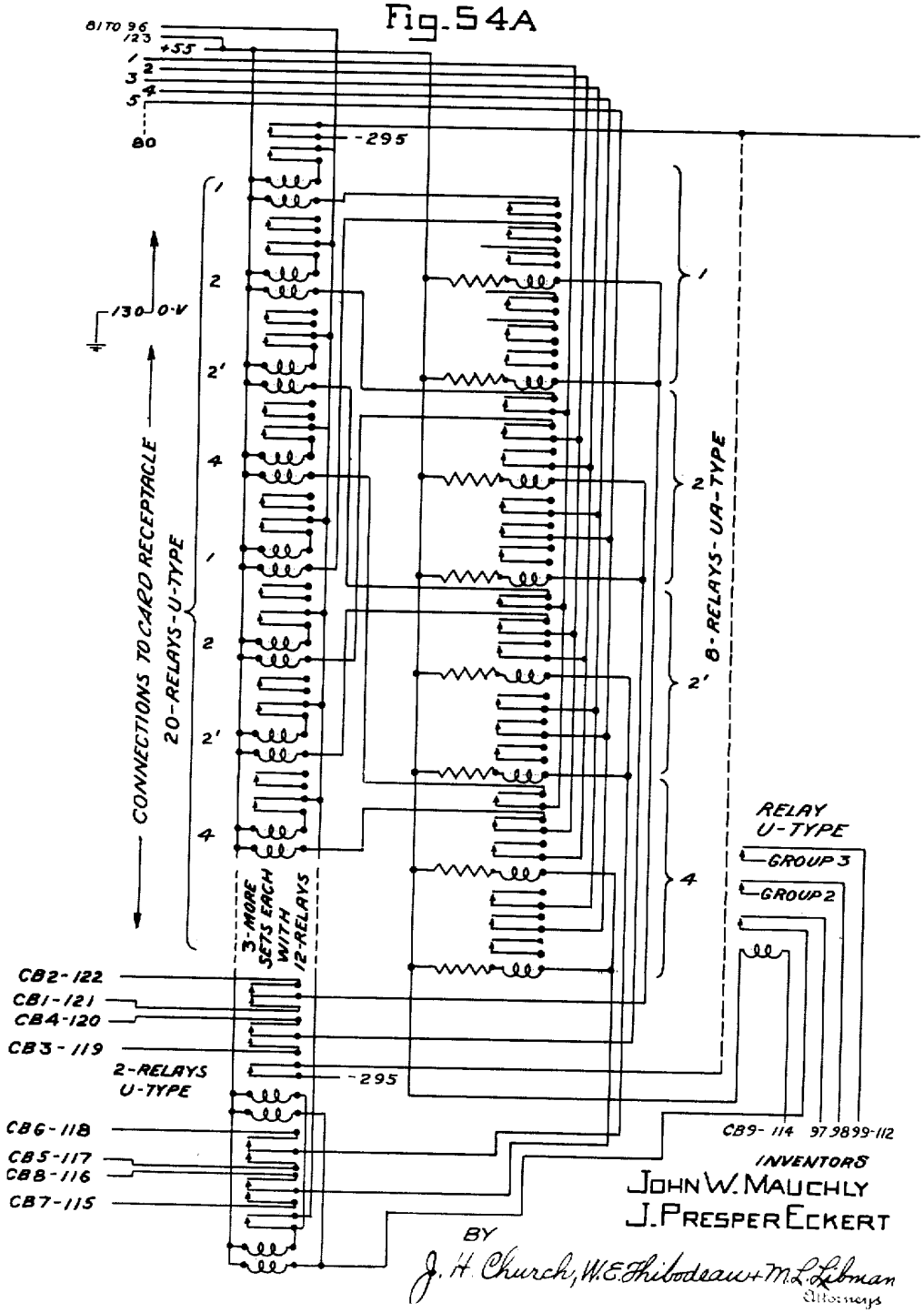
Fig. 54A



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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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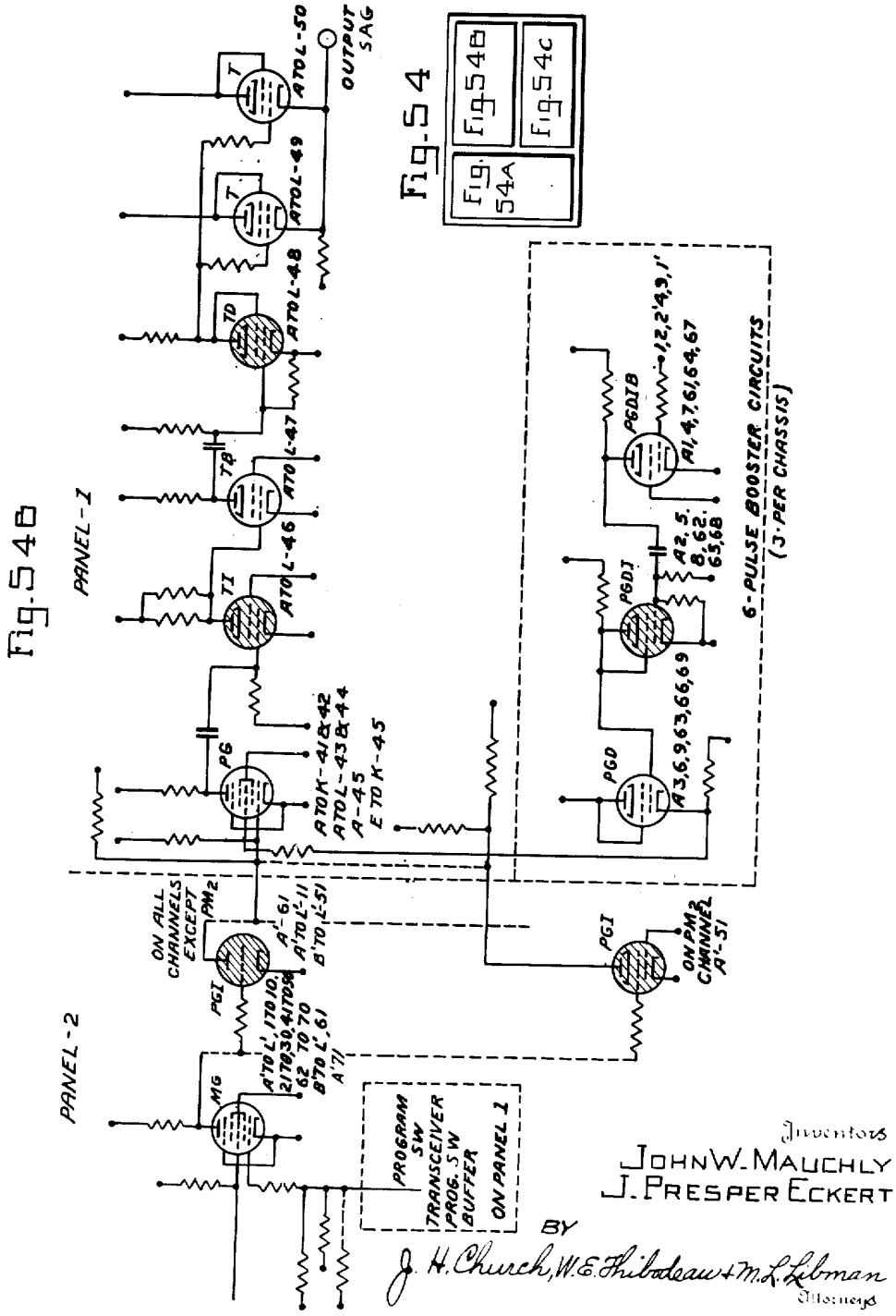
Fig. 54



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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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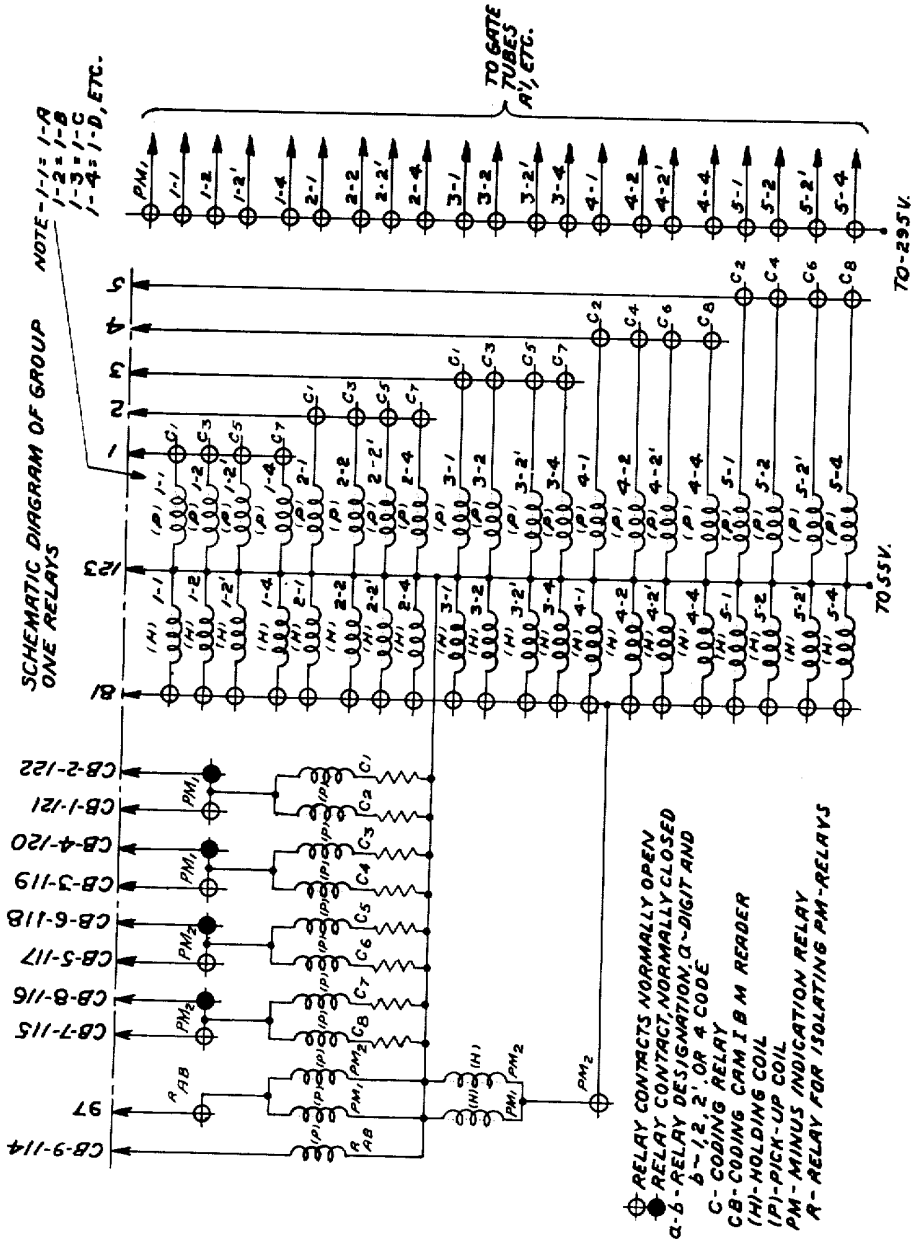
Fig. 54C



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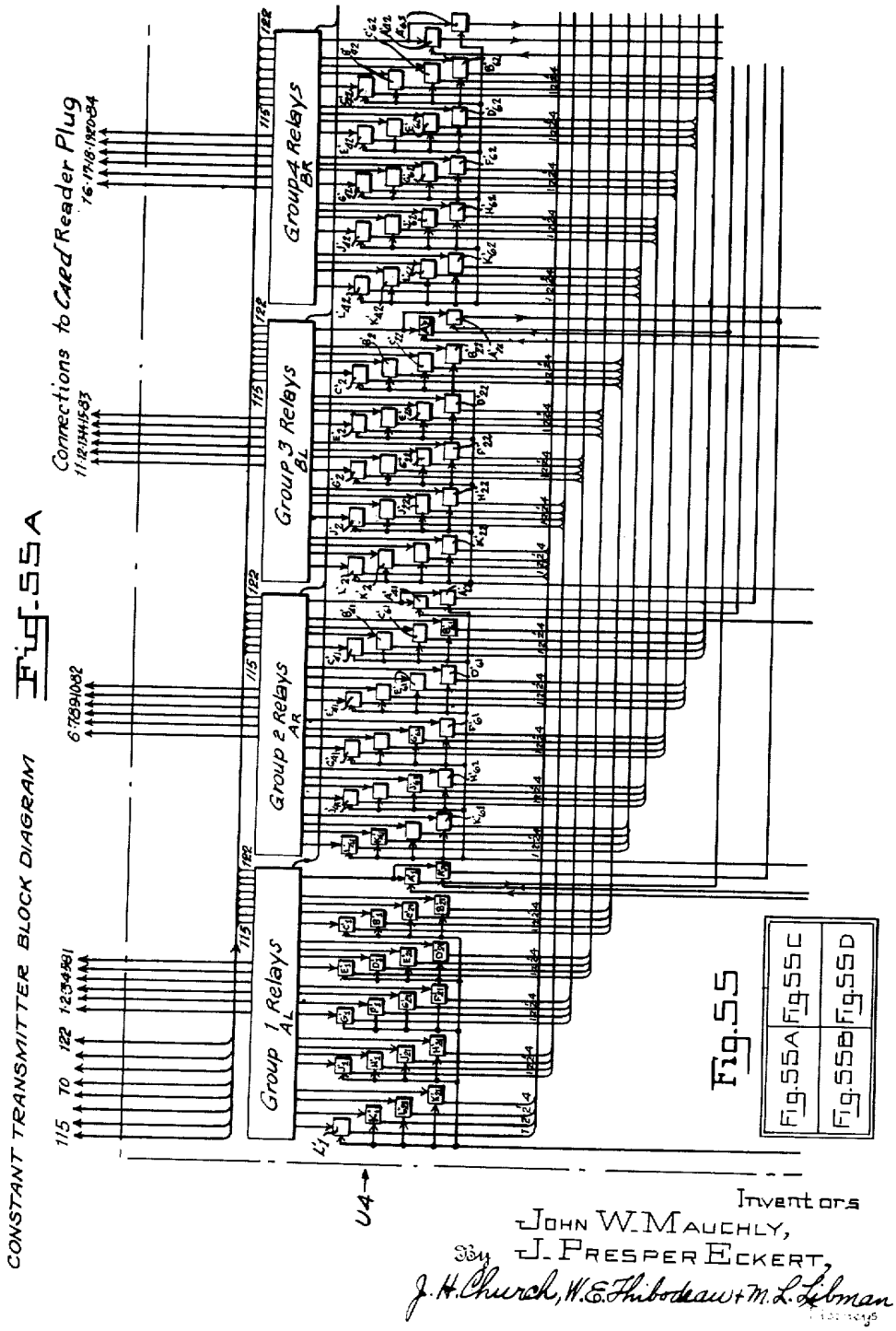

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

Filed June 26, 1947 91 Sheets-Sheet 65

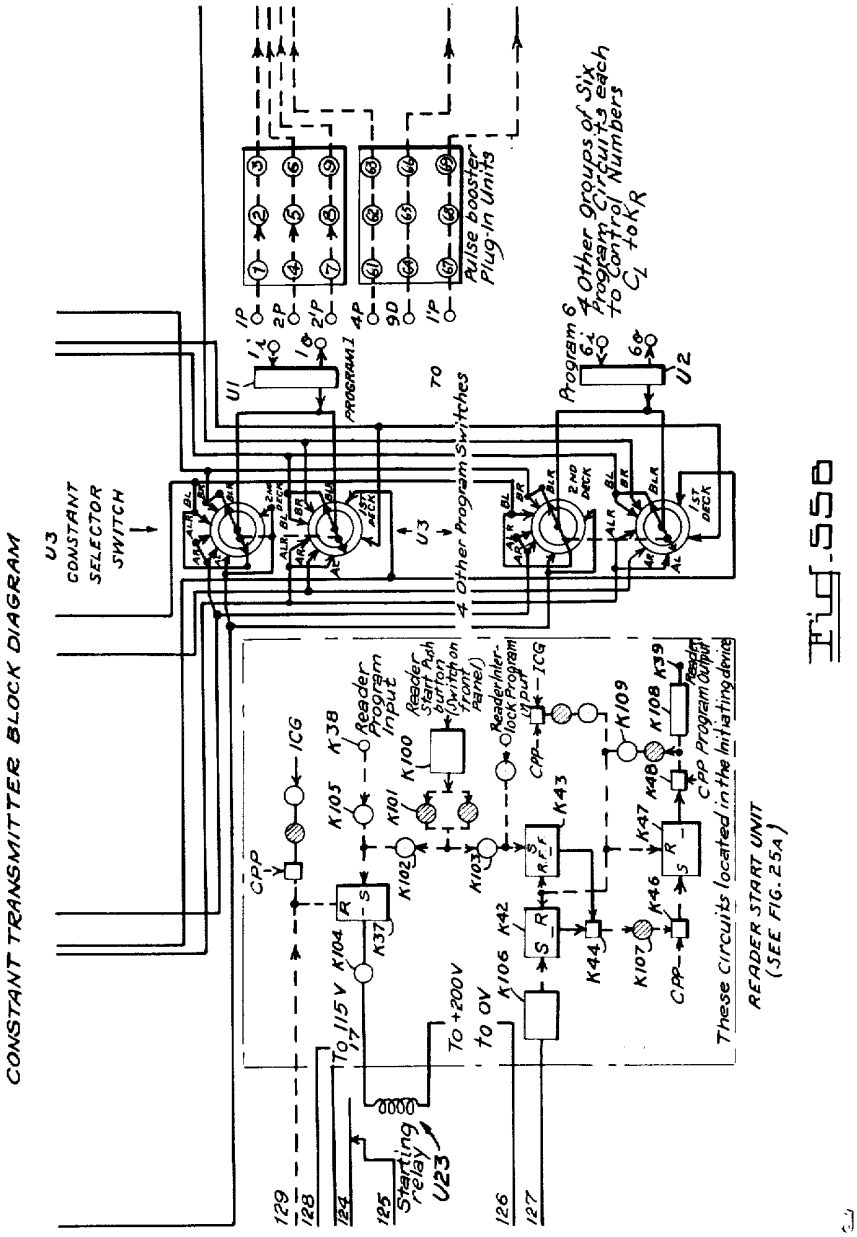

Fig. 55b

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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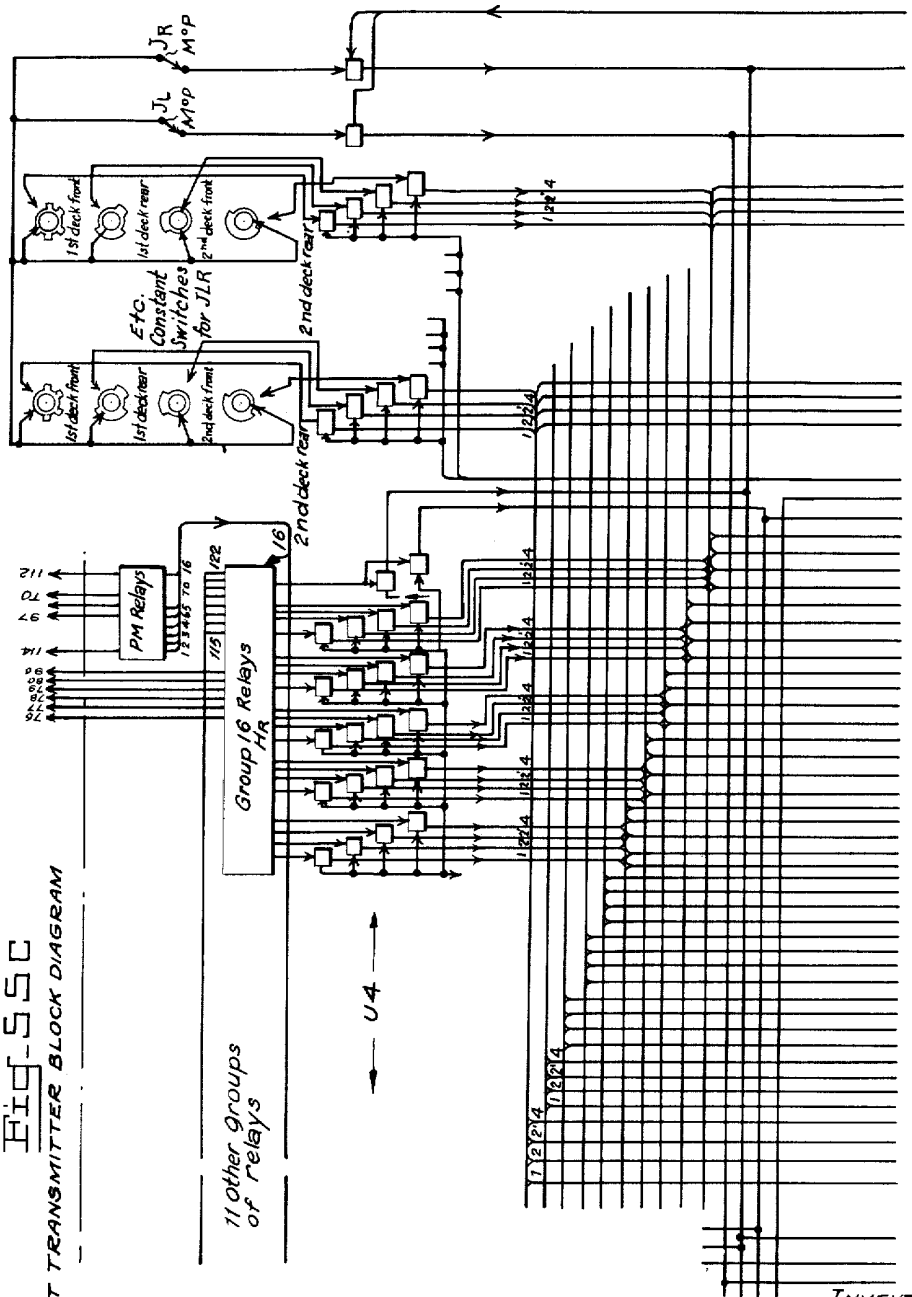

Fig. 55C

CONSTANT TRANSMITTER BLOCK DIAGRAM

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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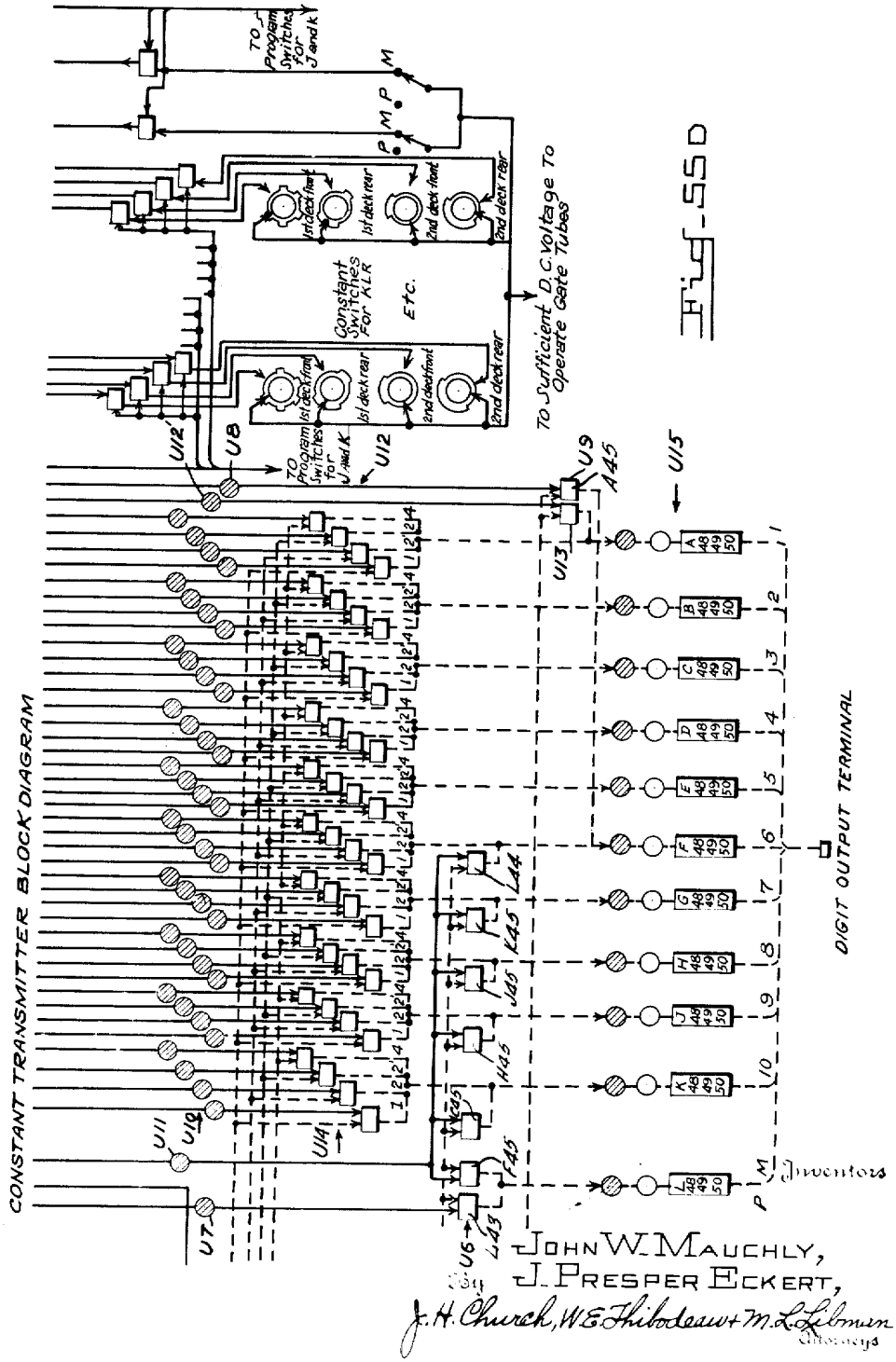

Fig. 55D

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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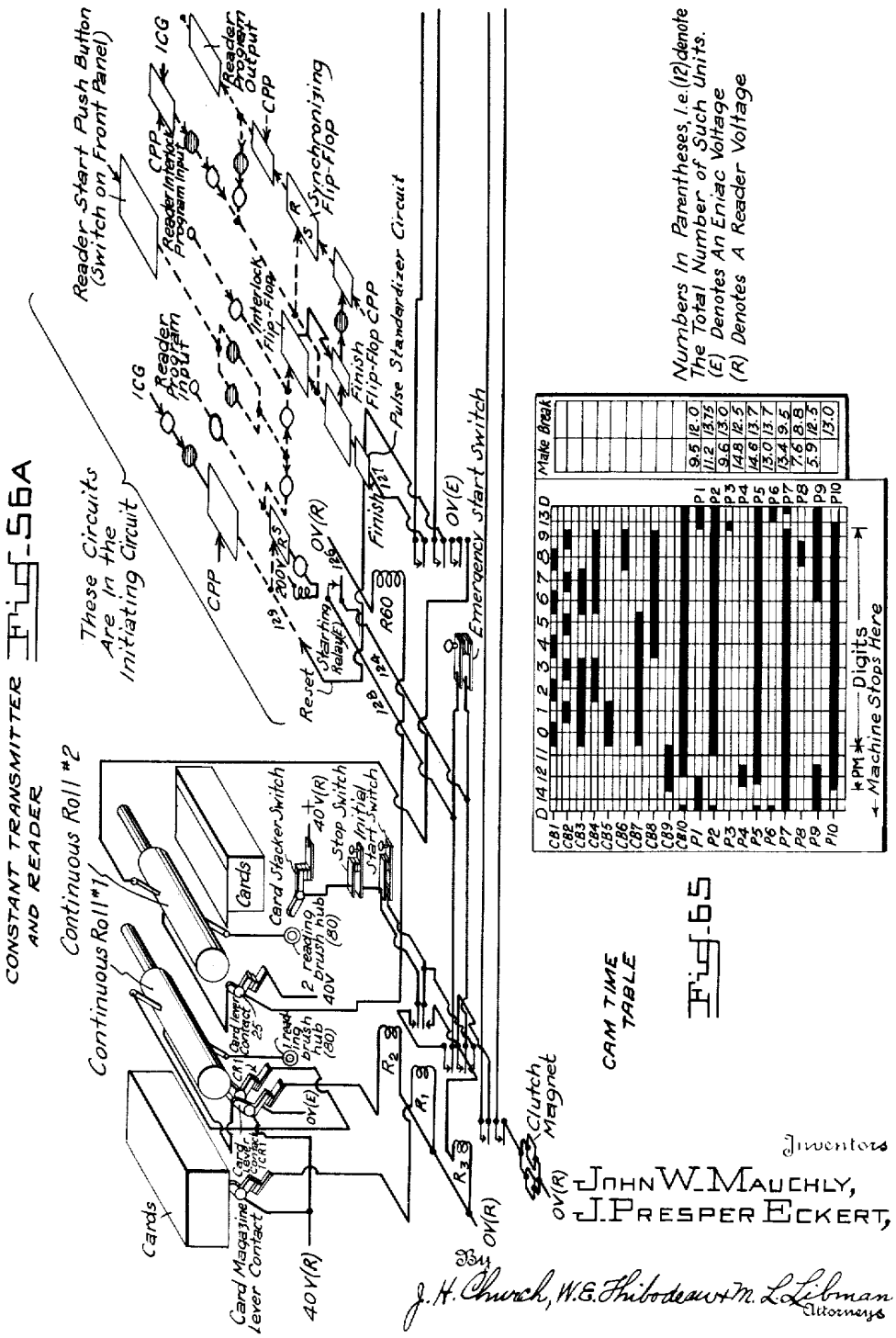

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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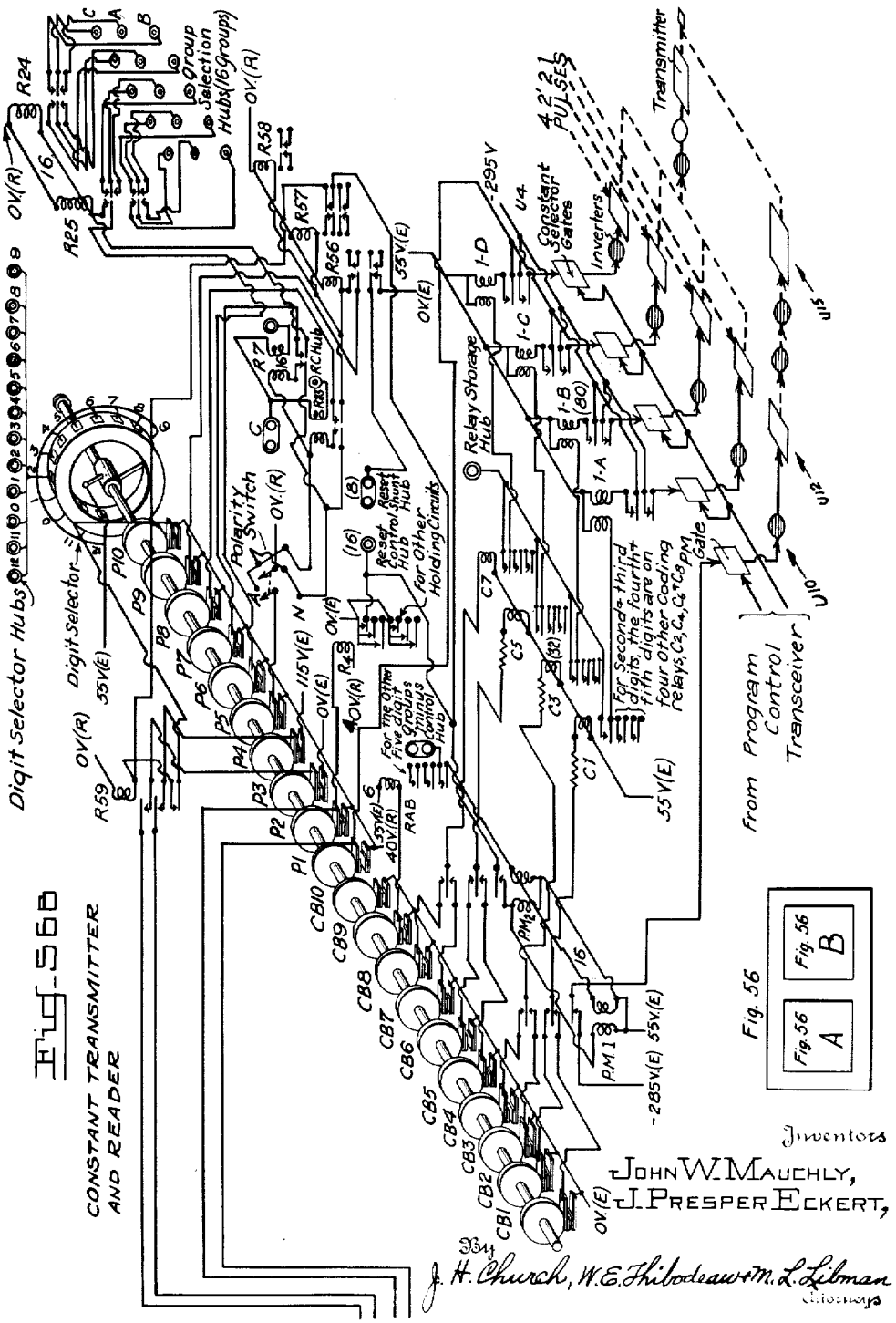

Fig. 56

CONSTANT TRANSMITTER AND READER

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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Fig. 57A

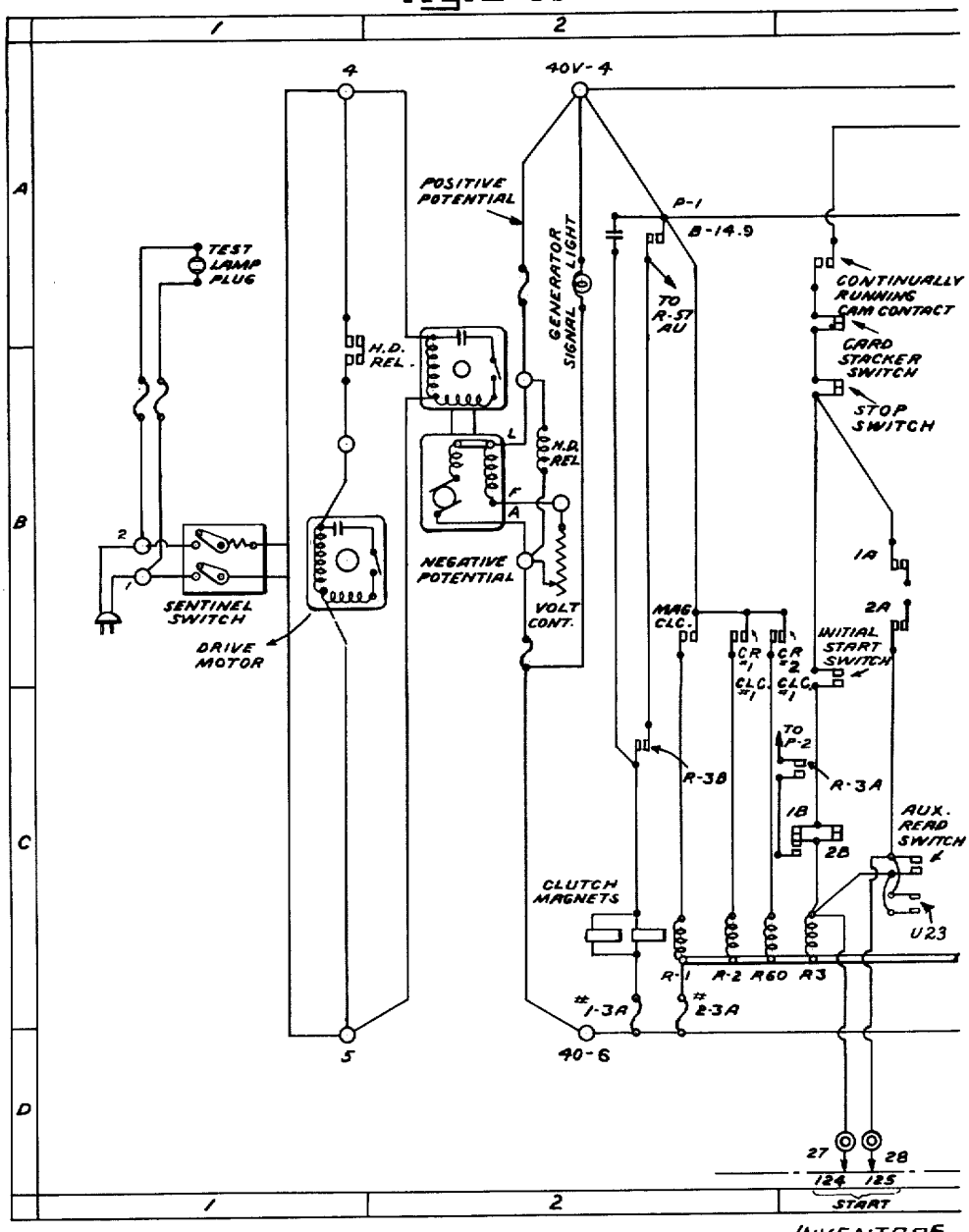

Fig. 57A | Fig. 57B | Fig. 57C

Fig. 57

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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Fig. 57B

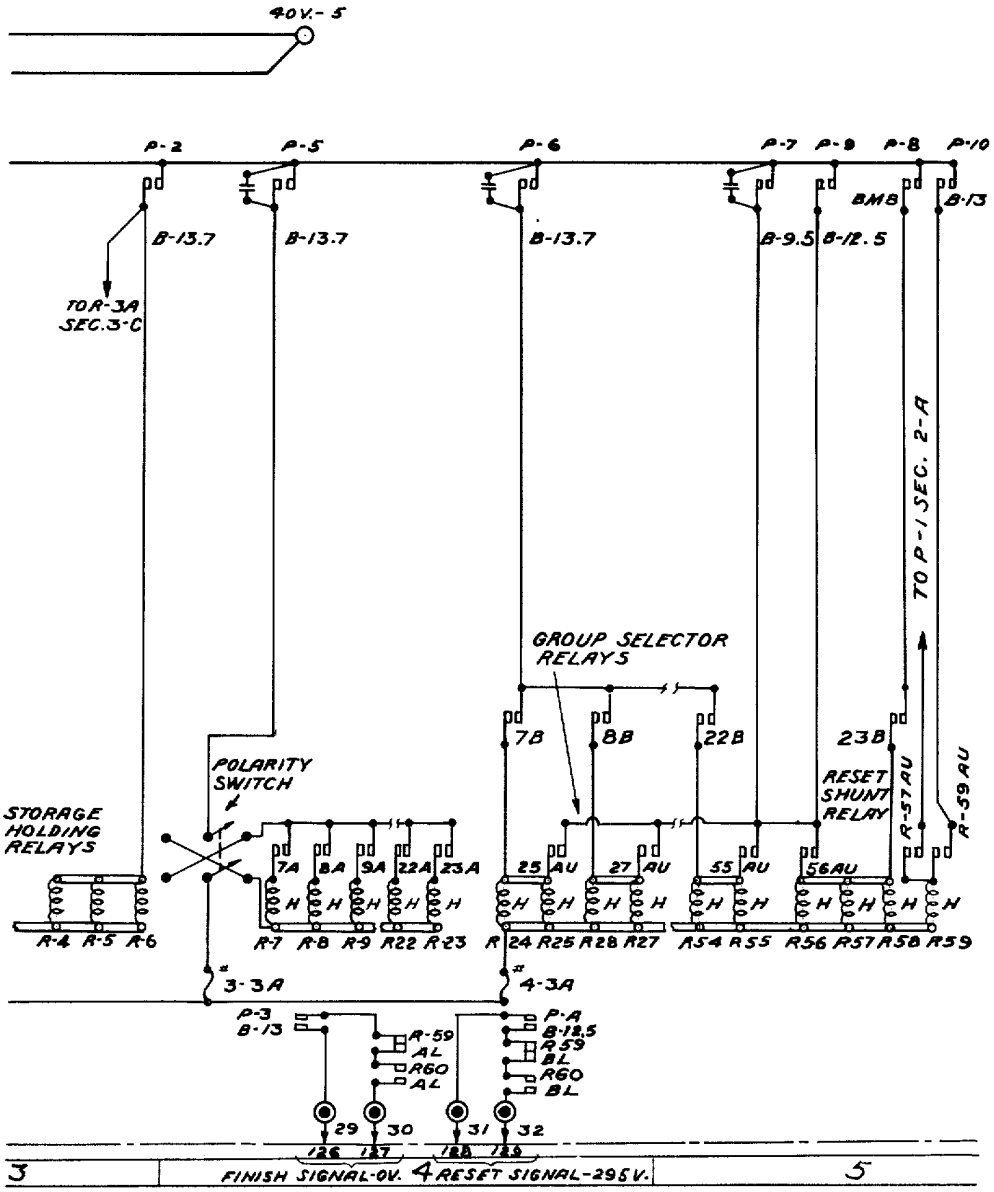

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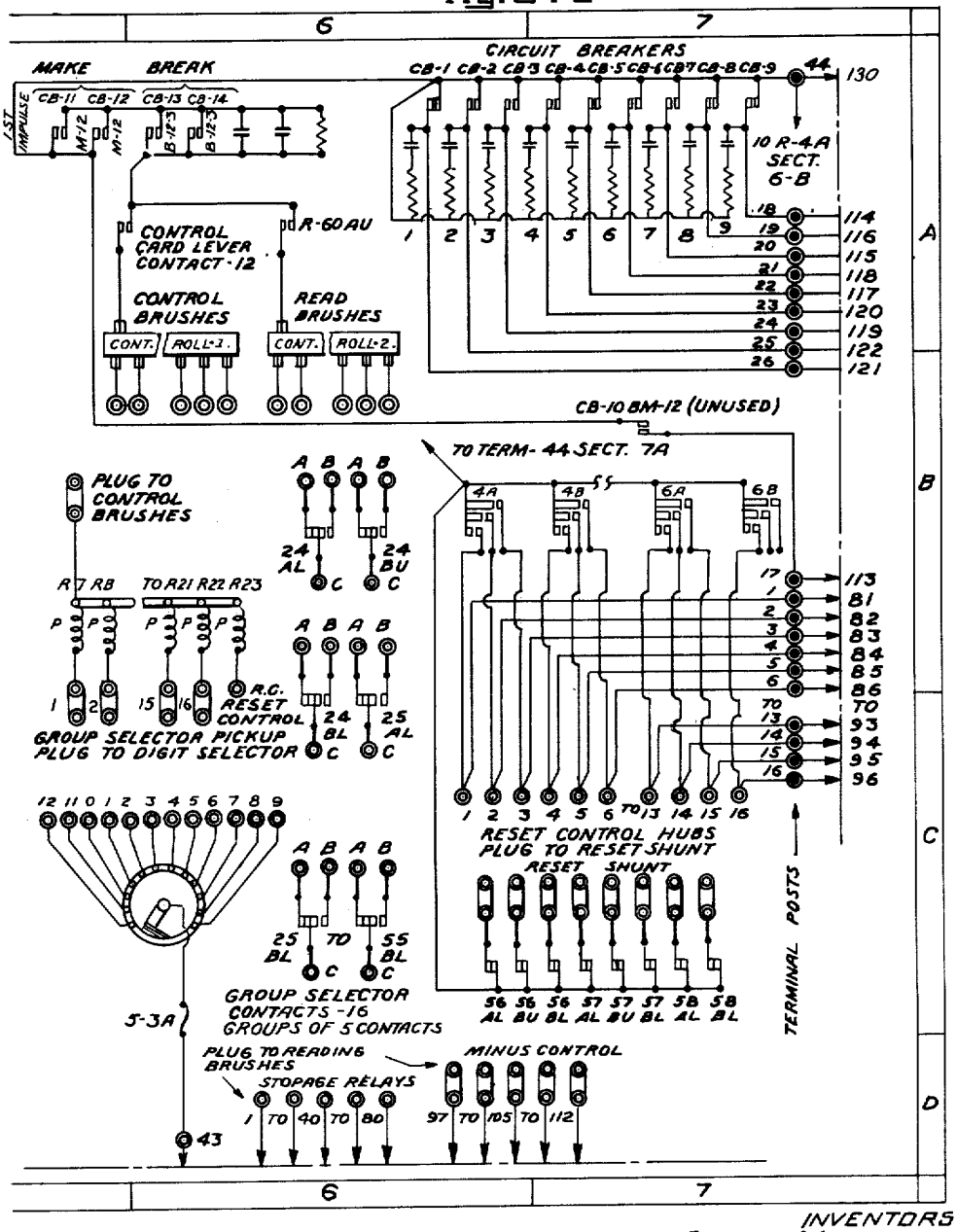
Fig. 57c



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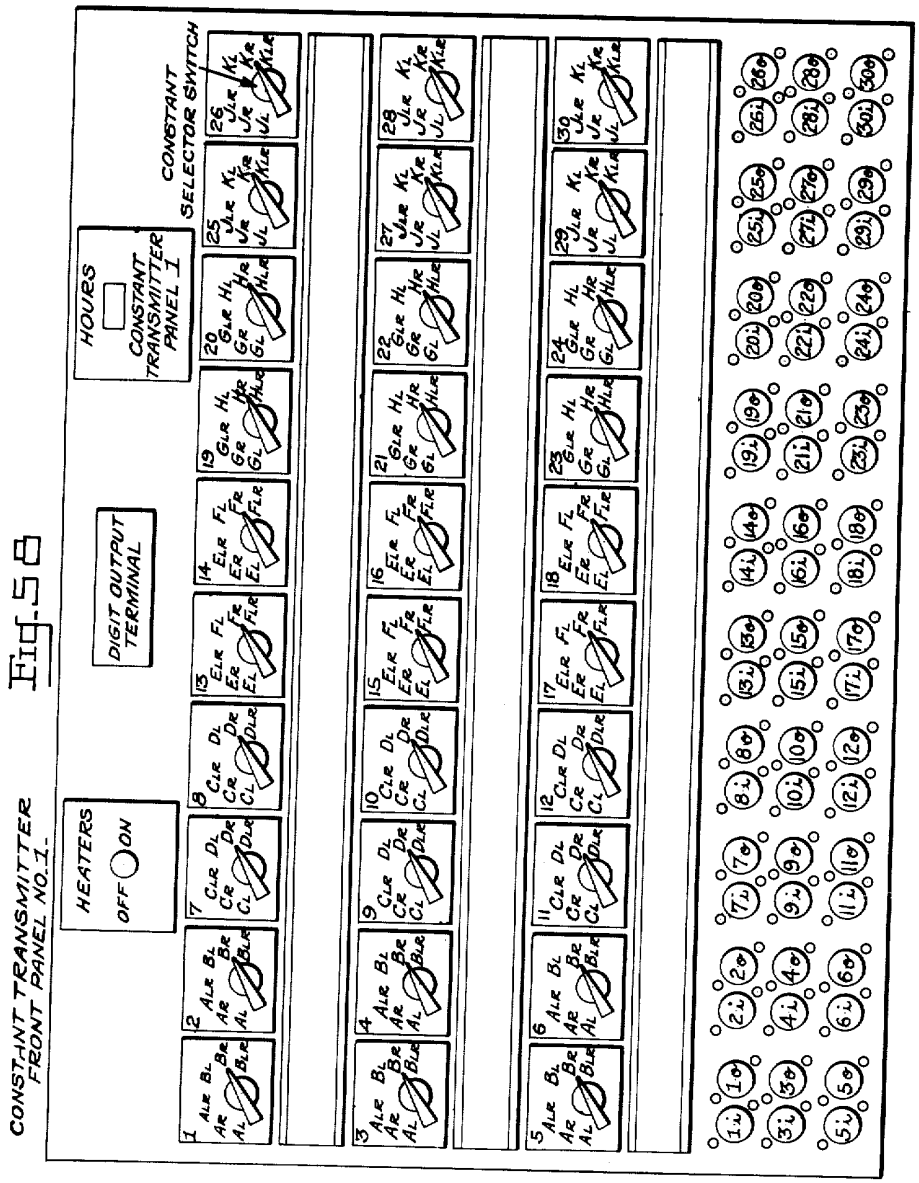

Fig. 58

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Fig. 59

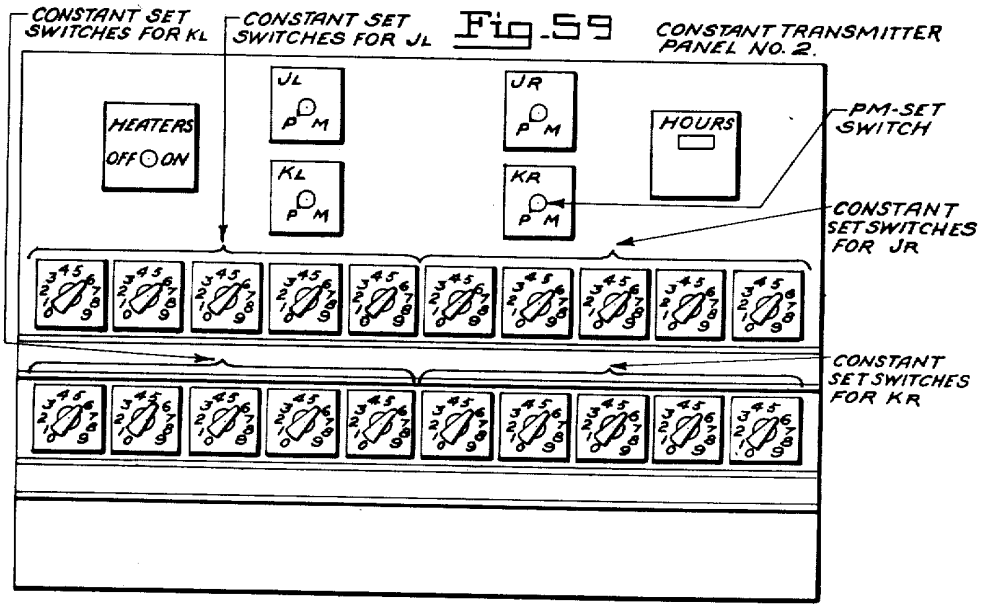
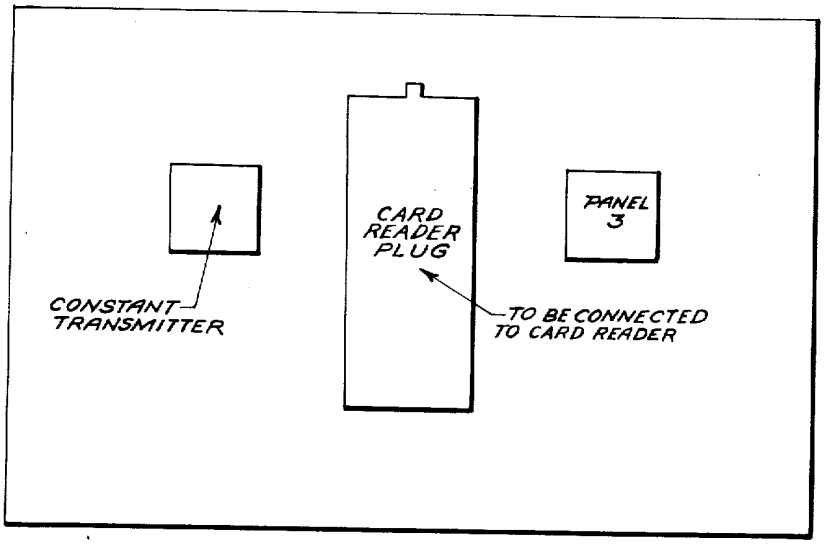


Fig. 60



CONSTANT TRANSMITTER PANEL #3

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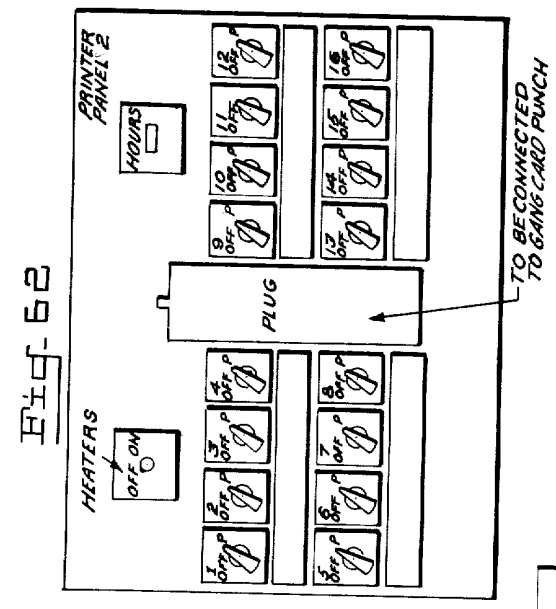

Fig. 62

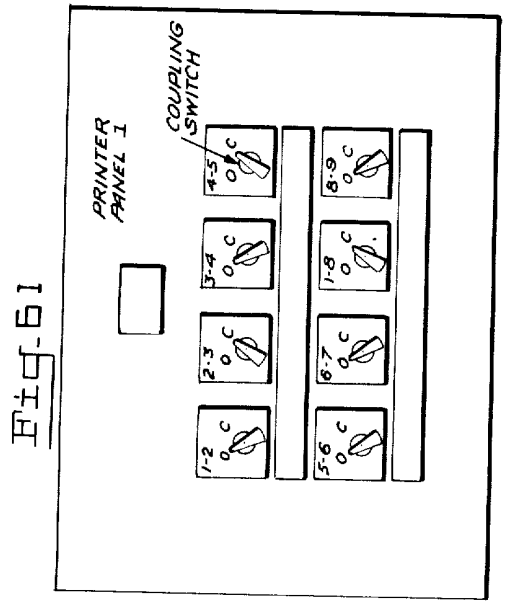

Fig. 61

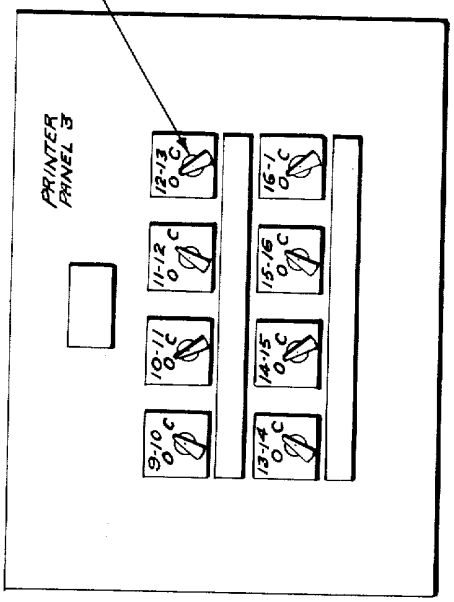

Fig. 63

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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Fig. 64

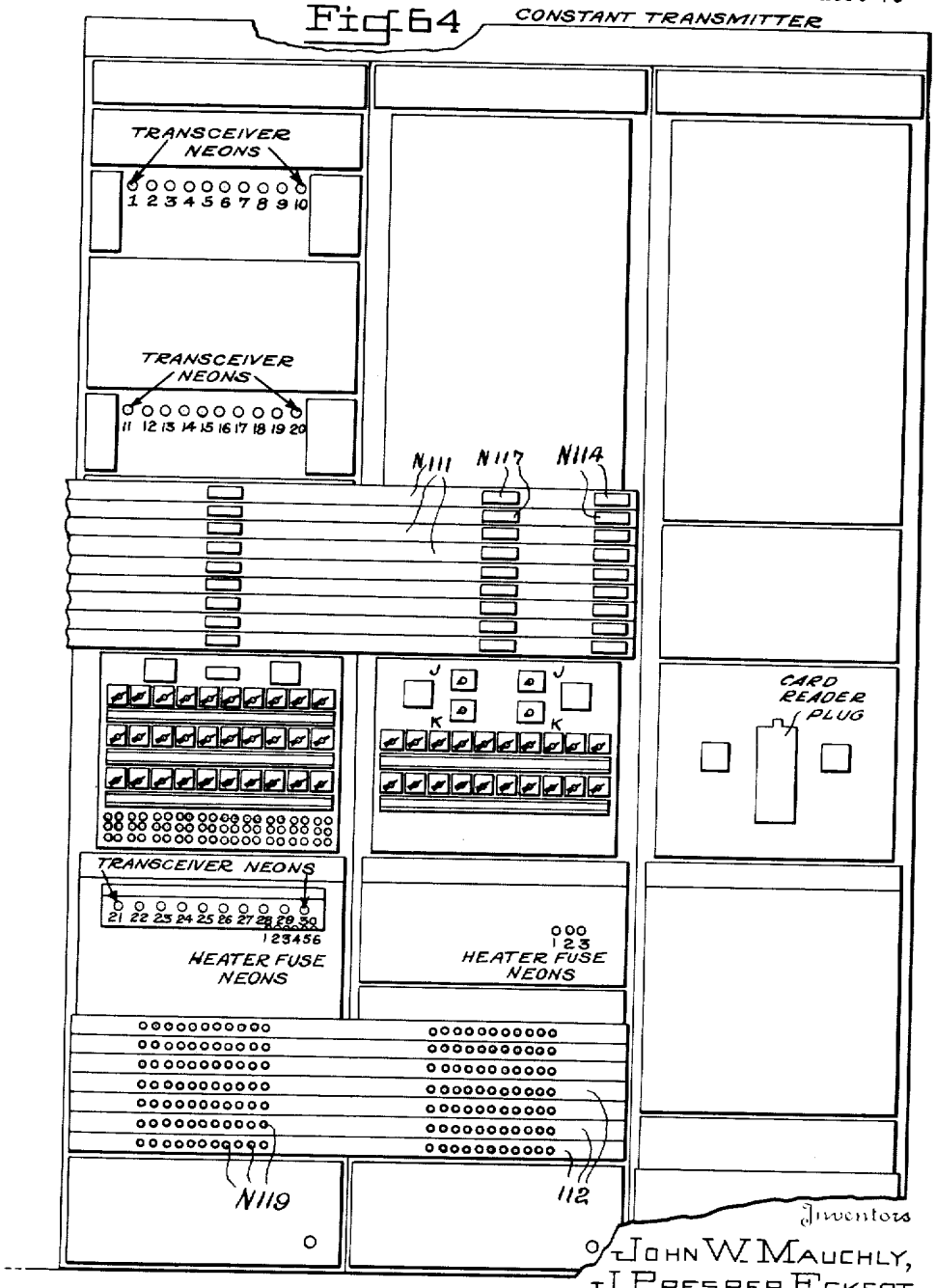

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Fig. 66A CARD PUNCH

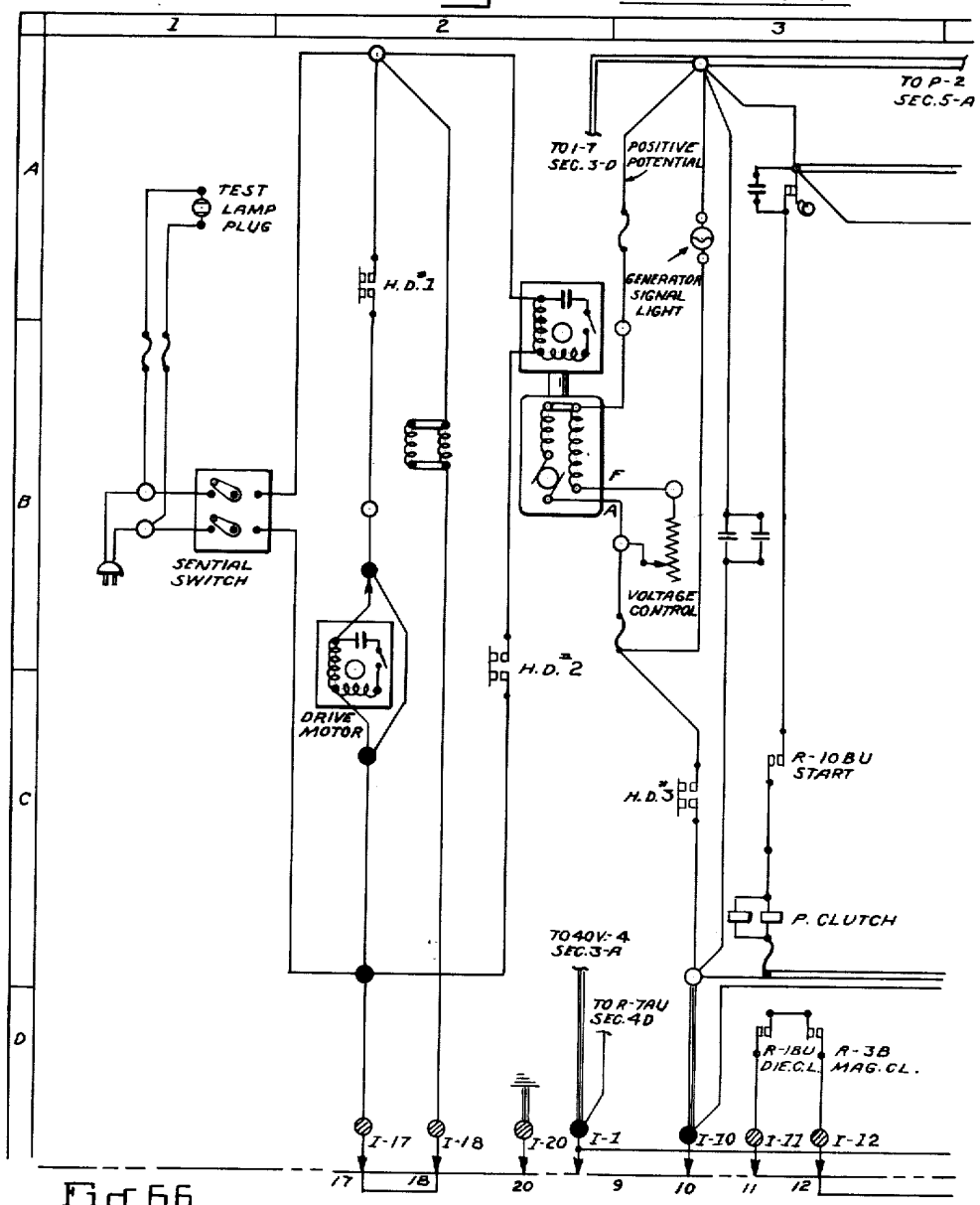

Fig. 66

Fig. 66A	Fig. 66B	Fig. 66C

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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Fig. 66B CARD PUNCH

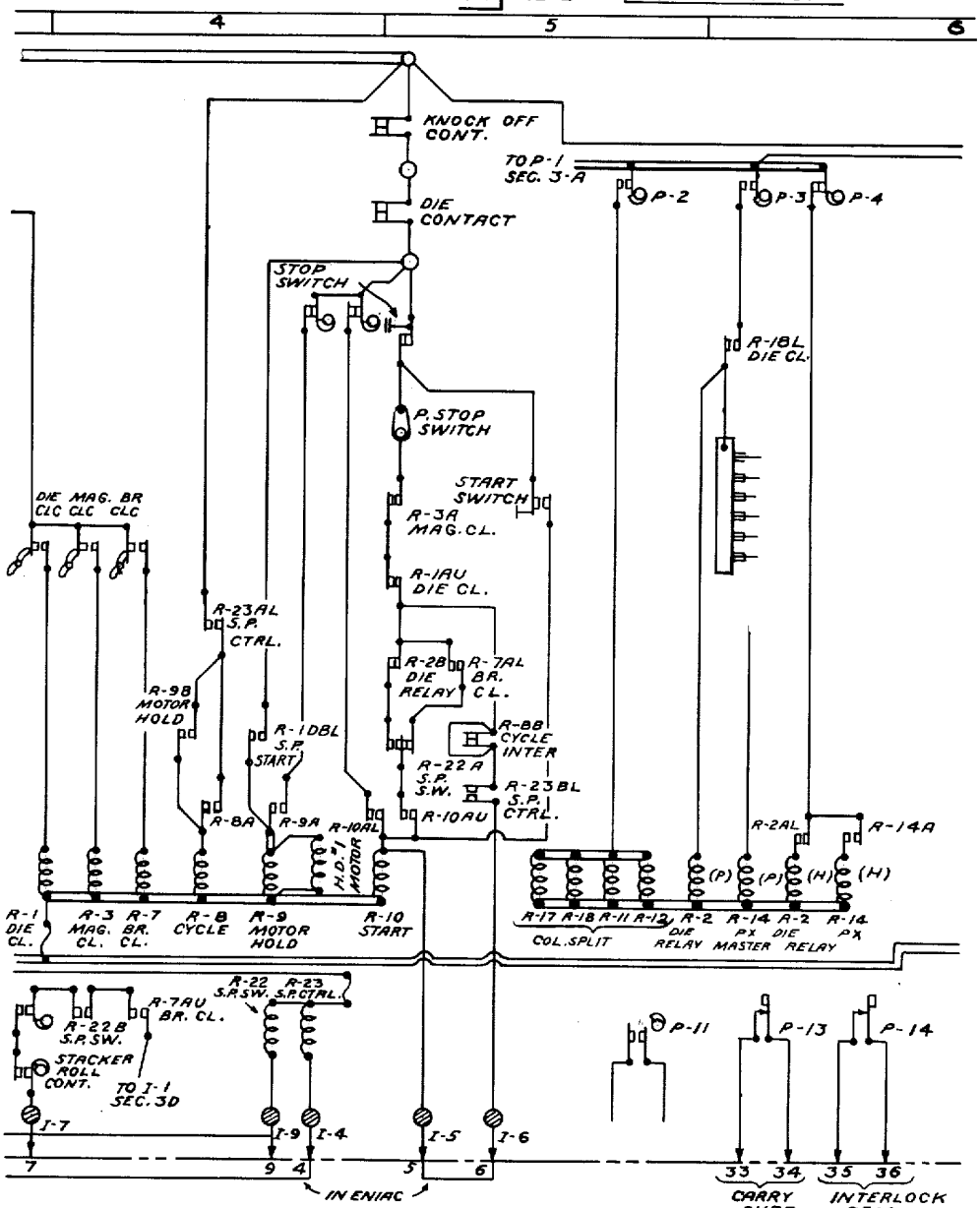

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Fig. 66 c CARD PUNCH

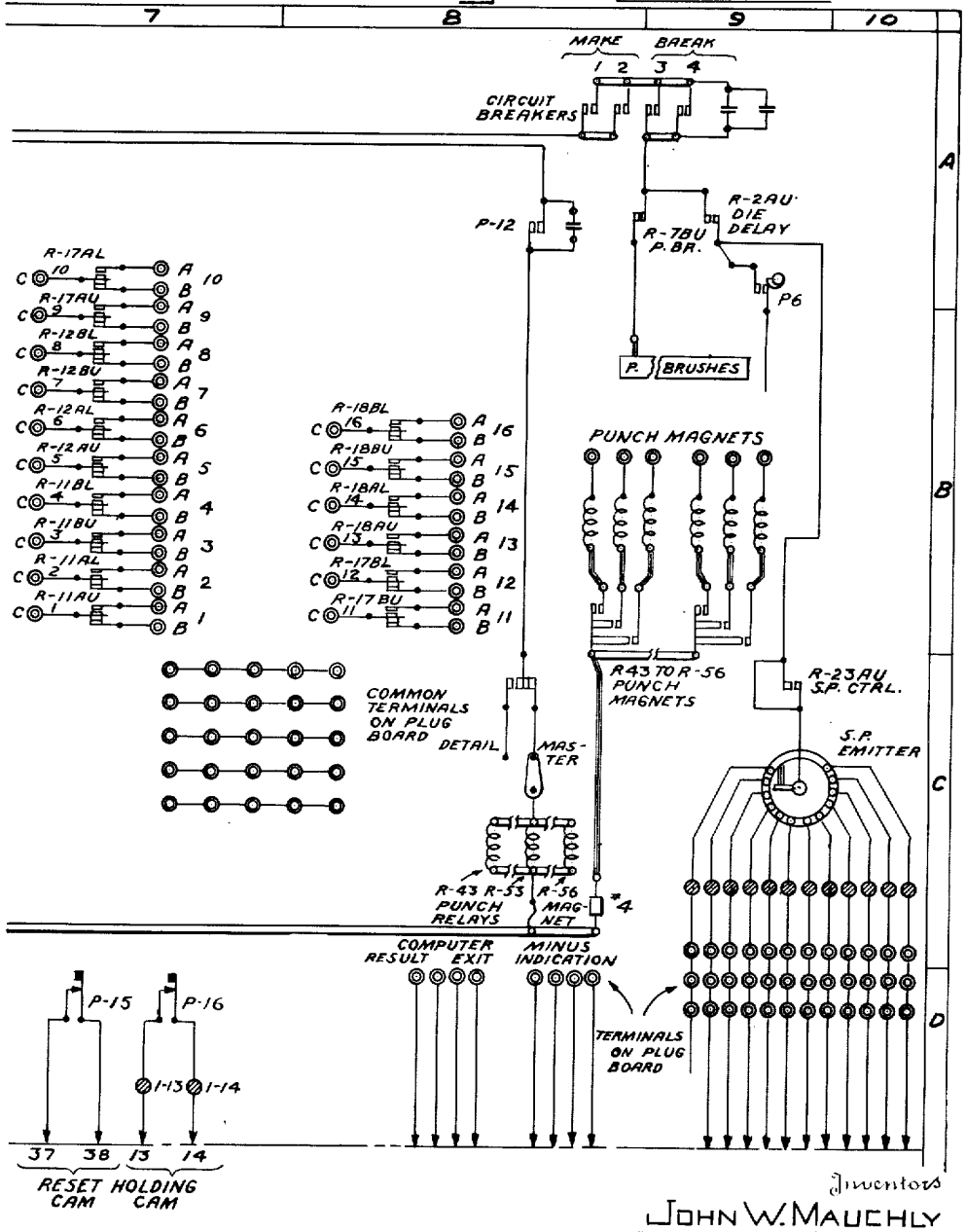

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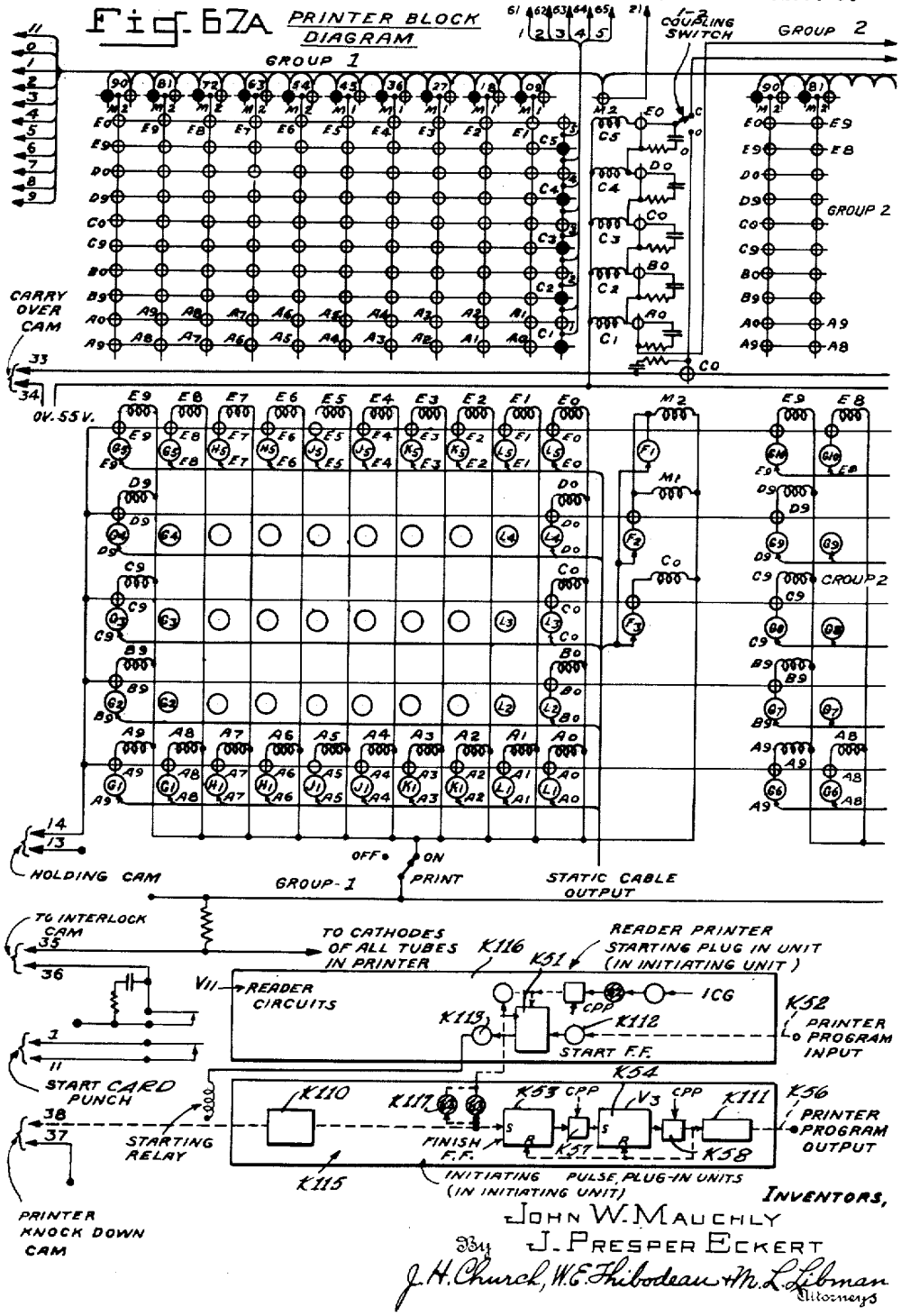
Fig. 67A PRINTER BLOCK DIAGRAM



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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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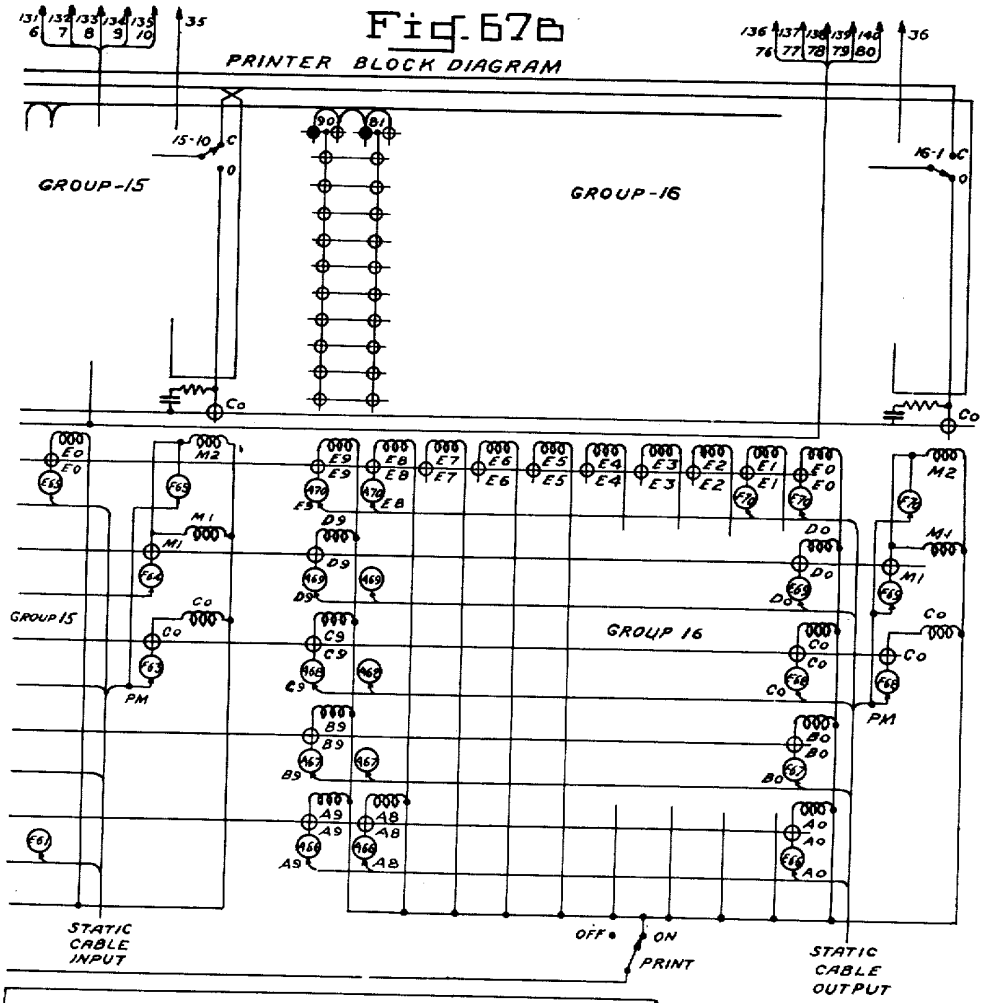
Fig. 67a

PRINTER BLOCK DIAGRAM



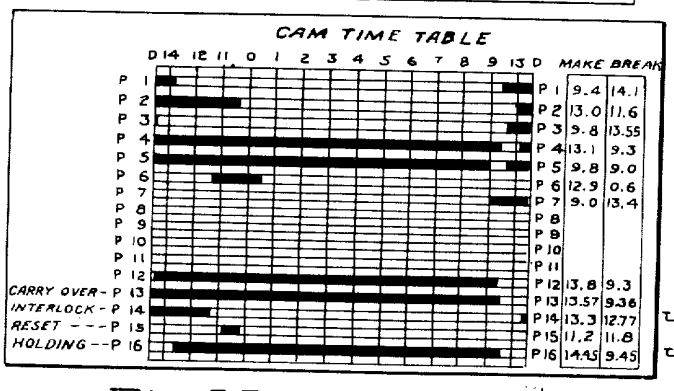


Fig. 67b

Fig. 67

Fig. 67a	Fig. 67b

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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Fig. 68A

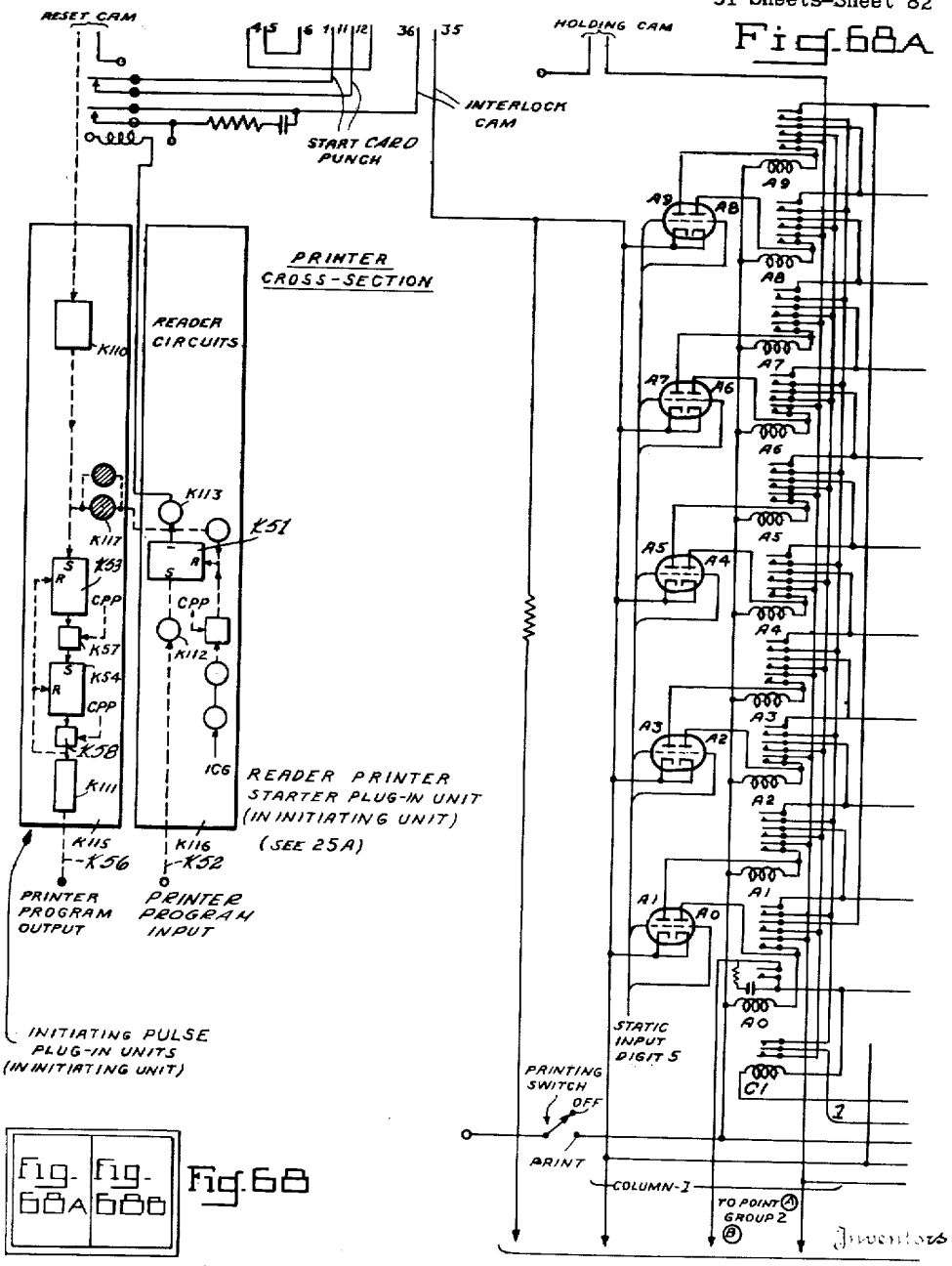

Fig. 68A | Fig. 68B

Fig. 68

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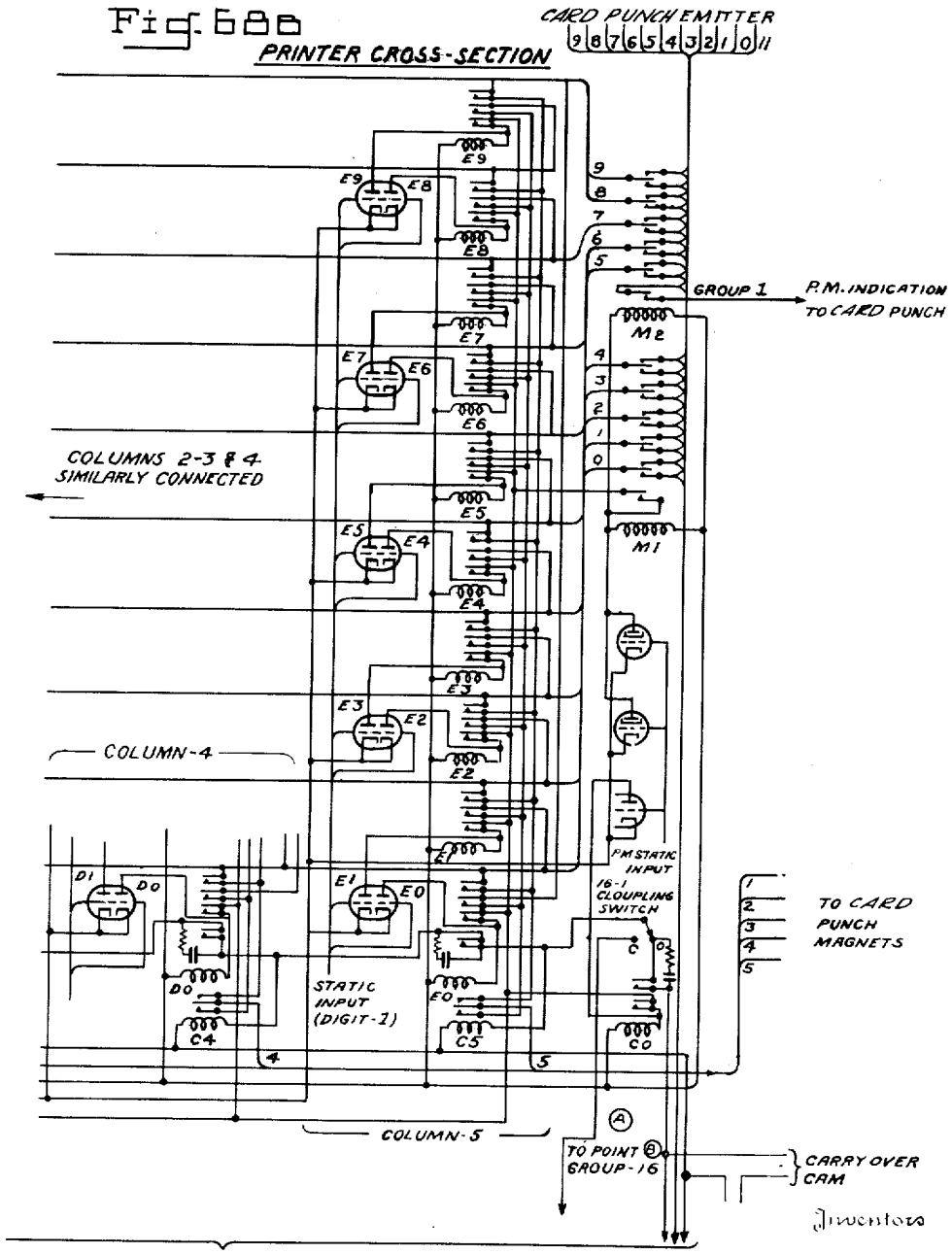
ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

Filed June 26, 1947 91 Sheets-Sheet 83

Fig. 68a



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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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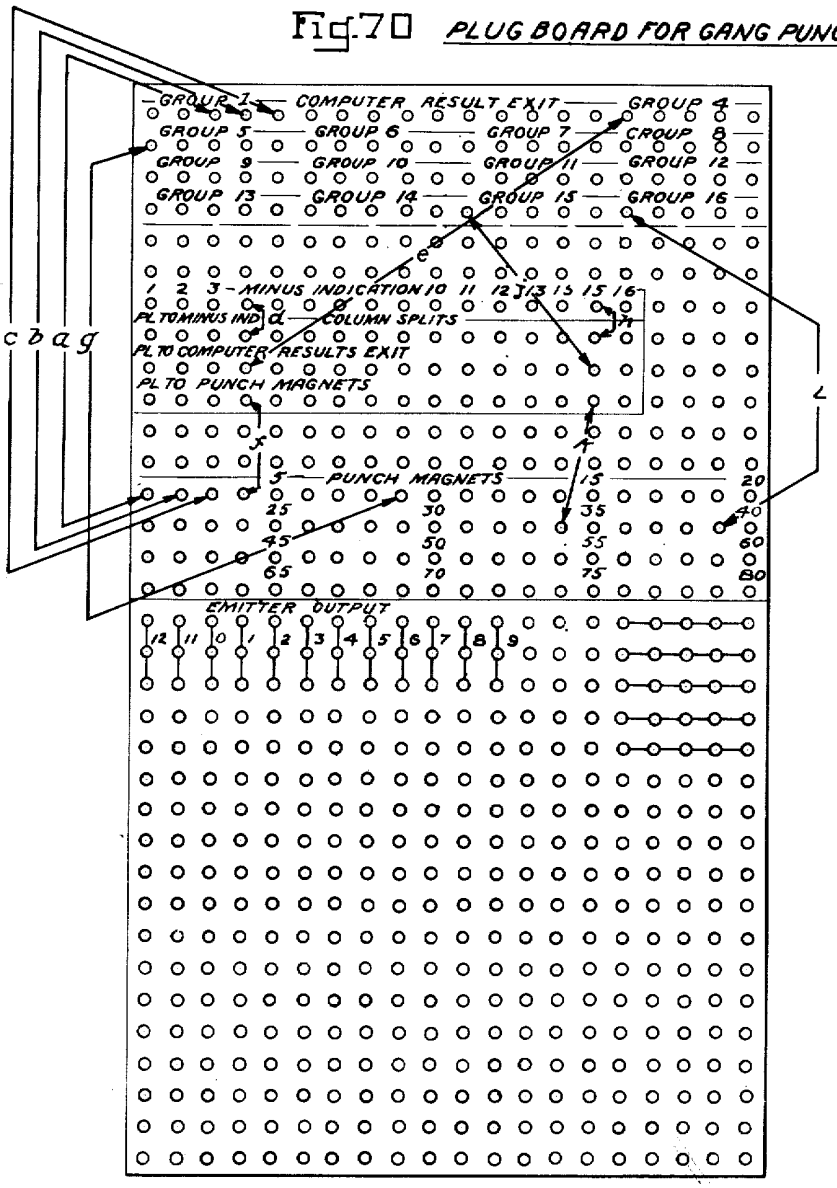
Fig. 70 PLUG BOARD FOR GANG PUNCH



PLUGBOARD WIRING FOR PRINTING IDENTIFICATION NUMBERS AND VALUES OF N_K

LINES - A, B, C: - WIRING FOR IDENTIFICATION NUMBER
LINES - d, e, f, g: - WIRING FOR FIRST AND LAST DIGITS OF N_O
LINES - h, j, k, l: - WIRING FOR FIRST AND LAST DIGIT OF N_S

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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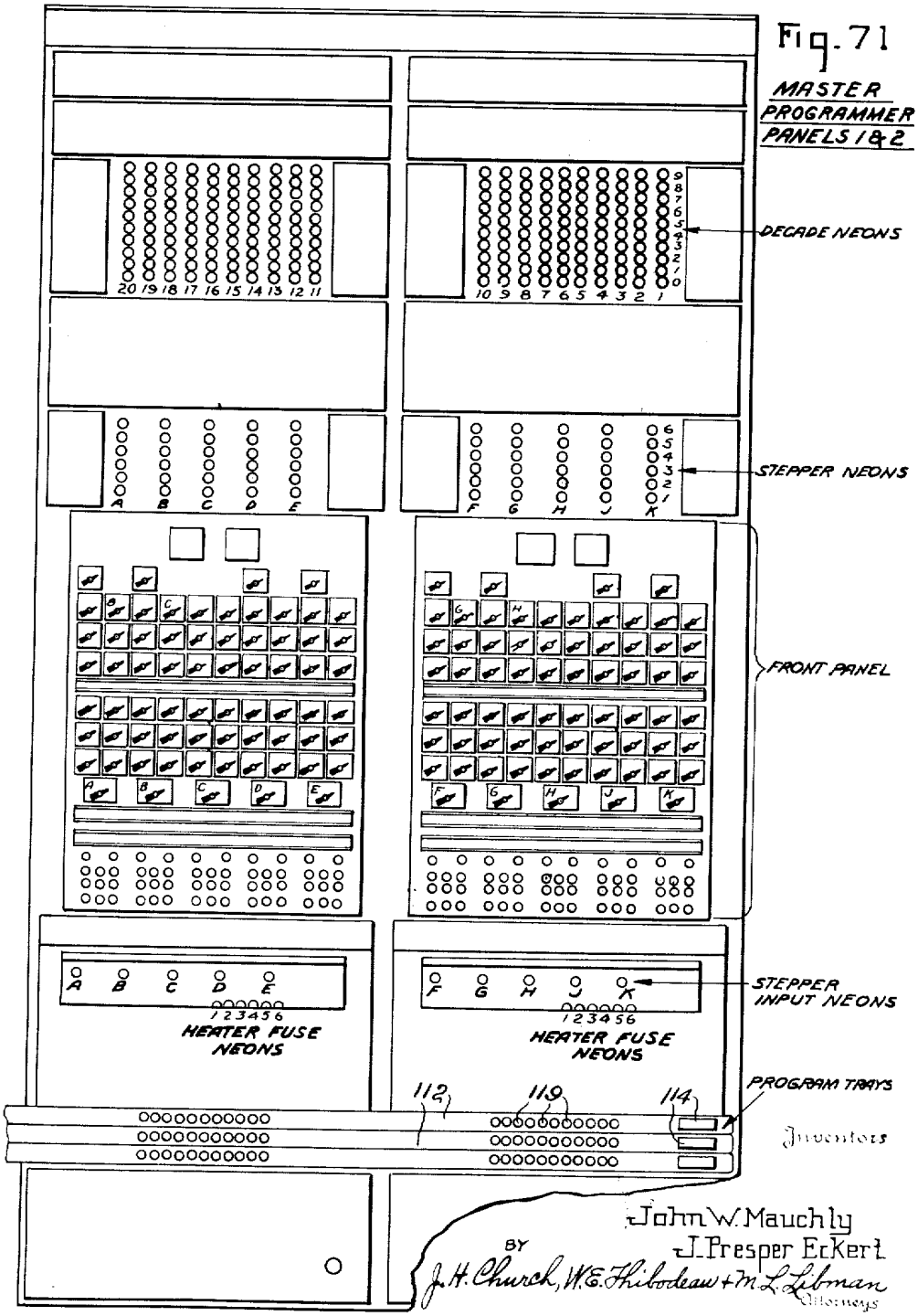
Fig. 71



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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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Fig. 72A MASTER PROGRAMMER

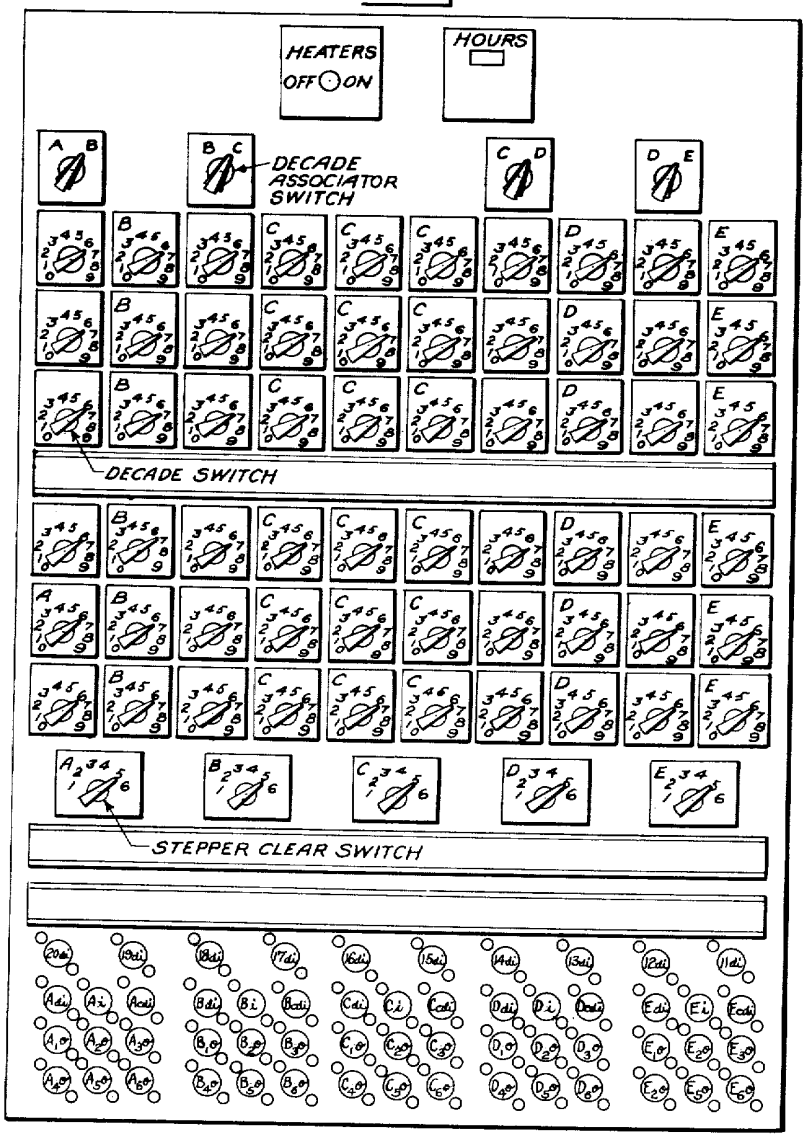

Fig. 72A | Fig. 72B

Fig. 72

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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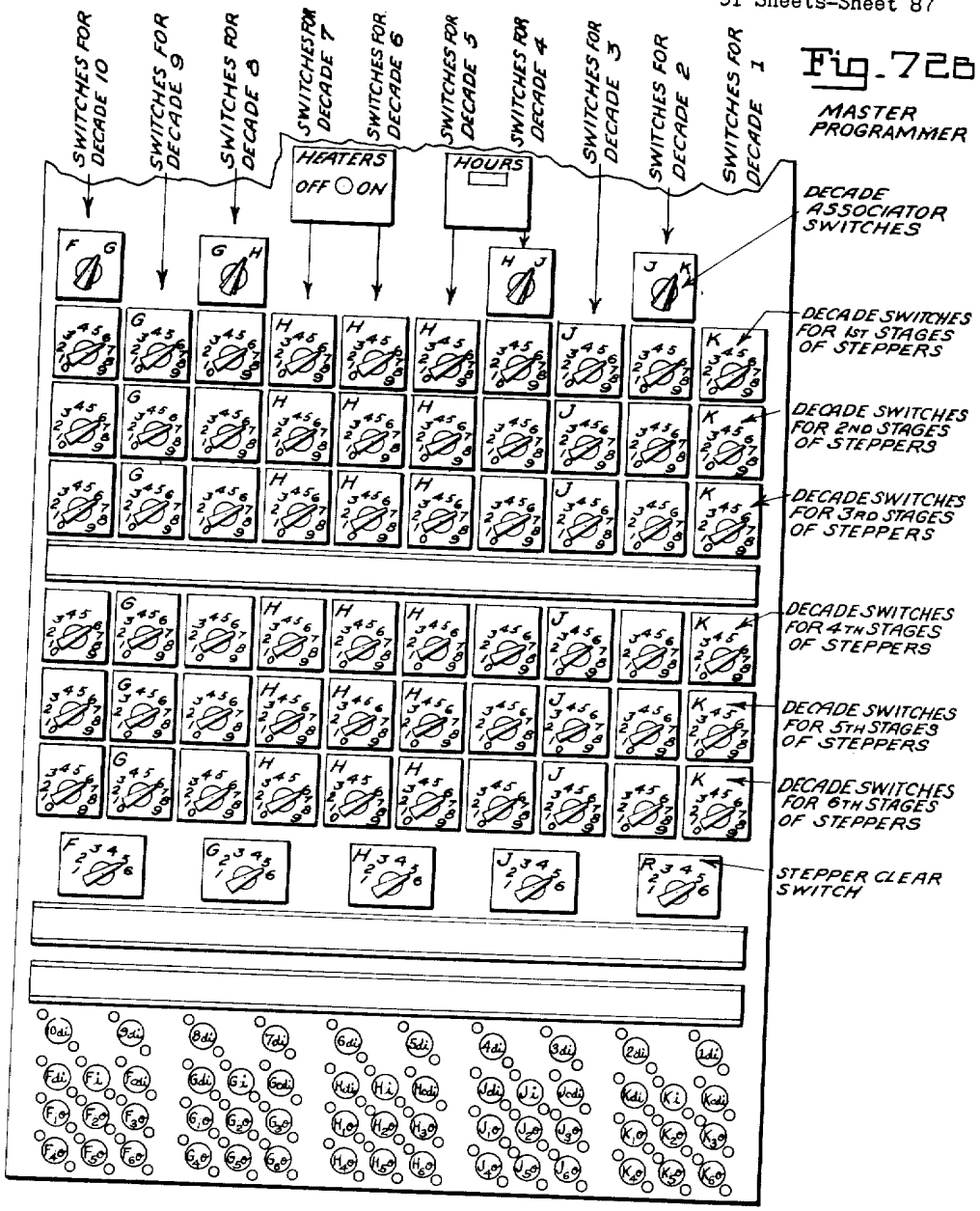
Fig. 72B



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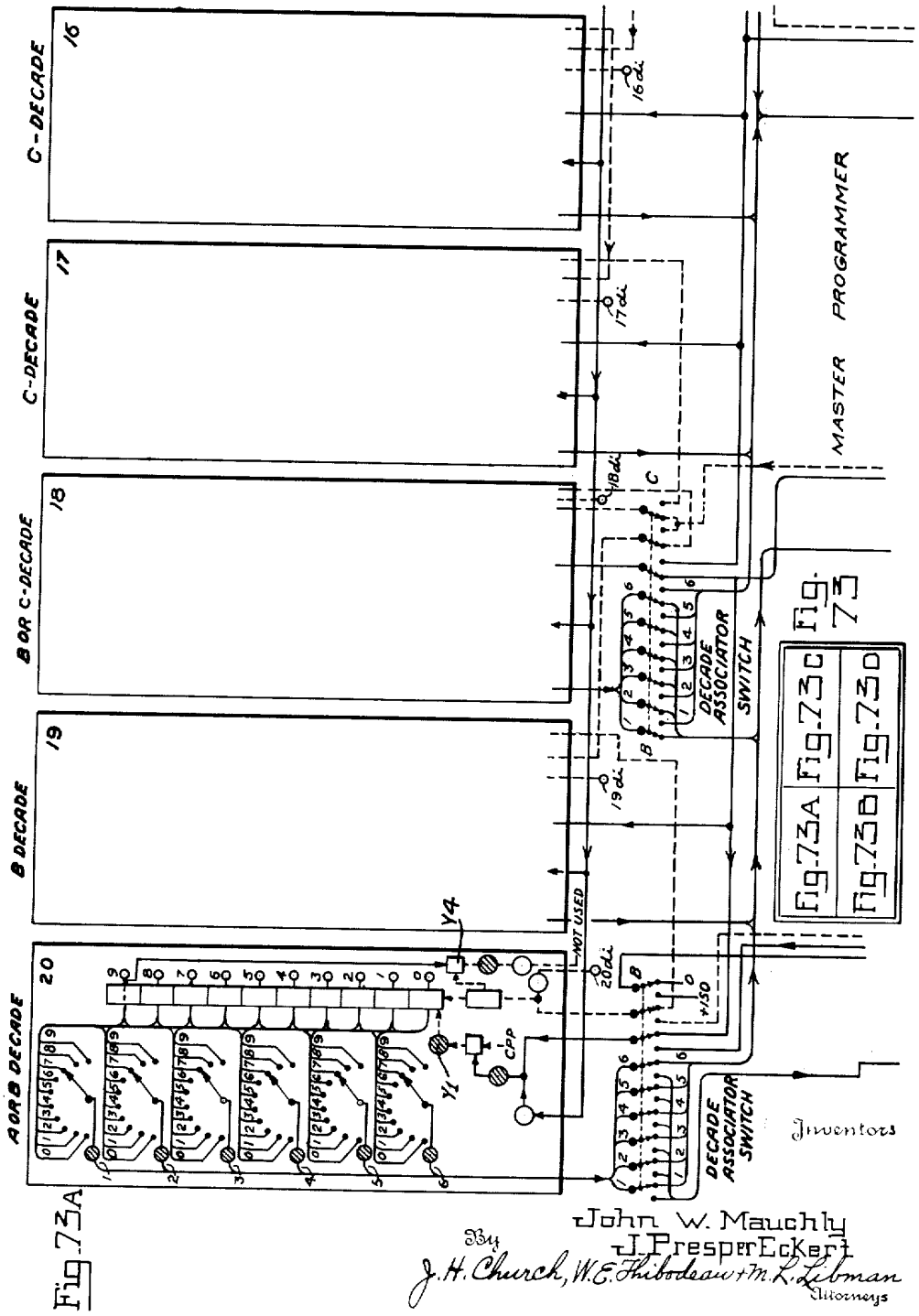

Fig. 73A

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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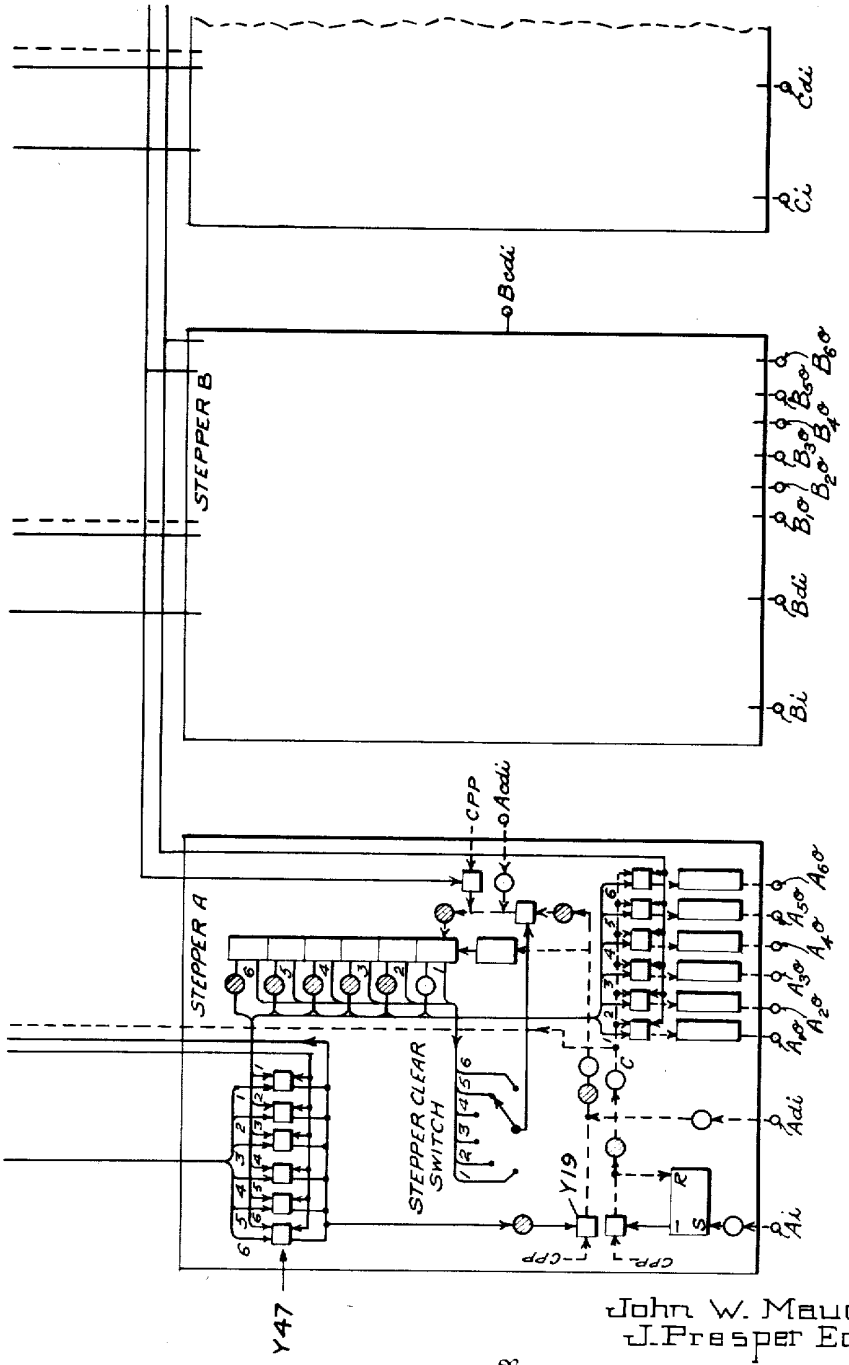

Fig. 73B MASTER PROGRAMMER

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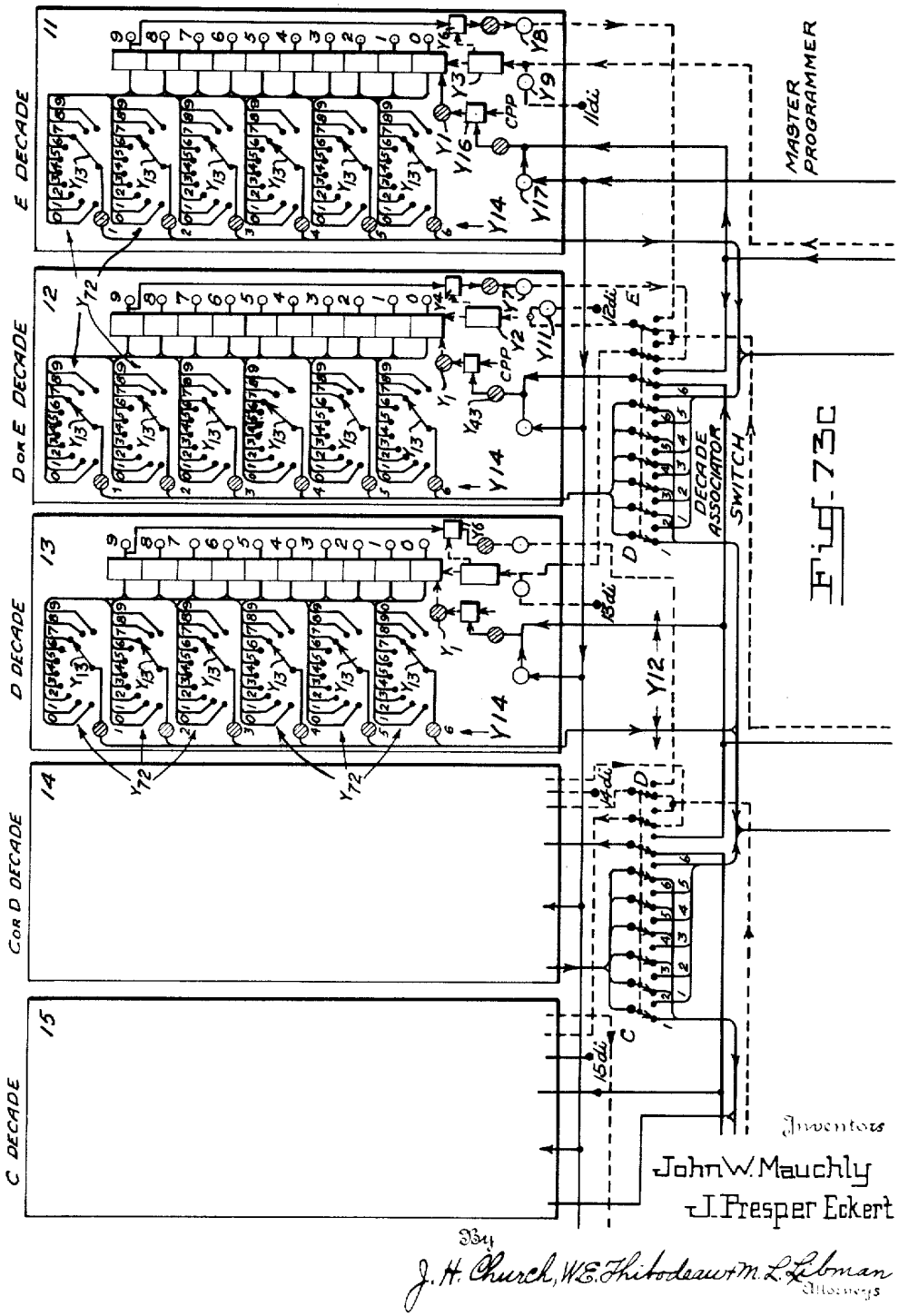

Fig. 73c

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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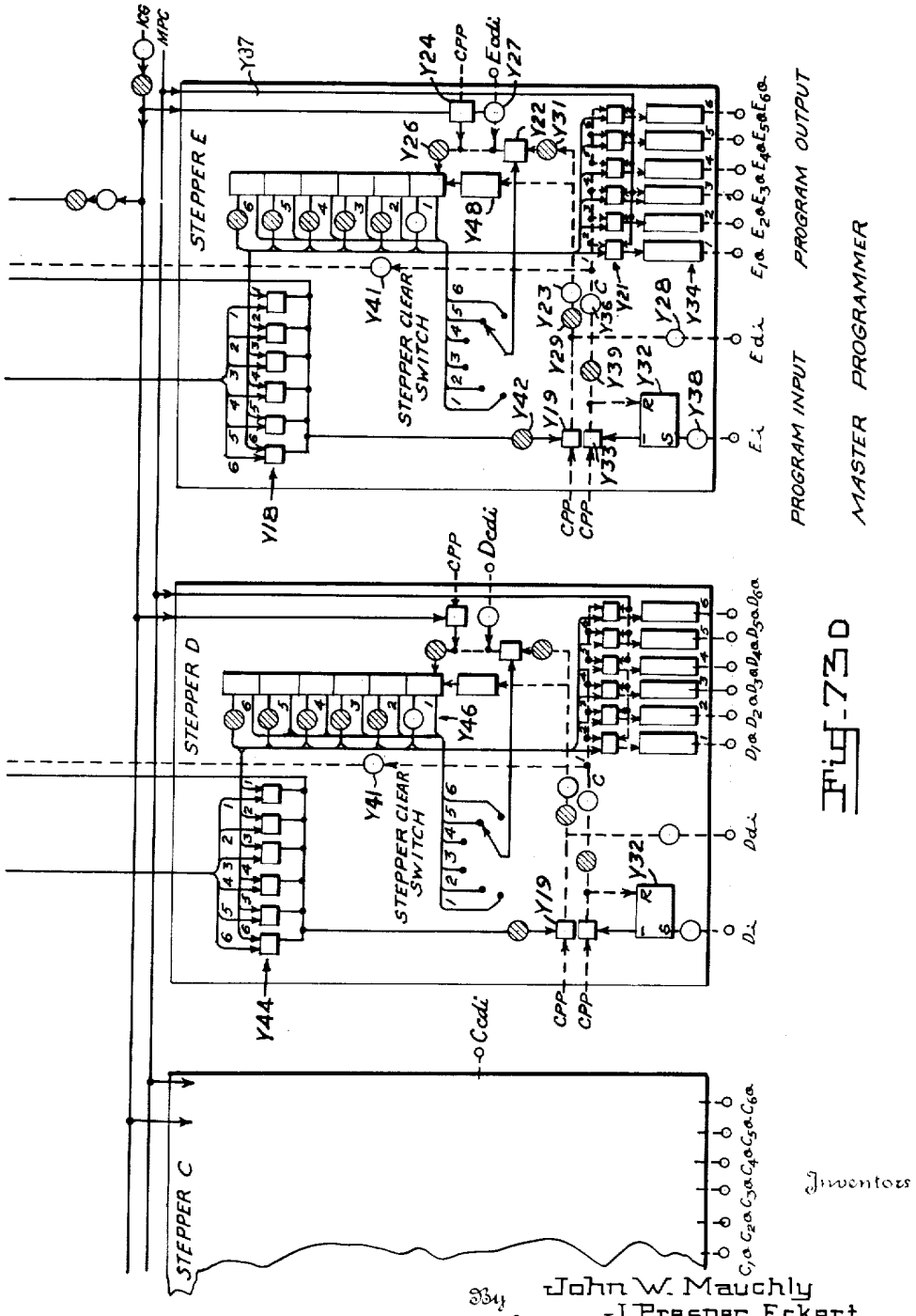

Fig. 73D

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ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

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This invention relates to methods and apparatus for performing computations involving arithmetical operations, at extremely high speeds, and with minimum use of mechanical elements, as generally so termed, and more particularly, relates to the art of electrical computing machines, with particular reference to a machine utilizing electronically produced pulses (i.e., sharp voltage changes not greater than five microseconds in duration) to represent digits and numbers, and using such pulses for control and programming operations, thus obviating the need for mechanically moving parts for these purposes. The present invention also relates to the method of using such pulses for computational purposes.

In the progress of development of computing machines from the time of the use of pebbles or grains, and the application of the abacus, to the extensive mechanical or partly mechanical and partly electrical machines of the present day, the aim has been to remove from the mind of man as much as possible of the responsibility of remembering numbers, remembering the necessary computations to be performed, remembering and writing the results of parts of computations, and how and when to use such results of such parts in complete equations, as well as to effect the necessary operations more rapidly and without physical labor.

The art and technique of aids to computation and calculation have been the subject of extensive development, extending through simple adding machines to present day complex computing machines, which include electric devices, in part in answer to the need and demand for greater speed and the elimination of moving mechanisms whose inertia sets a definite limit to the practicable speed of operation.

With the advent of everyday use of elaborate calculations, speed has become paramount to such a high degree that there is no machine on the market today capable of satisfying the full demand of modern computational methods. The most advanced machines have greatly reduced the time required for arriving at solutions to problems which might have required months or days by older procedures. This advance, however, is not adequate for many problems encountered in modern scientific work and the present invention is intended to reduce to seconds such lengthy computations.

In automatic machines the manner of controlling the storing in memory devices of the necessary numerical components and the "programming" of the pickup of these numbers and their transfer to particular operating units, as well as the special programming of peculiar internal arithmetic operations in the units, has involved a problem of foremost importance which it is here sought to advance. In such machines it is convenient to designate as "memories" those parts or elements which are so constituted as to predetermine and cause definite effects from signals transmitted to the system. External memories may consist of switches and coupling between units, arbitrarily made in accordance with the planned use of the apparatus for the solution of a given problem, and of means such as tapes or punched cards and reading machines by which numerical data (numbers pulses) and program instructions (characteristic control pulse signals) are introduced into the apparatus. Functions of the machine by which numbers are stored and control pulse signals

stored for subsequent transmission or collection from storage, as well as any automatically generated or guided to particular units, may be termed internal memories.

It is an especial aim to reduce the requirement of external memories in such machines, and to provide for the replacement thereof by internal memories, so that approach to more fully automatic operation is attained by the mere insertion of data in pulse form and the automatic generation within the machine of the necessary further data, including control pulses.

A machine has been constructed at the University of Pennsylvania which embodies our invention. This machine, hereinafter referred to as ENIAC (from the initials of its name, "Electronic Numerical Integrator and Computer") is the first general purpose automatic electronic digital computing machine known to us. Its speed considerably exceeds that of any non-electronic machine, and its accuracy is in general superior to that of any non-digital machine (such as a differential analyzer).

The ENIAC is extremely flexible, and is not fundamentally restricted to any given class of problems. However, there are problems for which its speed is limited by the input and output devices, so that it is impossible to derive the full benefit of its high computing speed in such cases. The ENIAC carries out its entire computing schedule automatically, but the sequence which it is to follow must be set up manually beforehand. The primary intended use of the ENIAC is to compute large families of solutions all based on the same program of operations, in which case the time spent in manual set-up is relatively unimportant.

It should be noted in this introductory section that it is recognized that the object of computing machine design is not merely to speed up arithmetic processes, but to attain a high overall speed, including the problem set-up and the preparation of results in useful form. It is desirable to have as much as possible done automatically.

It is also to be observed that a great deal of the equipment in non-electronic machines is "in multiple," that is, concurrent operation of many parts is used to increase computing speed. Electronic devices are inherently so fast that it is unnecessary to achieve speed in this way. By resorting to "serial operation," a considerable saving in equipment may be effected. However, the consequent loss in speed is tolerable only when electronic components having high inherent speed are employed. Reliability and maintenance are aided by this equipment reduction, and serial operation also has important advantages both from the point of view of checking and because it simplifies the work of planning the computational program.

An examination of the literature of the physical sciences shows that the principal emphasis in these fields has been in the solution of linear problems (those which can be formulated in terms of linear equations) which can be handled by analytic techniques. Physical problems other than those above mentioned are not necessarily more difficult from a physical science point of view, but they have prior to this invention been by-passed in favor of the problems whose analytic solutions are possible of attainment.

Those problems which cannot be solved analytically have been handled by computational methods or through the use of specific analogy machines. As an illustration of the computational approach we might mention the truly remarkable work of Hartree on the structure of the atom, a series of calculations extending over a period of about 15 years. An exemplification of the latter technique is found in the use of wind tunnels. At present, the supersonic wind tunnel at the Ballistic Research Laboratory, at Aberdeen, Maryland, is used about 30% of the time as

an analogy machine to solve two-dimensional steady state aerodynamical problems. Industrial companies frequently resort to highly specific analogy machines to solve, for example, linear equations of electric circuit theory or the partial differential equations which enter into electron-optics problems. It may be noted that much of present experimental work consists essentially of the solution of mathematical problems by analogy methods. If one had a computing machine of sufficient flexibility the necessity for these experiments would be obviated. Our invention makes available such a machine.

In discussing the speed of computing machines it is desirable to distinguish between so-called continuous variable and digital machines. Although existing continuous variable machines such as the differential analyzer and the A.-C. network analyzer are exceedingly rapid, the class of problems which they can solve is limited. Since both of these machines perform all operations of a computation in parallel, the size and complexity of the problems they can solve is limited by the number of arithmetic organs they contain. In addition, these machines are necessarily restricted in their accuracy due to their inherent nature. We have therefore chosen to direct our endeavors to the perfection of a digital computing machine.

The time required to carry out a multiplication provides a rather good index of the speed of a digital computing machine inasmuch as the time spent in multiplication usually represents the major part of the computing time when such machines are used. In general, the computing time for a given problem can be estimated roughly as 2 or 3 times the amount spent in multiplications. The multiplication time for the ENIAC is about 3 milliseconds. For electromechanical digital machines, the multiplication time ranges from about ½ second to 5 seconds.

To give some idea of the time consumed in carrying out an extensive computation, we may consider a typical aerodynamical problem of interest in ballistic research, which involves the solution of quasilinear hyperbolic differential equations.

I. E. Segal has formulated the partial differential equations for describing the pressure on a high-speed, sharply pointed and non-yawing projectile. The knowledge of this pressure enables one to compute the head drag, the air flow between the projectile and the head wave, and of course, the head shape of lowest drag in a given group of head shapes. If the mathematical solution of this problem is successful, it will evidently point the way to the solution of many problems now handled in wind tunnels or precision firing ranges as experimental problems. Segal's procedure above is a typical example in mathematical physics illustrating the need for high-speed computing equipment. It involves partial differential equations describing the motion of the fluid which are quasi-linear hyperbolic partial differential equations wherever the flow is supersonic, and they are solved by the introduction of characteristic parameters. The Segal formula requires interpolation in a family, of previously computed head waves to determine the flow around the given projectile head at a given Mach number. Segal estimates the number of head waves needed for this interpolation to be in order of 25.

Before the introduction of characteristic parameters the form of equations to be solved is

$$(a^2-u^2)u_y-uv(u_y+v_x)+(a^2-v^2)v_x+\frac{a^2v}{y}=0$$

$$v_x-u_y=0$$

where a is the local velocity of sound; u, v are the components of the fluid velocity at the point (x, y), and where subscripts denote the partial differentiation.

Without going into details, we can say that there are approximately 90 multiplications to be performed at each point in the field of integration, and that there will be about a thousand such points. Consequently, on the ENIAC the pure computing time, apart from reading or printing, will be about 5 minutes. Inasmuch as there will be 2000 cards printed at the rate of 100 cards per minute, the printing time is of the order of 20 minutes. It is thus seen that the total solution for Segal's problem for a given Mach number and a given head wave will be, with ideal ENIAC operation, about a half hour.

For the 25 solutions of this problem with respective head wave values, and possibly about 10 solutions for different Mach numbers the total problem will represent about 125 hours of total computing time with the ENIAC.

Contrasting this with the use of a hypothetical electromechanical machine corresponding to such as have been developed and therefore assuming a multiplication time on such a machine of about one second and a printing time of 5 characters per second, there would be spent 25 hours for the pure computing time and about 8 hours for printing, making a total computing time of about 33 hours, or a total time for the 25 solutions of about 8,000 hours. It would then be preferable to handle the problem by experimental techniques either in supersonic wind tunnels or precision firing ranges of the sort in use at the Ballistic Research Laboratory.

The question arises, why not be content with long time numerical computations? The three arguments on this point are, cost per problem, urgency for getting a solution quickly, and the scope and range of problems which could profitably be undertaken. The second point is important not only because of deadline considerations but also because the high-speed machine can be used as a tool of the physicist or engineer, much as his other laboratory equipment is used. The latter attainment of the ENIAC will allow the scientist to undertake investigations which he would otherwise not even attempt.

Objects, advantages and features of invention in the present disclosure may be understood from the foregoing and in conjunction with the detailed description and illustration hereinafter. Among the objects and advantages contemplated, some are outlined herein, although others equally important may be recognized in the embodiment of the invention or its parts disclosed and in the results and benefits attendant on practice of the invention.

A serious obstacle to the successful construction of an electronic computing machine of satisfactory accuracy and reliability has been the tendency for parasitic signals and other manifestations to develop, due to the reactances inherent in interconnection circuits, and it is an important aim of this invention to prevent such parasitic impairment of the proper response of the machine to the significant pulses for either numerical effect, or for control and timing of computative operations.

An object of the invention is to so organize an intricate and extensive system of intimately associated circuits that liability of feed-back responses or capacitative or inductive effects which would change the essential significance of the functioning of electron emission tubes in the system is eliminated.

Another difficulty which it is a purpose of the invention to overcome in a novel way, is the tendency for signals to become distorted as to potential, duration, and shape (as recorded by the oscilloscope) by interferences capacitative or inductive. In this direction a novel approach has been effected by not transmitting properly timed pulses of numerical or control significance directly through the various conductors from the initiating device directly to the one which is to respond, but instead producing a program pulse which serves only as part of the potential necessary to operate a gate or pulse former device of very definite pulse forming characteristics, the remainder of the necessary stimulating potential being derived from a constantly repeated frame of pulses having a definite order. This frame has a duration called an addition time, which is a multiple of a pulse time, that is, the interval from the beginning of one pulse to the beginning of the next pulse.

As a consequence of the foregoing, in our invention at each introduction of data to an arithmetic unit, an original shaping of the pulse received by that unit is effected by the unit itself.

It is an important aim of the invention to devise a novel means of preserving the definite and highly effective form of signal information transmitted to or through the various parts of the system and which will have standard pulse forms and potentials at all stages of operations and registering caused by such pulses.

In a related sense it is an aim to offer a novel means by which the foregoing may be attained by maintaining at all operating units a frame of pulses occurring in timed sequence related to an overall time beat, so that at each unit a series of pulses is available in fully effective form for numerical entries, and for control functions, and by which, when such pulses are properly selected and made effective, several units may be caused to function together with exactitude.

In the same connection it is a purpose to enable the transmission of signals of both numerical significance and control significance in such manner that they become adequately effective at selected units to cause reception of predetermined pulses of the said frame of pulses with the desired numerical or control significance, whereby the initial signal is not required to maintain a high effectiveness as to form and potential by transmission past the functioning apparatus.

An important desideratum in the invention is the production by means of a simple constantly operating oscillator circuit of clock pulses having the basic frequency determined for effective operation of the various electronic elements of the machine, and to derive in a novel way from each of an arbitrary recurrent number or cycle of such clock pulses, a variety of pulses in a plurality of circuits in a coordinated relation so that some of the pulses so derived will control the utilization of other pulses derived in the same or other cycles and other sources, for arithmetic functioning of units of the machine. In the same direction it is sought to reduce to a minimum the number of the clock pulses required in such cycle, so that a number of numerical signals and control signals greatly exceeding the number of pulses in such a cycle, but all occurring in the same cycle as the clock pulses with which they are associated, may be produced.

Among the objects of the invention either additional or contributory to the foregoing, are the following:

(*a*) To enable the performance of mathematical equivalents of differential equations by mathematical representations of the variables by discrete numbers, with such certainty that the introduction of the same data at different times will give the identical numerical result, as distinct from such machines as the differential analyzer.

(*b*) In the control of the arithmetical functions of the machine, to eliminate the repeating routines of instructions in external memory material.

(*c*) Further, where sub-routines of arithmetical procedure are required, it is a purpose to cause automatic origination of sub-routine controls and selection of these as an internal function of the machine, so that the material required to be prepared as external data to be fed into the machine is further minimized.

(*d*) To organize the elements of the machine so as to eliminate functions of such nature that they might be materially affected by variations of operating conditions such as often occur. The machine is thus adapted to practically infallible operation under varying conditions which extensive experience has shown may be expected to be manifest in such machines over a reasonable period of operation.

For instance, it is an attainment of the invention that electron emission high vacuum tubes such as common triodes or pentodes, used in radio receivers, are made use of as switching devices in such manner that their operation occurs in a condition far from the critical point between

conduction and non-conduction, and so that deterioration in the tube elements or the state of the space therein over a period of months, will not materially affect the response of the tube to control potentials applied to the grids as pulses or potentials of substantial values.

It is a related aim to use such tubes as switches or other kinetic equivalents in such manner that their function will be either conducting or non-conducting, accompanying this by use of the tubes at or close to saturation for their conducting state, and with a grid bias well below the critical point for their non-conducting state. This also permits use of tubes of high $m\mu$ and low capacitance in order to establish great certainty of operation and response generally. In this way aggregated reactances between trunk lines and other conductors and between electrodes of the tubes are not sufficient to distort transmitted signals materially or to set up parasitic pulses of sufficient degree to cause malfunction.

Associated with, and as a part of this relation of circuits and the objects in view, the potentials of circuits having mutually adjacent conductors or other relation in which relatively high reactance values are unavoidable, have been so organized in relation to their greatest possible reactances, their potential levels so fixed relatively to such liabilities and the operating pulses produced at potential levels so antagonistic to such liabilities, that impairment of signal pulses, or production of equivalent or intervening parasitic pulses, will be inconsequential.

A further aim is to present a novel means of determining the selection of predetermined pulses forming part of an arbitrary arrangement or frame of pulses being automatically transmitted in trunk conductors, by the timing of energization of plural grid tubes, so that a control pulse of long or short duration may be utilized to partially establish the necessary grid potential for changing the stable state of a tube having an adequate B potential for initiating a desired pulse on such change, and another pulse either for control or with numerical significance, forming part of a frame of pulses which are being manifest on another grid of such tube at the same time, will cause it to transmit to an appropriate conductor a pulse of a desired characteristic and significance with functional value effective at a unit conditioned to receive it.

In the attainment of functions necessary in an electronic system, by which arithmetically significant results may be produced, it is a salient object of the invention to enable the use of standard high vacuum electron radio tubes.

It is also an important aim of the invention to enable the use of such tubes for producing control actions in the system by which various parts may be caused to receive electrical impulses of numerical significance and hold a corresponding condition such that they may cooperate with other units to integrate two or more such storage equivalents of sums or digits, or to produce control responses by which the intercommunication of units may be effected as required, as well as effecting the clearing of the units of conditions representing stored numbers of controls.

While electronic ring counters have been evolved utilizing such tubes in relations known as trigger circuits and flip-flops, and the present invention utilizes an adaptation of a flip-flop ring to its use where the reception and counting of pulses of numerical significance is desired, it is a special aim of the invention to evolve novel means by which such ring counters are embodied so as to operate with great certainty and effectivenes, and to organize such counters in a correlated system whereby novel arithmetical computations are attained not heretofore conceived or possible with available apparatus.

In ring counters of the familiar prior art an output from the counter numerically significant of its stage of operation at a given time has heretofore only been obtained by operating the counter in such manner that the number value

contained is erased. The present invention seeks to enable the repetition of such output successively at basic times intervals, or to repeat the output at irregular intervals, while preserving the information in the storing element until required or purposely erased or "cleared."

It is further sought to present a novel means to take from a matrix such as a punched card a record significant of numbers and instructions, by mechanical means, and to establish a set-up significant of such numbers and instructions in such manner that pulse equivalents of these numbers and instructions will automatically by made effective electronically and transmitted through the system in the desired order required for arithmetical procedures in units properly responsive thereto.

It is a highly important purpose of the invention to provide a novel electronic means for carrying out the arithmetical process of multiplication very rapidly and to devise a novel system whereby the product may be secured through an automatic electronic operation of the system.

To this end it is sought to evolve a novel circuit system and associated tube organization whereby there may be effected the equivalent of the necessary off-set or shift of the product of the multiplicand by a digit of the multiplier in relation to the product of the same multiplicand by another digit of the same multiplier.

Another object related to the multiplication procedure in the system is to construct and coordinate a resistance grid system in which signals applied to the cross elements of one direction in the grid system may cause potentials on intersecting transverse members to select pulses to be transmitted to the counters of an accumulator in the necessary decades to effect the desired result.

An object subordinate to the last mentioned is to devise a novel and effective means for transmitting to the shifter device pulses significant of a treatment of input to the multiplier corresponding to the multiplication of one number by another.

Another important aim is to construct a novel organization of the multiplier grid work of conductors and resistance couplings at significant intersections with input electronic valves and pulse supplying means and output electronic valves in controlled relation to conductors signals by which the second named valves are energized by coincidence results to transmit pulses significant of results of factors represented in the input.

A purpose related to the last named object is to so organize the grid work and valve devices in the form of radio tubes that feedback and cross couplings are obviated and so as to avoid sufficient partial or complete diverted transmissions of pulses to set up or initiate output effects other than the numerical product or result equivalents corresponding to the computational procedure of multiplication.

It is an important aim of the invention to simplify the apparatus required in securing interaction between two or more computing or arithmetic units, by utilizing a novel coordination of an arbitrary clock frame work of pulses effective in all units alike and recurrent either at fixed intervals automatically, or at will and requiring only a small number of selectively transmitted pulses, so that the requirement of interlock coupling of circuits is eliminated to a large degree, and the amount of apparatus greatly minimized.

It is an important aim of the invention to enable the utilization in a novel way of a cyclically repeated frame of pulses of uniform interval in the cycle to effect the communication to the storing and computing units of the machine of pulses of numerical significance, either plus or minus, and all necessary operating pulses by which the various adding, multiplying, dividing, subtracting, and square rooting operations of the system are carried out.

A further object related to the foregoing is to establish a number of categories of control and numerically significant pulses with standard pulse times within the predetermined cycle, but wherein the number of control and

numerically significant pulses included in such categories greatly exceed the number of pulse times included within the cycle.

A related object is to enable the derivation from a frame of successive pulses cyclically repeated and communicated to parts of each unit in the machine, of numerically significant pulses communicated on one or more of a plurality of channels to units conditioned and intended to receive such data and/or to function computatively therewith and with other data previously or subsequently transmitted.

An important aim of the invention contributing to its succesful operation with a minimum of impairment or malfunction mathematically, is to effect intercommunication between units having pulse-responsive circuits which are maintained at widely different potentials for their normal conditions, by the communication of pulses from one such unit to another such unit without mutual disturbance of their normal potentials, yet in a most definite manner taking full advantage of the before mentioned operations of tubes well below or above cut off, or well above minimum conductance conditions (that is close to the saturation state of conductance).

A specific obect of the inventjion is to present a novel organization of electron valve tubes and circuits for communicating control signals and effecting the transmission of complements of nine. A related purpose is to enable the derivation of both decimal digits and/or their complements from the same clock pulses, in a novel and simple manner.

It is also sought to fix the value of transmitted number data as plus or minus, by novel means, which will be effective both in the functioning of computing units of the machine, and in the optically observable condition of the units.

A novel attainment of the invention is a means for the derivation of the complement of ten of a number. This means is further distinguished by functioning in such manner that the transmitted complement is obtained by transmission originally of the principal number itself, and a derivation of the complement by an automatic internal routine of the machine.

A further object is to provide a novel means of communicating pulses of positive potential from one circuit to another with a high rise and good form. That is to say, in usual methods of producing positive pulses with vacuum tubes it has been difficult to produce a pulse of a rise of fifty volts or more which can be limited to approximately two microseconds in duration and which will have a sharp rise and sharp fall at termination. In accomplishing this it is an object to utilize a vacuum tube in a novel way for the production of pulses by deriving the pulse from the cathode in an efficient manner.

Another important object of the invention is to provide a novel automatic means for producing the quotient of two digital quantities represented by electric pulses in terms of a digital quantity also represented by electric pulses. A subsidiary object to the above is to provide an electronic digital divider capable of handling digital quantities of either positive or negative sign, with the correct sign in the quotient.

Another object is to provide automatic means for electronically evaluating the square root of a digitally represented quantity.

An important feature of the invention is the provision of an electrical function table capable of storing digital values in tabular form for transmission to the computer at electronic speeds. An object subsidiary to the above is to provide, in such a function table, means for automatically transmitting at electronic speeds not only the value of the function corresponding to a given argument, but also a sequence of function values bracketing the one corresponding to the argument, for use in interpolation or any other desired mathematical purpose.

Another object is to provide means enabling the automatic transfer to the computer at electronic speeds of any

one of a number of digital values stored in an external memory or recording device, in any desired predetermined sequence.

Another object is to provide means for automatically repeating any operation of the computer at electronic speeds for any exact predetermined number of times.

A particularly important object is the provision of means and method enabling the automatic choice by the computer, at electronic speeds, of any one of a plurality of possible computational operations in response to the value of the result of a previous computational operation, in accordance with a predetermined standard of selection.

Another object is to enable the transfer of a digital number from a static mechanical representation thereof by the positional arrangement of switching elements, such as switches or relays, into a dynamic electronic representation thereof by means of coded and suitably channeled electrical pulses of extremely short duration, at electronic speeds.

ADVANTAGES OF ELECTRONIC DIGITAL MACHINES

A digital machine has more *flexibility* and *accuracy* than is possible or practical in a continuous variable machine. A digital machine which is electronic can also have a very decided *speed* advantage over one which is non-electronic. The evidence of many months' operation is that electronic digital machines can be made at least as reliable as any others.

Flexibility and accuracy also are important economic considerations in this invention. With specialized machines, specific problems may be solved rapidly, but time may be lost when new problems require either a new machine or the modification of an old one. Further, even if time is no object, the cost of a group of specialized devices can easily total more than the cost of one flexible all-purpose machine.

Accuracy

The accuracy obtainable with continuous variable machines depends upon the accuracy with which the component parts are constructed. However, exactly the same statement may be made about a digital machine. The essential difference is in the kind of dependence which holds in each case. In a digital machine, minor inaccuracies of components can be made to have no effect at all upon the accuracy of the computation. In continuous variable machines, there is a continuous (though not necessarily simple) relationship between the accuracy of the parts and the accuracy of the results (before translation into digital form). Increased computational accuracy can be attained only by increased precision of the parts. Not only are there practical limits to the precision with which the parts can be manufactured, but the maintenance of such precision during subsequent operation is extremely difficult. For instance, mechanical parts will lose precision through wear. On the other hand, digital machines require only that the accuracy of parts be kept within certain tolerances, and the tolerance band can be made very wide. The accuracy of a digital machine is then limited only by the amount of equipment which can be used in it. This limitation is more often an economic one than a physical one.

Flexibility

Analogy computing devices vary greatly in flexibility. Scale models and fixed electrical networks which are completely specialized represent an extreme which is of no interest here. Large network analyzers and differential analyzers are usually considered typical examples of highly flexible analogy devices. Nevertheless, these machines are somewhat specialized and restricted in application.

A digital machine which can be directed to carry out any of the common arithmetic operations in any desired sequence on any given set of numbers has all the generality and flexibility required for any practical purpose. (It cannot compute the "exact" value of pi, but it can compute in a finite number of steps any desired approximation of pi.) Therefore, it can, for example, compute to any specified definite approximation the solutions of nonlinear partial differential equations which are not obtainable from any existing analogy computer. This attainment is one of the important objects of our invention.

Digital Computing Speed and Cost

The preceding sections have indicated that advantages of accuracy and flexibility recommend digital rather than continuous variable computing devices. Even moderately large problems which are within the range of existing analogy machines require an enormous number of arithmetic operations when handled by digital machines. The cost of digital computing must be low if such calculations are to be undertaken.

Only very rough comparisons need to be made to demonstrate that digital computation by electronic devices should be a great deal faster than by the electro-mechanical devices used in existing large computers. Typical electro-mechanical devices are relays and electrically controlled counter wheels. Five or ten milliseconds is about the operating time for reliable high speed relays. Analogous operation of a vacuum tube can take place in 0.5 to 1 microsecond. The electronic device is therefore capable of operating about 10,000 times faster. (It may be observed that faster tube circuits can be developed.)

A vacuum tube and its associated circuit components costs approximately the same amount as a relay. This indicates that generally for a given cost the ENIAC gains time by a factor of 10,000, when compared to the non-electronic electromechanical digital computor.

For various reasons, the actual factor for the ENIAC is something like 100, and for our future electronic machines will probably be more nearly 1000. Since moderately large computing problems are already being done by digital electromechanical devices, it seems clear that the ENIAC will find much more extensive application than practicable with the electromechanical machine.

I. INTRODUCTION

Because of the complexity of the following description, frequent cross-referencing is necessary. In order to simplify this as well as the problem of looking up specific parts of the computer, the description has been organized into numbered chapters and sub-chapters, as is common in technical reports. To assist in locating any specific item, the following pages first present a "Table of Contents," which serves also to show the organization of the material at a glance.

TABLE OF CONTENTS

BRIEF DESCRIPTIONS OF THE FIGURES

FIG. 1 is a floor plan of the ENIAC as installed for use.

FIG. 2 is a diagram showing one cycle or frame of pulses as recurrently delivered into the ENIAC by the cycling unit.

FIG. 3 is a circuit diagram of one example of the flip-flop used in the ENIAC; the symbol adopted to represent such an element in the block diagrams herein being shown at the left.

FIG. 4 is the circuit of a binary ring used in a number of places in the ENIAC, its block symbol at the left.

FIG. 5 is the basic circuit of the decade ring counters, and stepper rings, its block symbol at the left. The number of stages of the ring are indicated by the number of segments in the symbol.

FIG. 6 illustrates a typical gate tube hook-up (used as a switch throughout the ENIAC) and its block symbol.

FIG. 7 shows a triple coincidence tube circuit which is used as an interlock switch, its block symbol shown at the left.

FIG. 8 similarly illustrates a multiple coincidence switch tube circuit and its block symbol.

FIG. 9 is a detail of a buffer tube with typical parameters, and its block symbol.

FIG. 10 is a similar showing of an inverter and its symbol.

FIG. 11 is a circuit detail of a tube used to deliver positive pulses of highly effective form and potential, termed the cathode follower; its symbol being indicated at the left.

FIG. 12 shows a pulse standardizer circuit used numerously in the ENIAC, and its symbol in the block diagrams.

FIG. 13 is the circuit detail of a special pulse standardizer used in the ENIAC to derive a pulse from a mechanically operated switch.

FIG. 14 is a diagram of a transmitter circuit, with its block diagram symbol.

FIG. 15 is a block diagram showing in elementary form the basic principle of operation of an accumulator capable of adding only.

FIG. 15–A is a block diagram illustrating the elementary principles of the cycling unit for producing the cycle of pulses shown in FIG. 2.

FIG. 16 is a schematic plan showing the mutual relation of FIGS. 16–A and 16–B—an elementary adder capable of subtractive addition.

FIGS. 16–A and 16–B together constitute a block diagram similar to FIG. 15, but including means for performing subtractions, and providing for one-addition-time operation.

FIG. 17 is a block diagram showing in elementary form the basic principle of operation of the multiplier unit of the ENIAC.

FIG. 18 is a block diagram showing in elementary form the basic principle of operation of the divider unit of the ENIAC, and serving to also illustrate the interrelationship of the accumulators and the principal computing units.

FIG. 19 is a similar showing of the elementary principle of operation of division of signed quantities in the ENIAC.

FIG. 20 is a diagram showing a procedure of interpolation of values.

FIG. 21 is a plan of the mutual relation of FIGS. 21–A and 21–B—the elementary function table.

FIGS. 21–A and 21–B constitute a block diagram illustrating an elementary function table.

FIG. 22 is a schematic diagram of a hook up for performing linear interpolations.

FIG. 23 is a front elevation of the initiating unit.

FIG. 24 is a detail of the controls on the panel of the initiating unit.

FIG. 25 is a plan of the mutual relation of FIGS. 25–A and 25–B, illustrating the cycling unit and initiating unit.

FIGS. 25–A and 25–B constitute a block diagram of the initiating unit.

FIG. 26 is a block diagram of the power system.

FIG. 27 is an elevation of the front of the cycling unit panel.

FIG. 28 is an enlarged view of a portion of the front of the cycling unit panel.

FIG. 29 is a plan showing the mutual arrangement of FIGS. 29–A and 29–B.

FIGS. 29–A and 29–B together are a block diagram of the cycling unit and initiating unit.

FIG. 30 is a chart showing the timing of certain pulses.

FIG. 31 is a front view of an accumulator panel.

FIGS. 31–A and 31–B are top and front views, respectively, of a Program Tray.

FIGS. 31–C and 31–D are similar views of a Digit Tray.

FIG. 31–E is a cross section of one of the trays.

FIG. 31–F is an elevation of a plug-in unit, with a middle portion omitted, and the wiring omitted.

FIG. 31–G is a front view of the last mentioned plug-in unit.

FIG. 32 is an enlarged view of a portion of an accumulator panel, showing switches and other details.

FIGURES 32–A illustrates the accumulator jumper connections for ten place operation.

FIGURE 32–B illustrates the accumulator jumper combinations for twenty place operation.

FIGURE 32–C explains the accumulator control switch legend.

FIG. 33 is a plan showing the mutual arrangement of FIGS. 33–A, 33–B and 33–C, relating to the accumulator.

FIGS. 33–A, 33–B and 33–C constitute a block diagram of an accumulator.

FIG. 34 is a circuit diagram of a transceiver with its block diagram symbol.

FIG. 35 is a circuit diagram of a received with its block diagram symbol.

FIG. 36 is a plan showing the mutual relation of FIGS. 36–A and 36–B of the decade plug-in unit.

FIGS. 36–A and 36–B together constitute a diagram of the circuits of a decade plug-in unit.

FIGS. 36–C and 36–D together constitute a circuit diagram of the principal features of a gate unit for the accumulator.

FIG. 36–E is a circuit diagram of a repeater circuit.

FIG. 37 is a schematic diagram showing certain uses to which dummy programs may be alternatively put, in the accumulators.

FIG. 38 is a front view of the panels of the high speed multiplier.

FIGS. 39, 40 and 41 are enlarged views of portion of the respective panels of FIG. 38, showing switches and other details.

FIG. 42 is a plan showing the mutual arrangement of FIGS. 42–A to 42–D, inclusive. FIGS. 42–A and 42–D, inclusive, constitute a block diagram of the high speed multiplier.

FIG. 43 is a plan showing the interconnection of the multiplier and associated accumulators.

FIGURE 43–A illustrates the multiplier input members and a portion of the multiplier per se.

FIGURE 43–B illustrates the balance of the multiplier per se and the output accumulators.

FIG. 44 is a front view of the divider-Square Rooter panel.

FIG. 45 is an enlarged view of a portion of the divider-square rooter panel showing switches and other details.

FIG. 46 is a plan showing the mutual arrangement of FIGS. 46–A to 46–F, inclusive.

FIGS. 46–A to 46–F, inclusive, constitute a block diagram of the divider-square rooter.

FIG. 47 is a plan showing the mutual arrangement of FIGS. 47–A and 47–B. FIGS. 47–A and 47–B show the interconnection of the divider-square rooter and associated accumulators.

FIG. 47–C shows the semi-permanent connections to be made between the divider square rooter and its associated accumulators.

FIG. 48 is a plan showing the mutual arrangement of 48–A to 48–D, inclusive. FIGS. 48–A and 48–D, inclusive, constitute a block diagram of the function table.

FIG. 49 is a front view of the function table panels.

FIGS. 50 and 51 are enlarged views of a portion of the respective panels shown in FIG. 49, showing switches and other details.

FIG. 52 is a front view showing details of portable function table switch arrangement.

FIG. 53 is a chart illustrating the use of the function table to store program information.

FIG. 54 is a plan showing the mutual arrangement of FIGS. 54–A to 54–C, inclusive. FIGS. 54–A and 54–B, inclusive, constitute a cross section of constant transmitter circuit details.

FIG. 55 is a plan showing the mutual arrangement of FIGS. 55–A to 55–D, inclusive. FIGS. 55–A to 55–D, inclusive, constitute a block diagram of the constant transmitter.

FIGURE 56 is a plan showing the mutual arrangement of FIGURES 56–A and 56–B.

FIGS. 56–A and 56–B constitute a cross section schematic view of the constant transmitter and reader.

FIG. 57 is a plan showing the mutual arrangement of FIGS. 57–A to 57–C, inclusive, FIGS. 57–A to 57–C, inclusive, constitute a block diagram of the card reader.

FIGS. 58, 59 and 60 are enlarged views of a portion of the constant transmitter panel showing switches and other details.

FIGS. 61, 62, and 63 are enlarged views of panels numbers 1, 2, and 3, respectively of the printer showing switches and other details.

FIG. 64 is a front view of the constant transmiter panels.

FIG. 65 is a chart showing the card reader cam template.

FIG. 66 is a plan showing the mutual arrangement of FIGURES 66–A to 66–C which constitute a diagram of the card punch circuits.

FIG. 67 is a plan of the mutual relation of FIGS. 67–A and 67–B.

FIGS. 67–A and 67–B together constitute a block diagram of the printer.

FIG. 68 is a plan for the juxtaposition of FIGS. 68–A and 68–B.

FIGS. 68–A and 68–B together constitute a schematic diagram of printer circuits.

FIG. 69 is a time table of the actions of the printer cams.

FIG. 70 is a plan of the setting of the plug board connections for the printer gang punch.

FIG. 71 is an elevation of the master programmer panels 1 and 2.

FIG. 72 is a plan for the mutual arrangement of FIGS. 72–A and 72–B.

FIGS. 72–A and 72–B together constitute an enlargement of the control parts of the master programmer panels numbers 1 and 2.

FIG. 73 is a plan for the relative arrangement of FIGS. 73–A to 73–D.

FIGS. 73–A, 73–B, 73–C and 73–D, together, constitute a block diagram of the master programmer.

FIG. 4 is a schematic circuit diagram and a chart showing the maner of interconnection of deleters.

FIG. 75 is a schematic diagram showing interconnections of shifters.

1.1. *General Description of the ENIAC*

1.1.1. *Classification of Elements of ENIAC*

In order to describe such digital computing machines as the ENIAC, it is desirable to set up a classification into which the different elements of the machine may be placed.

We divide the various units of the ENIAC into three basic classes—arithmetic elements, memory elements, and control elements. The arithmetic elements of the computing machine are those which form the basic operations of arithmetic—addition, subtraction, multiplication, division, and square rooting. There should be added to this list another operation which we classify as being arithmetic. This is "magnitude discrimination" or simply "comparison." In this operation in the ENIAC we obtain a result which is dependent upon which of two numbers is the larger. This operation is essential in any automatic computing machine and is used to make decisions between alternative possibilities which exist in many problems.

The memory elements of the machine may be divided into two groups—the "internal memory" and the "external memory." The internal memory includes all memory devices within the machine and is thus finite, while the external memory exists outside of the machine in such a form as punched cards or perforated tape. This memory may be increased indefinitely but has the limitation that it must be associated with the machine by an input and output mechanism which is usually comparatively slow.

It is convenient to divide the internal memory into three classes—first, memory for numerical data which can be altered by the operation of the machine (usually rapidly), second, memory for numerical data such as empirical data which are known before the machine is started and may, therefore, be introduced into the memory slowly, but must be withdrawn rapidly during the computing of the problem; and third, there must be a memory for instructions—those manifestations which cause transfer between the various memory and arithmetic units and cause the arithmetic units to do the various operations on the numbers. This form of memory, like the second class, may be set up slowly since the necessary information is available before the computation is started and likewise, it must produce its effect rapidly since it must control the operation at all points of the computation.

1.1.2. *Layout of the ENIAC and Description of Panels*

For convenience and economy in production of the machine, it is made up principally of a multiplicity of so-called panels, which are cases in which the tube and circuit assemblies are mounted on numerous removable chassis. For clarity in this description, parts of the apparatus having distinctive computative functions will be termed units, although there are unit assemblies of various kinds in each, and also, as will appear, certain of the units may comprise a single panel element, while others comprise two or more panels. The panels are all of similar size and somewhat similar appearance generally at the front side, but, while nearly all of them include ring counter devices, and other similar features, they are variously organized and have added features appropriate to their individual functions.

As shown in FIGURE 1 the machine is set up in a series of forty vertical planiform panels of uniform height (approximately 10 feet), and width approximately 2 feet, a large number of which are simple pulse receiving and emitting "accumulators," as registers or holders of significant numerical or control values, and others of which are in addition, arithmetical elements of special computing functions some including printer controlling elements; so as to present, in conjunction with function tables and "programmers" a machine capable of performing all necessary computative functions. All of the panels have elements capable of receiving, responding to, and transmitting pulses for control purposes, or for arithmetical use.

The panels are of heavy sheet metal and angle steel construction arranged in an aligned series side by side having a ground plan generally U-shaped, extending around three sides of a large room approximately 30 by 50 feet. The sides of the panels facing inwardly are considered the fronts of the panels and have provision for determining certain functions of the circuits therein and for effecting interconnection of the panels in a variable relation, by means of switches on the panels link cables and plugs, and so-called "trays" which correspond to cables (except that the conductors are mounted in widely spaced relation therein with shielding between, so as to minimize reactance effects and setting up of parasitic pulses or potentials). Also for connecting at alternative parts of the system, three fixed function tables, and three portable truck-mounted ones, the latter having multi-plug couplers with shielded cables by which a large number of circuits may be made from these function tables to and between accumulators or other elements of the system when the plug is inserted where desired.

Optical observation of numerical values registered in the various parts of the ENIAC may also be made on the fronts of the panels.

There are also provided three IBM card machines, commercially available (not illustrated except diagrammatically), one for punching cards with desired patterns; another, a reader, for forming contacts pulses in accordance with punched cards inserted, to complete circuits to electromagnetic input relays of the machine; and another, termed the "printer" to be connected to output points of selected units, by which cards are punched in a significant order defining the results of equations carried out in the machine. These IBM machines will hereinafter be referred to as the card punch, the card reader, and the card printer. A further IBM machine for converting the punched card output to a conventional printed sheet form is also commercially available (not illustrated).

In addition, there are several large power pack panels (not illustrated) erected at a distance from the U-shaped series, in which the necessary transformers and rectifiers are set up to derive from commercial A.C. service lines the necessary potentials and energizing currents necessary for the operation of the machine. The sides of the first named forty panels next to the walls of the room are spaced a distance from the walls to permit ready passage of personnel for access thereto, and are termed the backs of the panels. In the panels there are set up a multiplicity of decade counters, control tubes, gate tubes and the like, involving approximately 18,000 tubes for the whole system at this part. The circuits for, and the nature of, these tubes will be described in greater detail subsequently.

Each of the panels is in the nature of a long box, the length of which represents the height of the panel, the width being that of the horizontal width of the panel, the depth of the box from front to back being sufficient to afford a space between the assembled tubes and the rear side of the box for free movement of cooling air currents from the bottom to top, where exhaust flues are connected. The chassis of the tube-carrying elements of the panels are so arranged that the tubes may be inserted and withdrawn from the rear of the panel without necessarily removing the chassis. And the chassis are constructed as

plug-in units which may be withdrawn manually for repair, or replacement of resistors etc., and resoldering of connections as required, without disturbing other elements mounted in the same panel. The plugs have gangs of blades corresponding to those shown in FIGURES 31–F and 31–G at the ends of the decade unit, and the panel body carries appropriate sockets from which the necessary leads are extended to accord with the mutual connections between the respective elements and other parts of the system as indicated by the relationship shown in the complete drawings of the ENIAC. The rear side of the box has a removable cover extending the full height and width of the panel, having adjustable intake louvers adapted to admit air as required to carry off the heat evolved by the tubes, and at the upper end the box is connected to a flue leading to a manifold duct to which an exhaust blower is connected, as ventilating means. The ventilating system comprises a number of independent units each serving a number of panels and having suitable thermostatic controls. The tubes of the several functioning parts in each panel are all exposed when the cover is removed so that any tube may be readily removed and replaced. In addition, the tubes are mounted in removable chassis carrying tubes grouped according to their circuit relationship. Thus, for instance, each counter ring and its gating and directly associated control tubes are carried on one chassis. As the physical construction of the panels is not here claimed as our invention, it will not be illustrated or described in greater detail.

Considering the panels in succession beginning at the input or left end of the series as shown in FIG. 1, the panel number 1 constitutes the "initiating unit," and is constructed with means to establish the necessary electrical sources of the widely various potentials required to operate the ENIAC, and to permit manual initiation of the operation of the machine by the formation of a starting pulse properly synchronized with the basic pulse times of the system to assure positive starting without liability of splitting a pulse with a result then which might fail to secure proper operation yet might disturb desired initial conditions in parts of the system. The initiating unit also includes other features less essential in the normal functioning of the apparatus, including an oscilloscope to indicate the nature of pulses. The system is so constructed that the starting pulse once communicated, causes storing function of the apparatus with material supplied through the card reader from punched cards, and after such storing (which is limited in rate by the fact that the reader is a partly mechanical device and depends on the operation of electromagnetic relays) the machine will automatically function computatively on the stored material at an electronic rate thousands of times faster in the communication of values and results from one part to another.

Panel 2 is the "cycling unit" which includes a continuous "clock" oscillator from which are continuously derived at ten microsecond intervals pulses which determine the functioning of all other units of the apparatus. It includes tubes and circuits which are constructed to produce cycles or "frames" of pulses of the nature shown in FIG. 2, the use of which will be subsequently explained in greater detail. Each such frame or cycle has an overall or total transmission time of 200 microseconds, called an "addition time," arbitrarily chosen for the present machine because it affords a good margin of excess available time for the performance of an addition operation of maximum length, and is a convenient submultiple of periods for longer operations of different natures such as subtraction, multiplication, division and square rooting. These frames of pulses normally are repeated every 200 microseconds throughout operation of the system, but when required a single frame only, of 200 microseconds, may be transmitted, or a single pulse time operation produced whenever the operator so wills, usually for testing purposes.

It may be mentioned that each such frame of pulses

comprises 20 successive divisions or "pulse times" of 10 microseconds each, and within each of the first 10 of these divisions (numbered from "0" to "9" on the drawing) a "tens pulse" is transmitted to a trunk conductor or bus, each having a nominal duration of two microseconds, but not more than 2½ microseconds, delayed 90° from the beginnings of the respective divisions of the addition time; while in nine of the same "tens" intervals in the frame, "nines" pulses of similar shape, duration, potential and polarity are transmitted to another individual bus conductor, but 90 degrees out of phase with and in leading relation to the "tens" pulses, so that the "nines" pulses are at the beginnings of respective pulse times, represented by the divisions shown in the drawing FIG. 2. More detailed explanation of the derivation and transmission will be given hereinafter. Within the same "tens" pulses times, five control pulse signals are developed here, transmitted over five respective individual bus conductors, the first of these signals being a single "1P" pulse in the second pulse time of the cycle; the second signal being two immediately successive pulses in the third and fourth pulse times of the frame designated the "2P"; the third of the five signals being the "2'P" signal comprising two immediately successive pulses, in the 5th and 6th pulse times; and the fourth control signal being the "4P"—four pulses in immediately successive pulse times. These nine pulses for the four signals are synchronized with the respective "nines" pulses. At the tenth interval beyond the cipher pulse interval a "1'P" pulse is transmitted over a respective conductor. Beginning with and extending over the next interval and all succeeding intervals or pulse times to the end of the 17th pulse time of the frame, there is a "Carry-Clear Gate" which is designated the "CCG," a sustained potential the same as that of the other pulses, lasting throughout the seven intervals or pulse times indicated and communicated to a respective conductor. Also at the beginning of the 17th pulse time a standard pulse similar to those first mentioned is transmitted over a separate bus conductor and designated the "Central Program Pulse" or "CPP." All of the pulses named are of the same potential, which has been chosen at —290 volts; pulsed from a static potential of —345 volts and all except the CCG are of the same duration of two microseconds each.

Within the same frame of twenty pulse times—one addition time—two more pulses of two microseconds' duration are transmitted, over one conductor, one at the beginning of the thirteenth pulse time from the zero interval, and one at the beginning of the nineteenth pulse time, but these two pulses are positive pulses of approximately plus fifty volts, from a static level in the conductor of approximately zero potential. The last two pulses are termed reset pulses, or RP's. In the twelfth, fourteenth, fifteenth and sixteenth pulse times, no pulse is originated by the cycling unit, the periods involved being required however by functioning of the long CCG, to be hereinafter explained.

The third and fourth panels of the series constituting the operating part of the ENIAC are termed the "Master Programmer" panels 1 and 2 respectively. The apparatus in these panels determines where the pulse frames from the cycling unit and pulses from other sources, which are being applied in the remainder of the system shall be utilized. The control is such that, as will hereinafter appear, parallel operations in different panels are made possible.

The 5th and 6th panels in the U-shaped series are termed "Function Table No. 1" and are panels 1 and 2 thereof, respectively. This is an electronic multi-switch system, and operates to provide tables of experimentally or otherwise predetermined values of analytic functions under control of the master programmer. In addition, it may derive a number or numbers from analysis of tables, to be emitted and interpolated in equations as called for.

The 7th and 8th panels are designated accumulators numbers 1 and 2 respectively, and may be utilized, one or both, to gather—that is, to receive and register—arguments to enter on the function table, and are adapted as an internal memory to hold the gathered material for any desired number of addition times, while the function table is "setting up."

The 8th panel last named, labelled "accumulator number 2," while usable as last described, is primarily associated with the divider panel, next following, as a quotient accumulator (also at times it may be utilized as a simple accumulator for other purposes) and to hold the quotient as long as may be necessary, being internally programmed to receive and to transmit the quotient or other material held subject to selective control.

The 9th panel is designated as the "divider and square rooter." It serves to switch numbers between other accumulators so as to cause division and square rooting of numbers received or transmitted thereto for its computative treatment which will be dealt with in detail at further parts of this description.

The 10th to 13th panels comprise accumulators numbered respectively, 3, 4, 5, 6. They are associated with the divider, accumulator number 3 serving for 10 place numbers as a divisor accumulator, and functioning with accumulator number 4 when necessary as a unit for 20-place divisor numbers.

Accumulators numbers 5 and 6 may function as accumulators of the dividend.

The 14th and 15th panels are designated accumulators numbers 7 and 8 respectively and are designated as the "shifter" for use in subtractive division, controlled by the divider before mentioned and performing in any given problem as required and as will be more definitely described.

The 16th and 17th panels next following, designated accumulators numbers 9 and 10, respectively, are used for gathering the multiplicand and multiplier, respectively.

The 18th, 19th and 20th panels constitute the "High Speed Multiplier," designated multiplier panels numbers 12, 13 and 14 respectively, the principal purpose of which is to make available combinations of simple digits, to shift numbers as required in multiplication, and to control operation of the four following summing accumulators which receive the numbers given out by the multiplier panels.

The 21st to 24th panels are summing accumulators numbered 11, 12, 13 and 14 respectively, and include control cables to the printer, being the first panels with such connections in the order in which the panels are being described.

The panels which are 25th to 27th in order are general purpose accumulators designated accumulators 15, 16 and 17 respectively, but have direct cables to the printer. They accumulate answers from computations in any other units when required.

The 28th panel in the series is designated accumulator number 18, and it is associated with the next two panels (comprising Function Table Number 2) to gather arguments for use with Function Table Number 2 in the same manner that the seventh panel is associated with panels 5 and 6 of Function Table Number 1.

The 29th and 30th panels are designated as "Function Table Number 2" panels numbers 1 and 2, respectively, and operate in the same manner as Function Table Number 1, before described.

The 31st and 32nd panels constitute Function Table Number 3, panel number 1 and panel number 2 thereof, respectively, functioning generally in the same manner as the first two mentioned function tables. The 33rd panel is accumulator number 19 which operates with Function Table Number 3 in the same manner as accumulator number 18 (in the 28th panel) serves in Function Table Number 2.

The 34th panel consists of accumulator number 20,

primarily used with the constant transmitter which follows in the series.

The 35th to 37th panels comprise a "Constant Transmitter" "panels numbers 1, 2 and 3," the purpose of which is to receive and register data from a reader of punched cards and therby provide arbitrary constants for the machine. It includes also manually set switches in its panels which may be set to provide additional constants. It is controlled by the "reader" machine and by program pulses received from within the ENIAC. The reader is a machine for receiving and coding material in the form of punched holes in a card produced either by a "printer" in the ENIAC, or by a separate card punching machine with finger operated key board. This is a commercially available unit (not illustrated).

The 38th to 40th panels are designated as "printer" panels numbers 1, 2 and 3 respectively, operating as a unit to control by relays therein a printer. The relays mentioned are controlled by the output of the accumulators above mentioned directly connected to the printer.

There is also provided as a special coupler between units, and for instance located at the high speed multiplier a "pulse amplifier," which is a portable unit adapted to be plugged in between any two panels which are serially operating, to receive the pulse output of one, reform the pulses and transmit them to the unit of the two which is in receiving relation. This device serves an important function also in reducing the load on the transmitters of panels involved in a set-up, and preserves the effectiveness of pulses in the course of transmission, being especially important when the pulse has been carried through a large number of parameters.

In addition to the three function tables referred to, there are also three portable function tables, of identical construction, mounted on casters and having outlet cables with terminal multiblade plugs so that they may be plugged into operative relation with the various units as required, or connected with the permanent function tables to supplement their capacity. Their details will be more particularly described.

The various units above briefly referred to are not required to be limited to the particular locations described, and the order of their arrangement could be otherwise, since intercommunication is by means of program and digit transmitting trays carrying trunk lines leading to all units, and the machine is arranged so that simultaneous operation of several units may be carried out on different parts of a problem.

1.1.3. *Components of the ENIAC*

The important arithmetic units of the ENIAC as thus described are: twenty accumulators, one multiplier, and one combination divider and square rooter.

The accumulators provide facilities for storing numbers computed in the course of a problem and further allowing the addition or subtraction of a second number to or from the stored number. They are capable of performing these operations with up to ten decimal digits and the associated plus or minus sign.

The multiplier computes the product of two decimal numbers of up to ten digits each.

The combination divider and square rooter computes the quotient of two nine digit decimal numbers or finds the square root of one nine digit decimal number.

Electrical connections are established between the units of the ENIAC by connecting them to trunk or transfer lines with plug or cable assemblies in order to provide the intercommunication of numbers. A number of input and output circuits from different units of the ENIAC may be connected to a single trunk provided the number of units is not greater than forty or fifty depending on the length of the trunk. The decimal digits are transmitted into, and received from, these trunks in the form of groups of pulses having a number of evenly spaced pulses, equal in number to the value of the digit represented. Thus, such a group may have from zero to nine pulses. In order to obtain high speed, the trunks have eleven wires in them to enable simultaneous transmission to the ten digits and the sign. It is not possible to transmit signals from more than one unit into a trunk at the same time. Many units may, however, receive signals simultaneously from the same trunk.

1.1.3.1. *Timing Relations and Program Control*

Since the ENIAC contains a number of trunk circuits, operations between various pairs of ENIAC units can be carried out simultaneously. This is possible not only because of this multiple trunk system, but because all units are synchronized by permanent electrical connections with the "cycling unit." Therefore if several operations are started simultaneously between various units of the ENIAC, and since all of these are timed from one and the same circuit, the various operations will end at known times relative to one another. Thus it is possible to plan the next group of simultaneous operations with the assurance that all of the prerequisite steps of the first group have been completed. If the timing of the various operations were not known, interlock circuits would be required to insure the completion of those various operations which are prerequisite to the next group.

The cycling unit supplies a number of specially shaped signals to the other units. It contains an oscillator or "clock" which generates impulses at the rate of one hundred thousand per second, each pulse having a duration of two microseconds. These pulses are fed into a twenty position electronic stepping ring switch or "counter." The stepping of this counter is utilized to develop a frame or cycle of pulses, some of numerical utility and others of control use, including particularly a single "program" pulse at every twentieth pulse of the "clock," defining the completion of a cycle which has been designated as an "addition time." It is the maximum time required for the addition of two ten digit numbers in this machine, and the machine is so organized that lesser additions will each be performed in a respective such cycle. Also other operations of the machine are assigned, or performed in, a definite number of addition times so that results may be put out in synchronism with functioning of a plurality of the units. The program pulses form the basis of the programming system and mark the beginning and end of the addition cycles which are the basic arithmetical intervals of the machine. The addition cycles are thus repeated at one twentieth of the clock rate, or at five thousand per second. An addition, therefore, takes $\frac{1}{5000}$ of a second, or two hundred microseconds.

Each addition time, these pulses (or at least some of them) are supplied to all units of the ENIAC so that when the units are called upon to transmit or receive numbers, the required signals will be available from this source to enable the carrying out of the operation.

When one unit is required to transmit numbers to another, a special selective program pulse is transmitted to the second of the two such other units (the first one usually having been activated to automatically emit a significant pulse), establishing the second one in a receptive condition timed with emission from the first unit and with a pulse of the cycling "frame" so that the latter pulse, according to its time will operate the receiving unit with a corresponding value.

It will be seen from the last explanation that there is no serial transmission of a numerical signal in this system from a point of origin to a point of response, but that the transmitted signal is utilized to enable functioning of one of the pulses in the recurrent "frame" produced by the cycling unit as a clock function, and it will later appear herein that such functioning also results in standardizing the shape and potential of the pulse immediately at the receiving or emitting unit, so that uncertainties of response due to impairment of the pulse are eliminated.

A switch on the cycling unit enables the operator to

suspend continuous operation. The twenty steps of an addition cycle are then carried out every time a push button is pressed. This allows the machine to operate in a normal way during the addition, but permits the operator to advance the problem step by step allowing whatever time is required to check the results of the previous operation. Another position of the switch suspends this type of operation and allows a similar examination individually of each of the twenty steps that occur in an addition cycle. This ability to stop the machine at any or all states of its operation is possible since all of the memory elements are able to retain their state as long as desired, assuming the electric power supply is not interrupted. Each memory element is connected to a small neon lamp which lights up when the element is in the "on" position. Since all the circuits except some of those carrying pulses are directly coupled, any lower clock frequency can be used.

The program pulses previously mentioned as the means of sequencing the machine serve to initiate circuits called "program controls" on the various units. These controls, when initiated by a program pulse, cause the unit on which they are located to operate in accordance with the settings of several switches which are part of the program control. When the operation is completed, the program control may transmit another program pulse through one of a number of special program trunk circuits of one wire each. The program controls are connected to the trunks by a plug and cable assembly, in some respects similar to those previously mentioned for the digits. A program control capable of transmitting a program pulse is known as a "transceiver." A transceiver program control may repeat its operation as many as nine times in accordance with the setting of an associated switch before terminating its operation and transmitting its output program pulse. Some of the units are provided with program control called "receives" which operate only once upon reception of a program pulse and do not transmit a pulse when the operation is terminated. Transceivers, with their switches set to positions which do not operate the associated units, can be used to provide delays and isolating or "buffing" action.

It is now seen that one can set up sequences or chains of operations simply by connecting the output of one program control to the input of another program control, making connections through the program trunk lines using plug and cable assemblies. A special control, on a panel known as the "initiating unit," gives out a pulse upon operation of a manual push button, and this pulse can be introduced into such chains to initiate their operation.

In brief, the program control units known as transceivers and receivers remember, with their switches, what processes are to be done. They also time the operations, allow operation from a single terminal input, and permit signals from the cycling unit to cause the required operation to take place in the unit to be controlled.

If it were sufficient in most problems simply to go through a sequence of operations, the above chain system would suffice. However, two difficulties arise in practice. The number of steps in most interesting problems is so large that the group of about three hundred program controls in the ENIAC would be entirely inadequate. Secondly, it is sometimes desirable to make a choice between two or more sets or chains of operations, this choice depending upon some numbers which are the result of an earlier computation. If this choice were to occur only a few times in the course of a computation, one could allow the sequences to run out, thus stopping the computation. At this point the operator could make the choice manually. If this situation occurs a large number of times in a computation, manual choice would be impractical. Both of these difficulties may be overcome by the use of a unit in the ENIAC called the "master programmer."

The master programmer consists of ten major elements (including several panels), each of which may be employed in various ways to count program pulses and to switch program connections. Each major element contains a six-position electronic stepping switch and an associated counter. For each major element there is one input channel and any program pulse entering this unit is registered in the counter and also causes the transmission of a program pulse from one of six possible output terminals. The position of the stepper determines which output terminal is so activated. A group of manual switches is associated with each counter-stepper unit, and when the number of pulses received by the unit has advanced the counter to a number corresponding to the switch setting, the stepper is moved to its next position and the counter is cleared to zero. Separate switches are provided for each stepper position. The intervals between transfer from one output channel to the next can therefore be determined in terms of the number of pulses received, and a different number may be used for each stepper position. If less than six outputs are desired, a special switch can be set to cause the stepper to return to its first position after reaching any chosen position.

An input terminal allows the counters to be set directly from a pulse group. Another input terminal allows the stepper to be stepped directly from a pulse group. Finally, an input is provided to allow direct re-setting of the stepper. Thus, there are altogether nine terminals—one program input, six program outputs, one direct stepper input, and one stepper resetting input terminal.

To return to the two difficulties previously mentioned which the master programmer is to overcome, it is clear that since most problems may be separated into a large number of repeated routines, each with a comparatively few steps, the master programmer will allow the ENIAC to cope with these problems in spite of having only three hundred program controls.

The master programmer temporarily forms program chains into "rings." This would be impossible without the master programmer, since the number of program cycles around these rings would be uncontrollable if such a ring were established manually.

It is very important to understand that this far from exhausts the possible improvements which the master programmer makes in the ENIAC. It is possible to have the main routine divided into sub-routines, in which case one stepper is used to feed another stepper, thus allowing the proper sub-routine to be chosen in the source of a regular routine. This process can be carried even further, and thus an elaborate heirarchy of program sequences can be established. The saving in program controls accomplished by such arrangements is enormous.

The second difficulty, that of having to make a number of numerically determined choices as to what routine to do next, can also be overcome by using the master programmer. It is simply necessary to use an accumulator as a magnitude comparing device and to have it signal a stepper through its direct input to change to a new routine.

In the ENIAC, the master programmer does not serve as the sole governing unit, but coordinates many small decentralized control units.

1.1.3.2. *Memory*

The ENIAC has its memory divided into four fundamental classes. We shall now discuss three of these classes and postpone the discussion of the fourth until later.

The first class is the one in which the information can be introduced and withdrawn at extremely high speeds, preferably in one addition time ($\frac{1}{5000}$ second). As was previously noted, this is the type of memory provided by the accumulators. This type of memory is necessary to hold the information computed in the course of a problem while some further calculation is made upon it, or until the time when some operation is to be done which requires it.

The second class of memory consists of three function tables or constant storing units. This class of memory

differs from the type of storage employed in the accumulator, mainly in that the tabular values are introduced manually which requires considerable time. These values, however, may be withdrawn at the relatively high speed of five addition times ($\frac{1}{1000}$ second). The function table provides a hundred tabular values of twelve digits each—each tabular value having, however, two sign indications. The digits, as well as the sign indications, are all set by separate manually operated rotary switches. Thus, there are fourteen switches for each tabular value. The two sign indications are provided so that the twelve digits of a tabular value may be assigned to two separate numbers. By dividing the twelve digits into two equal groups, two functions of one hundred tabular values, or one function with two hundred tabular values can be stored in a single table. The hundred tabular values of the function table are designated by the successive decimal integers from zero to ninety-nine. Thus, the first two digits of an argument may be used to choose the correct tabular value, while the remaining digits are used in an interpolating routine which makes use of the regular arithmetic functions of the machine to obtain the value of the function corresponding to the argument. Thus, the function table supplies only the nearby tabular values that are to be used in an interpolation and does not itself do any interpolation. Any desired interpolation formula is set up as a sequence of operations, using the accumulators and multipliers in the same way as is done with any other arithmetic problem. In order to obtain the nearby values which are required in the interpolation, the program controls of the function table also produce arguments which are one or two integers above or below the argument introduced.

Four tabular values, in addition to the one hundred mentioned above have been added—two at each end of the table so that those extra arguments required above will be present in the table when the argument value is either zero or ninety-nine. These tabular values are designated by the decimal integers -2, -1, 100, and 101 respectively. Thus in reality, the table contains 104 entries. Since each entry has fourteen switches, there are 1456 switches to be set. If the switch settings are read to the person setting the switches, they can all be set in approximately half an hour. This comparatively long set-up time is partially mitigated by having three such function tables in the machine and by providing the switch assemblies with wheels and easily disconnected cable connections so that several banks of switches can be left set up and plugged in when required. In fact, where a function is required frequently, it is practical to replace the switch assemblies by permanently wired assemblies which can be plugged in when needed.

Several additional uses of the function tables are possible. They may be used for the storage of any group of constants which must be introduced into the machine at a high speed. In problems where the ordinary program controls of the ENIAC are insufficient, it is possible to employ the table as a 104 position program selecting device using its outputs to initiate program circuits by inserting the function table gang plug in a program tray, rather than feeding the outputs into digit channels. A function table may be used, therefore, to sequence operation, or chains of operations, which may be initiated in sequence or chosen at random depending on the value of the two pulse groups introduced as argument into the table. These pulse groups may be obtained either from the program circuits or from the digit circuits of the machine.

To sum up, three function tables of a hundred and four entries each are provided as memory of the second class, with facilities for dividing the entries into two numbers where twelve digit accuracy is not required for one function. The most notable feature of this type of memory is its large capacity and high speed. Unfortunately, this is coupled with the necessity for manual, and therefore slow, introduction of the data.

The third class of memory is the program equipment which was previously described. The program circuits remember what processes are in progress, what these processes are, how long these processes take, and what processes are to be done next. The actual physical memory is made up of the many tube circuits, switches, trunk circuits, and plug and cord assemblies which make up the programming system in the ENIAC.

The fourth class of memory (punched cards) will be covered later when we discuss the introduction and withdrawal of data from the ENIAC.

1.1.4. *Arithmetic Units*

The accumulators are the basic arithmetic units of the ENIAC. They are able to add a number to a number already stored in them. This ability to add is inherent in ten ten-stage ring counters which serve as the memory elements. In order that numbers may be simultaneously added into all ten counters, a special circuit at each counter originates and inserts in the next counter pulses corresponding to any carry-overs which may take place after the ordinary transfer process. Since subtraction is carried out by a system of complements with respect to 10^{10}, an extra pulse is required to simplify the mechanism for transmitting numbers. Seven pulse times are required for the carry-over process. This additional time must be added to the ten pulse times required to transfer the number, and the three additional pulse times required to allow the program equipment to operate prior to the transfer. A total of twenty pulses is obtained, which corresponds to the twenty stages of the cycling unit. Thus, an accumulator requires twenty pulses spaced at ten microseconds, or $\frac{1}{5000}$ of a second to do an addition. The complement system of subtraction was used to avoid the necessity for having counter rings which could advance in either direction.

The acumulators are provided with two output circuits—one for positive numbers and one for their complements. It is thus possible to transmit simultaneously a number from an accumulator into one channel and its complement into another. If both output circuits are connected to the same channel, it is of course impossible to do more than one of these operations at a time. Five input circuits are provided which allow the accumulator to receive from five different channels. This is a necessity if several simultaneous operations are to be carried out between different pairs of arithmetic units. These input channels are also useful in that they provide a simple method of multiplying numbers by powers of ten.

The accumulator contains eight transceiver program controls and four receiver program controls. Since the transceiver program controls allow an operation to be repeated up to nine times, a simple method of multiplication by small constants is possible. A program control can, if desired, by a manual setting of one of its switches cause an accumulator to clear its counters to zero following a transmission. A manually set round-off switch is provided on each accumulator which enables it to clear and leave a five, instead of a zero, in the decade on the least significant digit side of the digit order selected as the least significant digit to be preserved. This five, in conjunction with a special plug device to delete the undesired digits, allows retention of a few significant figures as may be required. If more than ten significant figures are required, it is possible to connect two accumulators in tandem by means of special plug and cable assemblies and to obtain as many as twenty significant figures. The accumulators indicate the numbers which they contain on a bank of neon lamps, which provide a very convenient facility in checking the operation of the ENIAC.

As previously stated, signals may be taken from the sign indicating circuits of the accumulator to provide magni-

tude discrimination which permits computed numbers to control the program sequence of the machine.

In addition to the two outputs previously mentioned, the accumulators have a set of "static" outputs which provide a ten wire circuit from each counter ring, one wire from each stage. Thus, since there are ten counter rings, a hundred output circuits are available. These circuits provide all the information about a number contained in the accumulator simultaneously and are essential in the multiplier.

The multiplier unit is fed by static outputs from the two accumulators which receive and hold the multiplier and multiplicand respectively. The multiplier contains an internal multiplication table which allows the multiplication of one digit of the multiplier by ten digits of the multiplicand at one time. Since pairs of single decimal digits have, in general, two decimal digits in their product, it is necessary to provide two accumulators to receive the twenty digits which result from the multiplication of one digit simultaneously by ten digits. This is true because it is desirable in the interest of speed, to add all of these "partial products" simultaneously to the accumulated partial products of the preceding steps. These two accumulators can conveniently accumulate the "units set" and the "tens set" of these partial products without any interference in the normal carry-over. Since each set of the successive partial products requires ten channels to receive them, and since every set corresponding to the different digits of the multiplier times all of the multiplicand digits must be shifted by one channel with respect to the preceding one, the product accumulators require twenty input channels. These twenty digits accumulators are made by coupling two ordinary accumulators in the manner previously described. Therefore, two sets of double accumulators, or four ordinary accumulators, are required to collect the partial products from the multiplier. After this collection has been accomplished, the final product is obtained by adding the units set and the tens set with a single shift between the channels to obtain the proper relation between the two sets.

If one of the numbers is a complement, the product obtained will be in error by a number whose magnitude is 10^{10} times the other number. If both numbers are complements, the product obtained will be in error by a number whose magnitude is 10^{10} times the sum of the two numbers. The constant term 10^{20} is discarded by reason of the failure of the carry circuits to accommodate it. Following the collection of partial products, but before the final product is obtained, a special sign-indicating circuit causes appropriate corrections to be made, transmitting them from the multiplier and multiplicand accumulators into the product accumulators.

The multiplier is equipped with twenty-four transceiver program control units, any one of which can control the above process. These program controls each contain a switch which allows the multiplication to be carried out with any number of digits in the multiplier between the maximum of ten and a minimum of two. In addition, other switches in each program control are available which allow the multiplier to cause the reception of numbers into the multiplier and multiplicand accumulators and which allow transmission and rounding-off by the product accumulators.

The time required for multiplication is computed as follows: (*a*) one addition time to operate the multiplication table, (*b*) one addition time for each digit of the multiplier, (*c*) one addition time for complement correction terms, (*d*) one addition time to add the units and tens parts of the partial products, and finally, (*e*) one addition time to transmit the product and receive the next multiplier and multiplicand. Therefore, the maximum time of a multiplication will be obtained with a ten digit multiplier and is fourteen addition times or $\frac{1}{360}$ of a second.

The third, and last, arithmetic unit of the ENIAC is a combination divider and square-rooter. This unit can either divide or take a square root, but cannot do both at the same time. This compromise seems desirable since square rooting is fairly infrequent, and is so similar to division, that very little additional equipment was required to make a combination unit. The method employed to do these processes was chosen so as to require a minimum of equipment since neither of these processes are as frequent as the other arithmetic processes, and, therefore, would not justify a large expenditure for equipment.

Division is carried out by the conventional method of successive subtractions. The only uncommon feature is that the shifting operation is accomplished by transmitting the dividend back and forth between the dividend-accumulator and a special shifting accumulator. This, unfortunately, limits single divisions to nine decimal places. However, since the remainder can be retained, the process can be carried further by a special program arrangement if greater accuracy is desired. Another feature of this divider is that, after successive subtraction of the divisor from the dividend has produced an overdraft, the remainder is shifted one place to the left and the divisor is added instead of subtracted in obtaining the next digit of the quotient. This turns out to be somewhat simpler to adapt to the ENIAC than the ordinary method of restoring the overdraft.

Square rooting is accomplished essentially by the method of subtracting successive odd numbers and is carried out by a method otherwise analogous to division. As in division, the overdraft is not restored before shifting. The combination divider-square rooter makes use of the ability of the accumulators to provide magnitude control and is in itself, therefore, merely a permanent assemblage of program equipment and circuits for supplying the various constants required to build up the answers. This unit requires several addition times to set up and round off its results. The main computational time is that required for the successive additions and subtractions. An addition time is required between each trial addition or subtraction to sense the sign of the remainder. Since five and a half trials are required by lumping the computational time with the set-up and round-off time in a simple formula which gives the total addition time as approximately 13 multiplied by one more than the number of digits required in the answer. Thus, for nine digit answers, the average time required for division or square root is 130 addition times (approximately $\frac{1}{48}$ second). Since this time is variable, depending upon the numbers employed, and may be as high as 210 addition times ($\frac{1}{28}$ second), considerable saving in time may result in carrying out parallel operations.

In order to make possible such parallel operations, an interlock circuit is arranged so that the output pulse, which signifies the end of dividing or square rooting, is not transmitted until both the parallel operation and the division or square root have been completed. This unit is equipped with eight transceiver program controls, each having its own interlock input as well as its own regular input and output.

1.1.5. *Input and Output Equipment*

Since the actual computing process is a highly automatic and rapid one, there must be some system for introducing or withdrawing numerical data which is considerably faster than setting switches or copying down numbers from a bank of neon bulbs, which are the only means so far described for doing this.

In the ENIAC, automatic business macihnes which operate with Hollerith punched cards are employed. Comparatively simple modifications of standard machines of this type give higher speed for introducing or withdrawing data, than appear possible with any other type of

commercial equipment. This speed results from the simultaneous use of eighty channels.

It is, of course, evident that some intermediate memory, such as the cards provide, is necessary if the transition from slow manual operations to fast mechanical operations is to be made. In addition, however, these cards play a very important role in providing the machine with an auxiliary memory of infinite capacity. It is this memory which was referred to earlier as the fourth class. While the absolute speed of introducing and withdrawing data from this type of memory is quite fast (approximately $\frac{1}{12}$ second for a ten digit number), it must be considered as a slow memory compared to the electronic equipment in respect to both the putting in and the taking out of data. Since the card machines, both in reading data from the cards and in punching data onto the cards, scan across one dimension of the card, some auxiliary memory is required to hold these numbers.

Rather than use for this rather slow operation some of the expensive and limited electronic memory which the accumulators provide, a number of telephone relays, of a very reliable type, were employed for this purpose.

Relays are employed not only because they provide an inexpensive memory of adequate electronic pulse initiating speed, but also because they constitute the simplest method of transition from the electro-mechanical card machines to the electronic circuits. This is especially true in the printer where, because a number of contacts may be put on a single relay, it is possible to have a simple mechanism for converting negative numbers expressed as complements (in the electronic circuits) to their true negative form (on punched cards). This latter form is preferred on the cards both to facilitate examination and printing of the numbers and because it fits in with the system which is used by the standard auxiliary card machines. Commercially available prior card printers adapted and constructed to perform this arithmetic operation are used in the ENIAC, and so the particular mechanism of the printer for the purpose will not be described in this application. The final output of the printer unit of the ENIAC itself is utilized to pick up relays such as or corresponding to those customarily used in the commercial printer machine by which the punching of a card is caused in accordance with the numerical value of the output of the ENIAC.

The particular card used for the fourth memory of the ENIAC is also a conventional form largely used in commercial card-operated calculating, sorting, and statistical machines. It has horizontal lines (extending longitudinally of an oblong card) for digits, and two additional such lines for the sign of a digit represented thereunder in one of the ten lines. In each line there are 80 uniform divisions in which holes may be punched. These divisions are aligned transversely of the card to form vertical columns determining the order of the entry, and consequently the value set up in the ENIAC by the contact formed therethrough by the reading brush, as is usual in the prior reader machines.

The input unit including the reader and relays and immediately associated parts of the ENIAC, constitute the "constant transmitter." It can receive cards at the rate of 120 per minute. The output or card punching unit, which we call the "printer," operates from a group of relays which are controlled by the static outputs of the counters in the accumulators and master programmer. Semi-permanent cable connections allow the printer to have its eighty columns controlled from any eighty of the two-hundred and twenty counters which the machine has, with the exception of those which already have their outputs employed in the multiplier and multiplicand accumulators. The printer is capable of punching cards at the rate of one hundred per minute.

1.2. *"Building Blocks" of the ENIAC*

The ENIAC proper consists, as previously stated, of

40 panels (see FIG. 1) each of which in the present computer is approximately 2 feet wide by 8½ feet high, and also includes 3 portable function tables, a card reader and a card-punching machine. The term *unit of the ENIAC* is used to refer to 1 or more panels and associated devices (e.g., the protable function tables) containing the equipment for carrying out certain specific related operations.

The units of the ENIAC can be classified functionally into 4 categories: arithmetic, memory, input, and governing. The arithmetic units include 20 accumulators (for addition and subtraction), 1 high-speed multiplier, and 1 combination divider and square rooter. There are two primary memory aspects in the ENIAC: memory for numbers and memory for programming instructions. The constant transmitter, 3 function tables, and the 20 accumulators provide numerical memory. The constant transmitter with its associated card reader reads from punched cards, numbers that are changed in the course of computation and makes these numbers available to the computer as needed. Numbers that remain constant throughout a computation are stored on the switches of the constant transmitter or of the portable function tables and emitted when needed. The accumulators, not only function arithmetically, but also can be used to store numbers which are computed in one part of a computation and required in other parts. All units have program controls which contribute to the programming memory in the following ways:

(1) By responding to a program input signal which stimulates the unit to perform,

(2) By causing the programming circuits to operate (as specified by the setting of program switches when there are options regarding the operation to be performed), and

(3) On the completion of the operation, by emitting a program output signal which, by means of program cable connections to program lines is brought to other units to cause them to operate. *The program cable connections and switch settings are established before the computation begins.*

The kind of programming described in points 1, 2, and 3 above is described as *local programming* memory because it is taken care of locally at each unit for that unit. The master programmer provides a certain amount of *centralized programming* memory by coordinating the local programming of the other units.

The input unit devices for the ENIAC consist of the card reader and the constant transmitter mentioned above in connection with numerical memory. The printer and output unit card punch record computed results.

The governing units of the ENIAC are the initiating unit and the cycling unit. The initiating unit has controls for (1) turning the power on and off; (2) initial clearing, and other special function; (3) starting a computation. The cycling unit converts 100 kc. sine waves emitted by its oscillator into a fundamental train of signals repeated every addition time (i.e., repeated 5000 times per second). These signals include various sequences of pulses and a gate. The term *pulse* is used to refer to a voltage change (either positive or negative) from some reference level and the restoration of the reference level which takes place in a short time, between 2 and 5 microseconds. The term *gate* also refers to a voltage change and the restoration to the reference level but differs from a pulse in duration. In the ENIAC a gate lasts for at least 10 microseconds.

There are certain fundamental circuits which are repeated many times throughout the ENIAC. We shall discuss a number of these here. In the course of the following discussion we shall use the terms "Pulse" and "gate" with the following meanings:

1.2.1. *Pulse*

A pulse is a positive or negative change in potential

which has a duration of about two to five microseconds (μsec.). Within the meaning of the appended claims "pulse" will be construed to mean a change or excursion in potential or current which has a duration not exceeding about five microseconds.

1.2.2. *Gate*

A gate is a positive or negative change in potential which has a duration of ten micro-seconds or more. The Carry-Clear Gate (see FIG. 2), for example, lasts for 70 microseconds.

1.2.3. *Flip-Flop*

A flip-flop is a four tube vacuum circuit which is the electronic analogue of an electric switch. Two of the tubes (A1 and A2 on FIG. 3) constitute the flip-flop itself; that is, a circuit with two stable states. The other pair of tubes (A3 and A4) are called triggering tubes. In practice each pair of electrode circuits A1, A2; A3, A4; is housed in a single envelope, as shown.

The triggering tubes.—Assuming that no signal is arriving over the *set* input, the grid of tube A3 is at saturation. This causes the tube to conduct. Thus, if a negative signal of the proper magnitude arrives over the set input the grid will fall below cut-off and the tube will cease to conduct.

In order to secure reliable operation it has been a design principle that in *all such cases* the grid should be driven negatively to an extent impressing about three times cut-off bias thereon. Furthermore, to provide for the increase in tube resistance with aging, the applied signal has been so arranged that it will always drive the grid negative with respect to its associated cathode an amount exceeding cut-off bias by a factor at least two and one-half.

If the trigger tube A3 goes off, the grid of A1 will rise well above the cathode potential and A1 will start conducting. The plate potential of A1 will drop and this drop in potential will be carried through the condenser A5 to the grid of A2 tending to cause A2 to go off. As conduction through A2 diminishes, its plate potential rises, impressing a positive-going potential on the control grid of A1 through condenser A6. This causes the grid of A1 to rise even faster. Thus, the whole process accelerates. Tube A1 remains on and A2 off until such time as trigger tube A4 goes off.

In our computer as constructed, the output potential at A7 is −465 volts and at A8 is −430 volts. It will be understood that these values are merely illustrative. After the flip-flop is set by an incoming signal at A9 the potentials of A7 and A8 are interchanged, and they will remain this way until a reset signal arrives at A10.

Note that the condensers A11 and A12 isolate the D.C. circuits so the input to the flip-flop may operate at a voltage level which is sometimes as much as 600 volts above the level of the flip-flop.

The general plan will be to connect the outputs A7 and A8 to the grids of tubes whose cathodes are at a potential between these two output potentials. For example, in receivers and transceivers these outputs go to the grids of 6SN7's whose cathodes are at −450 volts. Thus, −465 volts is well below cut-off for the one tube whereas −435 volts is far above cut-off for the other one. In this manner static voltages produced by a flip-flop are transmitted to other circuits.

It will be understood that the voltage values here given are intended by way of example only, and not as a limitation. For example, it is obvious to any person skilled in the art of electronics that different tubes may be used, which will generally alter the voltage values.

The same type of electronic units located in different parts of the ENIAC will sometimes operate at different absolute voltage levels. For example, the flip-flop at FIG. 3 may operate in a voltage range from −555 volts to −360 volts, but the flip-flops may operate in ranges of from −85 to 110 volts and from −920 to −725 volts. The power supply produces a range of voltages from −920 to 550 volts.

Throughout this description the following convention will be followed with regard to input and output circuits. An input or output will always be represented by only one lead. The return circuit is represented by only one lead and should always be thought of as going back to some point on the bleeder of the power supply. For example, the cathode of a tube may be at zero volts and the output may come from the plate with a range of potential of from 100 volts to 150 volts. Instead of using this output with respect to zero it may be used with respect to −20 volts giving an input potential for the next circuit of from 120 volts to 170 volts. Thus the reference point varies a great deal from circuit to circuit through the ENIAC, and it seems impractical to try to represent the return circuits on the diagrams.

The neon light is visible on the front panel. It is lighted when the flip-flop is set, that is when tube A1 is conducting.

1.2.4. *PM Counters (FIG. 4)*

The PM counter is a binary ring counter; that is, it has two stable states and just one input line. A first incoming signal will step it from stage one to stage two whereas the second incoming signal will step it back to stage one. Thus, an even number of pulses arriving over the input line will leave it in its initial condition whereas an odd number leaves it in the other state.

The tubes A20–A21 in FIG. 4 act as a triggering tube. Whenever a positive signal arrives on the input A22 both of these tubes begin to conduct. This causes the grids and plates of both A23 and A24 to take a negative swing. Since A24 is off it has no effect there, but A23 is caused to go off. As A23 goes off its plate becomes more positive and through condenser A26 the grid of A24 also takes a positive swing. As A24 begins to conduct its plate takes a negative swing and this through condenser A27 further causes tube A23 to go off.

The static output circuits are very similar to the outputs of the flip-flop described above. The positive output has the high potential (relative to the other output) whenever the PM counter is registering a positive number. With tube A23 conducting and A24 not (as illustrated) the neon bulb labeled P will be lit and the one labeled M not.

A positive-going incoming signal on the "clear" input A28 will leave the counter in its initial (or P) state no matter which tube was previously on.

1.2.5. *Decade Ring Counters (FIG. 5)*

A decade ring counter is a ten stage (with two tubes per stage) ring counter with ten different stable states. Each stage has two tubes which will be called respectively tube A and tube B. Only one tube of each stage is conducting. If tube A is conducting that stage will be said to be in state A; if tube B is conducting then that will be said to be in state B. The stable state of the whole ring is with one stage in state B and the other nine stages in state A. The circuits (see the cross section FIG. 36-B or the decade wiring diagram FIG. 5) are so arranged that if one stage is in state B and a pulse is received it will go into state A and the next following stage will go into state B. Pulses that step the ring are negative and are introduced on all the cathodes of the tubes A. This pulse has little effect on the stages in state A but causes the stage in state B to go into state A. As this stage goes from state B to A the carry-over circuit causes the next following stage to go into state B. The fact that this carry-over pulse (through the 50 mmf. condenser) will be in conflict with the stepping pulse applied to the cathode requires careful design to obtain reliable operation. Thus, the stepping pulse must be of precise shape and duration, and the carry-over pulse must over-ride it. This is accomplished by putting the incoming pulses through a pulse standardizer (see ch.

1.2.11) and by using the proper circuit parameters in the decade ring circuit.

The two cathode resistors for tubes in state A and tubes in state B are so chosen as to permit only one mode of operation, namely, one stage in state B and the other nine stages in state A.

The counter is a device of great importance in our computer, being used in approximately ten different forms as will appear later. All of these employ the same basic stepping principle. Because of the importance of the counter and the difficulty encountered in perfecting it, its principles will be discussed in some detail.

In FIG. 5, the 0 stage is shown in state B, and its neon lamp **106** is therefore lit, since it is connected between the plate of tube A of stage 0 and the B minus line **108**. As **A0** (i.e., tube A of stage 0) is not conducting, its plate voltage is high enough to light neon **106** through resistor **109**. All the other stages are in state A, the various circuit potentials being chosen to maintain stability in the condition shown, and therefore the other nine neons are unlit, since the plates of their respective associated tubes are in the conducting condition, and therefore are not at sufficiently high potential to light these neons.

We assume now that a negative pulse of extremely brief duration (e.g., in the order of 10^{-6} sec.) is applied to pulse bar **99**, of sufficient amplitude to make tube **A0** conduct, as the plate voltage of **A0** begins to fall due to this conduction a negative pulse along lead **100** applies a negative bias to the grid of **B0**, which therefore becomes less conductive which in turn raises the voltage (through lead **111**) of the grid of **A0**, in the usual flip-flop action, which continues until stage 0 is changed over to the A state, and neon **106** goes out. At the same time, the rise in potential at the plate of **B0** causes a positive pulse to bias the grid of **B1** through lead **101**, which renders tube **B1** conducting and tube **A1** non-conducting by the same flip-flop action, thus putting stage 1 into state B and lighting neon **107**. As **B1** becomes conducting its plate voltage drops, producing a negative pulse on lead **112**, but this has no effect on tube **B2**, which is non-conducting. Note that this counter is shown as a ring counter, that is, each pulse will change the state of the next tube on the right of the "abnormal" one until stage 9 is reached, after which stage 0 is activated, through lead **113**, to begin the cycle anew on the next pulse.

It will be obvious that at each stage of the counter voltages are available for actuating other elements of the computer as desired, in the form of static positive or negative voltages or else voltage pulses which change respectively to negative or positive as each stage changes its state.

1.2.6. *Other Ring Counters*

There are a number of other ring counters in the various units of the ENIAC. Essentially they differ from the decade ring counters only in the number of stages they contain and therefore do not require detailed description at this point. A list of these ring counters follows:

(*a*) *The repeater ring.* (See FIG. 36–E.)—The repeater ring is used in each accumulator to count the number of times a particular repeat program control operates. This ring and its pulse standardizer are built in one plug-in unit. This same plug-in unit is used in the divider-square rooter for a different purpose, see (*d*) below.

(*b*) *The cycling unit ring.* (See FIG. 29–B.)—There is a twenty stage ring counter in the cycling unit which controls what happens during the twenty pulse times of an addition time.

(*c*) *The multiplier ring.* (See FIG. 42–A.)—This ring controls the process of multiplication. It consists of fourteen stages, ten of which are associated with the ten digits of the multiplier which may be used in multiplication.

(*d*) *The divider-square rooter program ring.* (See FIG. 46–A.)—This ring controls the beginning and final parts of the processes of division or square rooting. It is a nine stage ring which with its pulse standardizer is identical with the repeater ring plug-in units (see (*a*) above).

(*e*) *The divider-square rooter place ring.* (See FIG. 46–F.)—This ten stage ring keeps track of the place in the division or square rooting process. This ring is identical with the master programmer decade rings (see (*h*) below).

(*f*) *The function table argument ring counters.* (See FIG. 48–A.)—These rings (a unit ring of ten stages and a ten ring of eleven stages) receive the argument from an accummulator.

(*g*) *The function table program ring.* (See FIG. 48–A.)—This thirteen stage ring controls the setting up of the function table networks and counts the number of times (up to nine) the functional value may be transmitted.

(*h*) *Master programmer decade rings.* (See FIG. 73–C.)—There are twenty decade rings located on the two panels of the master programmer. These can be used to count the number of times certain sequences of computations are performed.

(*i*) *Master programmer stepper rings.* (See FIG. 73–D.)—There are ten six stage rings which are associated with the ten steppers of the master programmer. These control the output of the program pulses given out by the master programmer.

1.2.7. *Gate Tubes*

Besides being able to count and record pulses at high rates it is necessary to control the pulses, switching them into one unit or another. In order to do this quickly, electronic switching is used. A multigrid vacuum tube is principally used as a switch so as to allow or deny passage of pulses or other signals and is known as a gate tube. Gate tubes are used in the ENIAC for a variety of control purposes. In one case, they place the input channels of any given accumulator in receiving relation to pulses on particular digit trays when a "program" pulse or gate pulse acts on one control grid. They are used in the carry-over circuits to pass carry-over pulses. Each programming circuit contains many gate tubes. The same is true of the various arithmetic units of the ENIAC.

Various gate tube circuits are illustrated. For example, referring to FIG. 6, if there is no input signal to either control grid of the gate tube **A30**, the second control grid **A31** is at about −40 v. relative to the cathode. This is well below cut-off for that grid (cut-off would be −14 volts for 6SA7 if the first control grid **A32** were connected to the cathode). Moreover, the first control grid **A32** is at −40 volts bias, which is well below cut-off (cut-off by this grid would be −7 volts if second control grid **A31** were connected to the cathode); so the tube is not conducting, and the potential on the output lead **A33** from the plate is near 160 volts. If a positive signal (say, of about 50 volts) arrives on either control grid the tube will not conduct. Thus, such signal arriving on the first input **A32** has no effect. However, if such a signal arrives on each grid, the tube will conduct and the plate potential will drop according to the parameters. For example, for the derivation of an input pulse, input 2 at grid **A31** may connect to the plate of an inverter tube (see FIG. 10 for the latter), which is normally on. If this inverter tube is conducting and the circuit parameters are properly arranged, the potential of second control grid **A31** of tube **A30** will be well below cut-off and any signal arriving on its first control grid **A32** will not be passed. A proper negative pulse transmitted to the control grid of the inverter tube will extinguish the latter, and when the inverter is off, the second control grid **A31** will be at about +20 volts relative to the cathode. A positive signal arriving at the first control grid **A32** will then cause the tube **A30** to conduct. The resulting drop at the plate will be manifest as a negative pulse on the output lead **A33**, which is equivalent to passing the signal received as a negative pulse.

The voltages vary from circuit to circuit throughout

ENIAC, and the tubes used in elements of similar function may be varied to provide characteristics suited to such voltages. At the same time the resistances and condensers may also be correspondingly varied to afford the necessary pulse characteristics and required RC time constants. These are expedients well understood and follow as a matter of course in the selection and installations of the parameters. This will be observable in various situations illustrated in the circuit diagrams herein.

A gate tube may be called a coincidence tube, since an output will be obtained only if signals applied to the inputs one and two coincide in time. Besides the one shown in FIG. 6, two other types of coincidence circuits used respectively in the Function Table and the Master Programmer are illustrated respectively in FIGS. 7 and 8.

In the case of the triple coincidence circuit (FIG. 7), all three of the inverter tubes **A35**, **A36** and **A37** must go off before the two control grids of the 807 type tube **A38** are sufficiently positive for it to conduct. In the Master Programmer control or gate circuit shown in FIG. 8, with any one of the tubes **A40**, **A41**, **A42**, **A43**, or **A44**, on, the second control grid potential in the gate tube **A45** remains below cut-off. Thus, this gate tube will conduct only when there is an approximately standard positive signal on the first grid or input 1 and also a required potential on the second grid, and in this instance the latter potential is only manifest when the five tubes **A40**, **A41**, **A42**, **A43** and **A44**, are off.

The positive gate potentials which must be supplied to a gate tube for switching purposes can be obtained from the output of a flip-flop (see FIG. 3, and section 1.2.3.). With the proper relationship of supply voltages for the gate tube and the flip-flop, the positive output lead of the flip-flop may be connected directly to one of the control grids of the gate tube. The effect obtained is that of a switch which may be opened or closed at desired times by pulses applied to the S input **A9** or the R input **A10** of the flip-flop (FIG. 3).

It will be understood from the foregoing that where a negative value signal is to be utilized to operate a gate or coincidence tube, it must be first passed through an inverter, but where the initial signal is positive and of suitable potential and duration, it may be transmitted directly to the appropriate grid of the gate or coincidence tube.

1.2.8. *Buffer Tubes*

Many occasions arise in which it is necessary to couple two or more circuits, say, A, B, C, etc., to another circuit, X, so that any one, say A, can operate X without affecting the others, B, C, etc. This can be done by the use of buffer tubes such as at **A46** (a triode) in FIG. 9. If such a tube has its grid below-cut-off then any moderate or even substantial change in plate potential short of the critical extreme will not cause any disturbance in the potentials of its grid or cathode circuits. Thus, the plates of a number of such tubes (representing the circuits A, B, C, etc.) may all be connected together and to the input of the circuit X, for instance the grid of an inverter. If the grid of one of these buffer tubes receives a positive signal the tube will go on, causing an effective negative input signal to circuit X. This will cause no disturbance in the grid potentials of the others of the tubes A, B, C. However no harm is done if more than one buffer tube goes on at the same time.

A good illustration of the action of buffer tubes is involved in the accumulator (FIG. 36). In the accumulator there are eight transceiver units, each with a clear gate buffer tube (CL.G.B.). The plates of all eight of these buffer tubes are connected to the grid of one inverter tube in the gate unit, FIG. 36C. If any one of these buffers begins to conduct, the potential on all their plates and on the grid of **J50** will fall. The only effect, however, will be that **J50** will go off, which is desired, to cause transmission of a positive signal to the first grid of a clear gate tube. The latter will then function if a coinciding gate potential is manifest on its second grid, by conducting and transmitting a negative pulse to effect the desired clearing action in the accumulator. Although the grids of these clear gate buffers are directly connected to certain gate tubes in the transceivers, operation of the latter tube in one transceiver will not disturb those in the other seven transceivers.

1.2.9. *Cathode Follower*

A cathode follower is illustrated in FIG. 11. The input of the tube **A51** there shown may be derived from the plate of an inverter tube, which is normally on. The conditions in the inverter circuit would then be such that while tube **A50** is conducting the IR drop to its plate keeps the grid of the cathode follower tube **A51** below cut-off. If a signal turns this inverter tube off, the grid potential of tube **A51** will rise to about 50 volts and the cathode follower tube will conduct. As the tube **A51** goes on, its cathode potential will rise making a positive output available between the cathode and its B-lead resistor. This rise in potential is limited by the grid potential.

1.2.10. *Inverter Tubes*

If a positive pulse or gate, rather than a negative one, is required (in order to operate another gate tube, for example), then an additional tube must be inserted in the circuit. This tube, illustrated at **A50** in FIGURE 10, is known as an "inverter." It is normally conducting, and when a negative potential is applied to its grid, so as to bias it to cut-off, a positive change in plate potential takes place. This rise of potential may be used to operate other tubes, normally nonconducting, by causing them to conduct, for appropriate operational effect.

The role of a gate tube is that of the logical "and" while a buffer is similar to a logical "or." Arrangements of inverters such as illustrated on FIG. 7 correspond to the logical "and."

In some cases it is desirable to use a simple switch by which, in response to a positive signal, a positive output signal will be derived, and we have provided a cathode follower element for this purpose.

1.2.11. *Pulse Standardizer*

It has been mentioned that in the operation of a counter it is necessary that the input pulses have a certain shape and magnitude. Distortion of pulses because of the capacitance of interconecting circuits and because of passage through various gate tubes makes it necessary to use a pulse-standardizing means between some of the circuits. A means adapted includes a flip-flop different from that of FIG. 3, discussed in 1.2.3. in that one of its states is only semi-stable (see FIG. 12).

After an input pulse has flipped the circuit from the stable state shown in FIG. 12, with all tubes reversed in state, it will flip back to its original state in a time determined by the circuit constants and practically independent of the input pulse.

The explanation of this action is as follows: the values of resistors **A56**, **A57** and **A58** are such that when tube **A60** is conducting the potential drop across resistance **A57** causes biasing of the tube **A61** at its cathode to cut-off, aided by the condition already existing at the grid of tube **A61** due to conduction at the first tube **A62**. A negative pulse is then applied to the input—the grid of tube **A62**, to diminish the flow of current through the said tube **A62**, impressing a positive-going signal on the control grid of the tube **A61** to initiate the flow of current producing a negative going potential excursion at the anode terminal of the resistor **A59** which cuts off tube **A60**. Then, after a time which depends on the product **A59**, **A63**, tube **A60** is no longer biased to cut-off and as it begins to conduct, the increased current and higher potential across resistance **A57**, acting on cathode of tube **A61** begins to bias tube **A61** to cut-off again. This change in tubes **A61** involves a rise in its plate potential which re-

acts on the control grid of tube A60, and the action is accelerated, bringing tube A60 to full conduction, flipping the circuit back to its original state.

This standardizer includes in its plate circuit an inductance A64, in the present instance a choke of 5 mh. the effect of which on cut-off of tube A60 is to augment the rise of potential at the plate.

This rise in potential is transmitted through A65 to the control grid of A66, causing it to conduct. The duration of this positive signal applied to A66 is almost entirely determined by the parameters A64, A65 and A67 and certain operating voltages, since tube A60 remains non-conducting during this interval. A negative pulse is therefore generated at the plate of tube A66 and appears at the output. Since tubes A61 and A60 constitute a modified flip-flop, it is important to note that the effective plate electrode of tube A60 for this flip-flop action is the screen grid electrode which is held at a fixed potential, and the potential changes of the actual plate electrode of tube A60 have negligible effect on the flip-flop action. The time constant of the flip-flop circuit is made large enough by choice of condenser A63 so that tube A60 will not return to a conducting state until tube A62 is returned to conduction by termination of the input pulse. However, when this occurs no output pulse will be generated because the initiation of conduction in tube A60 will apply a negative pulse to the control grid of A66, and this tube has already returned to a non-conducting state with the decay of potential across the inductor 64.

1.2.12. *Special Pulse Standardizer*

The Special Pulse standardizer A69, shown in FIGURE 13, is intended to enable the communication of a single pulse to the ENIAC from a circuit closing device either a manual switch, or a machine switch or relay device or other, in such manner that the pulse transmitted from the standardizer will be of electronic speed, as, for instance, two microseconds' duration, notwithstanding that the manual switch may be a push button in the operation of which a fluttering contact may occur, and the full period of the contact will extend over a second or more. In the machine switch, also, a satisfactory contact may be considerably longer than the desired duration of the pulse to be transmitted.

There are a number of these circuits located in the cycling unit (see FIG. 29). For instance there are three, the respective inputs for which come from (*a*) the initiating pulse switch on the front panel of the initiating unit, (*b*) the reset cam of the IBM punch producing the "printer reset signal," and (*c*) from the finish cam of the IBM reader producing the "Reader Finish signal."

The special pulse standardizer element normally operates at much higher potentials throughout its circuit than in the case of the pulse standardizer, even the cathodes being at plus 75 volts in the tubes used. FIGURE 13 shows a twin triode A76, like electrodes of which are bridged so that both ends of the tube function alike and simultaneously. A static potential of 75 volts is maintained on the cathodes, and the grids are connected to a 110 volt source, with an interposed outer resistor of 100K, and an inner one of 4.7K in series. Between the resistors a lead from the pulse initiating switch or other circuit closer A75 is connected, which includes another resistor of 4.7K ohms. The two 4.7K resistors are thus in series in the input to the grid. A plus 75 volt lead is also connected between the three resistors named, across a 0.5 microfarad condenser A77. The plates of the tube A76 are connected to the grid of the left tube A80 of a twin triode, and also to the plate of the right tube A81 of this twin triode across a resistor of 47K, a condenser being also connected in parallel with the last named resistor, between the last named grid and the last named plate. The two plates in this twin tube are connected across identical respective resistors of 39K to a plus 285 volt source, and the plate of the left tube is connected across a resistor and parallel condenser to the grid of the right hand tube in symmetrical relation to the leads to the left tube, the cathodes of the two being bridged and connected across a 15K resistor to a plus 75 volt source. There is an additional connection of the cathodes to a static plus 75 potential across a .001 mf. condenser A82. An output lead from the plate of the left tube A80 is taken across a 100 mmf. condenser A83. A plus 75 volt potential is applied to the grid of the right hand tube A81 across a 47K resistor A84.

If the switch A75 is closed, connecting zero potential with the grids of tube A76 through the 4.7K resistor, the condenser A77 will discharge through the 4.7K resistor. The time constant for this discharging action is slightly more than 2 milliseconds. Thus, the switch should be closed for a period of this order of duration, which will be exceeded in the usual manual operation. Closure beyond the time when current flow through the tube A76 is cut off will do no more in the action of the device. As the condenser discharges, the grids of the twin triode tube (initially conducting at both triodes) drop in potential and the tube goes off at both ends.

After the switch is opened the time constant for charging of the condenser A77 with parameters and potentials as indicated in FIG. 13 is about 50 milliseconds. Therefore, if the switch were pushed again before the condenser had recharged, the tube A76 would have not begun to conduct again and there would be no output pulse the second time. The time constants here are purposely slow (compared to the speed of operation of the ENIAC) to prevent any chattering of the contacts of the switch (or other transient effects) from causing more than one pulse to be given out at the output of the circuit.

As tube A76 goes off its plate potential rises causing tube A80 to conduct. The flip-flop action of tubes A80 and A81 gives a negative pulse to the condenser A79 causing the tube A81 to go off. As long as tube A76 remains off, which is at least as long as the input switch A75 is held closed, the tube A80 will remain conducting, and because there is a resistor as well as a condenser from the plate of this tube to the grid of tube A81, tube A81 will remain non-conducting. The time that tube A81 is off is therefore directly dependent upon the time that contact A75 is closed. Two pulses are actually derived at the output of this circuit. The first of these, which occurs when A75 is closed, is a negative pulse since it comes from the plate circuit of tube A80 which has suddenly been caused to conduct. When the contact A75 is opened, the potentials of the various elements in this circuit are again altered as tube A80 becomes non-conducting and a positive pulse appears at the output at this time. The output from this pulse standardizer is used in a further circuit which responds only to negative pulses and does not respond to positive pulses. Such a circuit is, for instance, that of the ordinary pulse standardizer of FIGURE 12.

As a matter of policy the grids in all the tubes such as described in the rings, steppers, gates, inverters, cathode followers, pulse standardizers and the like, throughout the ENIAC, are driven to saturation when the tubes are on, and they receive biasing potentials exceeding the cut off bias potential by factors of three to four when off. This means the circuits are not amplitude-sensitive, that is, a considerable change in supply potentials and in tube conductance (as might be due to aging) will not affect the reliability of operation. Furthermore, to avoid coincidence problems, pulses are never used to gate other pulses; that is, at least one grid of a gate tube is always operated by a gate voltage which has a duration much longer than a pulse (for instance, the carry clear gate—CCG—which lasts over seven pulse times; or the output from the ninth stage of the decade counter to the flip-flop setting gate (in the carryover circuit) which is about one pulse time; or the input to the first grid of gate tube A45 of FIG. 8 which will usually last over a number of addi-

tion times, and the "gates" to the tubes A40, A41, A42, A43 and A44, which may last over several addition times).

It should be appreciated that the inherent result of the particular organization of elements in the pulse standardizer of FIG. 12, not only produces a definite pulse of high effectiveness in relation to the initiating pulse to which it responds, but it is also organized with time constant values definitely related to the internal time constants of the ring circuit, so that the speed of response and certainty of performance of the machine are achieved which are so necessary to a mathematical machine in which great reliance is reposed.

The use of a standardized pulse to operate the ring by application of the pulse to the cathode, in addition to the simplification of constructional and manufacturing details, has among others, also the following highly important advantages contributing further to the durability of the machine, its certainty of mathematical operation (so that successive identical computations will render identical numerical results):

(1) Relieves the grids of the capacity loading of the pulse input circuits.
(2) Allows the use of smaller power to drive the ring circuit.
(3) Prevents undesired modes of counting by the degeneration effect resulting from the operation of the activated tubes.
(4) Pulsing the cathode by a negative pulse permits obtaining the pulse from the plate of a driver tube rather than from the cathode, so that the driver tube is not degenerated.

1.2.13. *Transmitter*

FIG. 14 shows the details of a transmitter circuit A85. Because of the large capacitances inherent in the parallelism or proximity of the interconnection circuits, such as digit trays, program trays, and patch cords, it is necessary to use power tubes working into relatively low load resistances in order to transmit pulses from one unit to another at the rate of 100,000 pulses per second. These pulses are positive in order to operate gate tubes and buffer tubes in the accumulators. Transmitters are used in many situations in the ENIAC, to transmit a pulse from one unit to another or to transmit a pulse from one part to another.

The output, or transmitter, tubes have a load resistance A86 in the cathode circuit, 220 ohms. This load resistance is located in a load box and, in practice, is plugged into a socket in the digit or program trunk into which the transmitter output is fed. This load resistance cannot be connected permanently to the cathodes of the transmitter tubes since, depending upon the jumper connections made on the front panel, several transmitter tubes may feed into the same line. Thus, just one load box must be plugged into each digit trunk and each program trunk.

The transmitter tubes A87 which form the output pulse are beam power tubes, operating simultaneously, but normally off. Since the output load is essentially a large capacitance, the positive pulse can be produced quickly only by abruptly driving the grids of these output tubes positive with respect to their cathodes. In order to make the output pulse amplitude stable, the grids must be sufficiently positive so as to reach the saturation current for the tubes. Considerable grid current will then ordinarily tend to flow, which would bring the tubes below saturation, and it is necessary to provide another tube A88, known as the driver tube, capable of maintaining the required grid potential under these conditions. The driver tube is also a power tube. It is normally conducting, and is cut off by a negative pulse input to its grid in order to effect transmitter operation.

When such a signal arrives at the driving tube the grid drops from about −105 volts to approximately −165 volts. This causes the driver tube to go off, raising the grid potential of the transmitter tubes. As the transmitters to go on their cathode potential rises to about 45 volts, providing the strong positive potential which may be transmitted as a positive pulse past the load A86. The cessation of the negative pulse which operates the driver tube allows the leak of the grid charge therefrom across resistor A89 to the plus 20 volt source shown, and restoration of the driver to conductance

The digit outputs of the divider and multiplier do not have standard transmitters. They have inverter tubes with built-in load resistances. Thus the lines that these tubes feed into must not have load boxes, and for reliable operation the pulses should not be fed into a transmission system exceeding proper loading rules, which will be understood according to the course of transmission.

1.2.14. *Receiver Plug-In Unit (FIG. 35)*

The details of one of two identical circuits used in what we call a receiver A90 appear in FIG. 35 with the receiver block diagram representation. Four receivers are used in the Accumulator.

The incoming signal arrives as a positive pulse at a buffer tube A91, turning it on, and the plate drop here thereupon transmits a negative pulse to a trigger tube A92 in the flip-flop A92, A93, A94, A95, and sets this flip-flop. The incoming signal being a short pulse, the positive charge on the grid of tube A91 leaks to a zero potential source shown connected to the grid across an outer resistor at 47K and an inner one of 15K, the pulse line being connected between these two. This tube consequently goes off without regard to the condition of the flip-flop.

The negative signal from the tube A93 when the flip-flop is set, is passed through an inverter A96 to a cathode follower A97, from which the proper positive pulse of adequate effectiveness is derived. This output termed the fast buffer output, is connected to one deck of one operation switch (not shown in FIG. 35) on the front panel of the Accumulator. On resetting of the flip-flop, which occurs by receipt of a negative pulse at the tube A95 (which remained in conduction on setting of the flip-flop), the conduction at tube A94 and consequent extinguishment of tube A93 removes the negative potential from the grid of A96, restoring A96 to conduction, and thus the output tube A97 is extinguished again. The negative output of the flip-flop derived from tube A94 goes to a buffer tube A99 forming what is called the slow buffer output. The time constant for this output is much longer than that of the so called fast buffer output; this explains the terminology. When the flip-flop is set the positive output from A94 excites the buffer A97′ and transmits a signal to two outputs A97″ used in the gate unit of the Accumulator, for instance, to a carry gate and a reset gate of a decade unit. The last named negative output of the flip-flop also goes to the grid of a gate tube A98 (which is the source of the resetting pulse for the flip-flop), so as to extinguish this gate tube. However, when the flip-flop is set, this gate tube is thereby established (by high plate potential at tube A94) in condition to pass a reset signal, such as the "CPP," and reset the flip-flop. In the case of receivers used in the accumulators the other grid of this gate is connected to the central program pulse (CPP) line. Since the set signal is usually a CPP gated at some other unit of the ENIAC (as will be apparent elsewhere herein), the receiver will start to come on at about pulse time 17 (or slightly later depending upon the time constants of the intervening path) of one addition time. At pulse time 17 of the next addition time the reset gate (the time constants are such that this does not open in time to pass a resetting CPP which would conflict with the setting program pulse) will pass a CPP which resets the flip-flop. Thus, the receiver is on for one addition time. In other units (in particular, in the divider and multiplier) the reset pulse passes through other gates which allow the receiver to remain on more than one addition time.

1.2.15. *Transceiver Plug-In Unit*

As with the receiver, a block diagram symbol **A100** of the device appears in FIG. 34 with the circuit.

As far as the flip-flop, the input to the latter and the fast buffer output are concerned, the transceiver is identical wtih the receiver **A90** and the corresponding parts have the same reference characters, primed. On the normally negative output of the tube **A94** of the flip-flop, however, are two buffers **A101**–**A102** giving two slow buffer outputs. This line also feeds a reset gate **A103**. The output of the latter goes through an inverter **A104** to two more buffer outputs **A105**–**A106** and to a gate **A107** which passes a CPP when the inverter **A104** is off. The CPP passed by this gate resets the flip-flop and goes through a transmitter **A108**, **A109**. The buffers **A101** and **A102** deliver negative pulses respectively to inverters by which the carry output program gate is opened, and the Repeater Input Gate inverter opened—that is established in transmitting condition in case a coincident pulse is received there.

The usual mode of operation is as follows. An incoming program pulse goes through the buffer **A91** and sets the flip-flop. The gates provided by the fast and slow buffer outputs are used to cause the unit (for instance an accumulator) to perform a certain task. When the task is finished a signal arrives at the gate **A103** opened by the normally negative (but now positive) output of the flip-flop. The gate passes this signal, turning off an inverter giving two more output gate signals, and opening the gate **A107** to pass a CPP. This CPP resets the flip-flop and also (having come via cables and program trunk) is admitted to some other unit to program the next step in the computation. The delayed buffers **A105** and **A106** furnish gate signals which may perform the final parts of an operation.

The gate tube **A107** plate output, in addition to being applied to the flip-flop of the transceiver to reset it, is also applied to the control grids of a 6V6 inverter tube **A108** by which a 6L6 power tube cathode follower **A109** is operated to deliver a program output pulse for the control of some other basic computing unit of the ENIAC which will be established in cooperative relation, as by the use of a coincidence tube and the passage of a CPP.

1.3. *Elementary Operation of Units*

The following section will be devoted to a description of the basic principles of operation of ENIAC units. In order to exemplify the principles and interrelations of the elements involved, certain features not essential to an understanding of the basic operation will be omitted; those omitted include such features as the means whereby delayed carry-over is established from one decade ring to another, details of the system for establishing the correct sign of a number, etc. All such details will be included in the final complete description of the ENIAC units, which will be presented in later sections. The present section will include only such details as are necessary to explain the basic principles of operation of some of the most important arithmetic, synchronizing and control units of the ENIAC, and to exemplify in elementary form some of the ways in which these units may cooperate. Block diagram representation will be used throughout, in which the blocks will represent the elements previously described.

As standard practice on all block diagrams of the complete ENIAC, both in this and in all following sections, the following conventions will be followed:

(1) Broken lines indicate pulse-carrying lines, while solid lines conduct gates.

(2) Tubes (except for stages of rings and pulse standardizers) which are normally conducting are shaded, others are not. The word "normally" here means immediately after initial clearing, or in the case of the cycling unit, the situation which exists when the ring is at stage zero and no pulse is coming in from the oscillator.

1.3.1. *Elementary Addition (FIG. 15)*

The following description will not necessarily follow the order of units as they are actually arranged, but will commence with a description of an elementary accumulator composed of 3 decade ring counters as shown at **D1**, **D2**, and **D3** in FIG. 15. The individual decade ring counters are of the type previously described in connection with FIG. 5, and are connected together as shown to represent a 3-digit number, in this case the number 342. Each counter except the extreme left one is so connected with the counter to the left of it that when it is in stage IX and receives an additional pulse to set it back to stage 0, it will at the same time emit a pulse to the next counter on the left on line $D1^1$ or $D2^1$, so that for every ten pulses each counter receives, the counter to its left will register one additional pulse, and thereby count the next higher power of ten in conventional fashion for any decimal system of decade counters. This of course will not apply to the last counter on the left.

In FIG. 15 incoming pulses are separately carried to the 3 counters on lines **D21**, **D22**, and **D23**. In practice, these lines will be connected to the suitable lines of the digit trays described in 4.2.7. The units counter is connected to the units line **D21** of the digit tray; the tens counters to the tens line **D22** of the tray, etc. We shall assume that the incoming lines are to add the number 168 to the number 342 carried by the counter. It is assumed that this takes place during one addition time ($\frac{1}{5000}$ sec.), during which the numbers 1, 6 and 8 arrive over lines **D23**, **D22** and **D21**, respectively, in the form of the desired number of pulses coming in over each of these lines to its associated counter during the one addition time under consideration. How these pulses are produced will soon be shown.

The addition of 342 and 168 is indicated below in conventional fashion:

(1)

342
168
510

In the counter shown, it will be seen that the units counter **D1**, registering at stage II, receives 8 additional pulses from line **D21**, which changes the registration to stage 0 to give the units digit of the above sum, 510. As the counter passes from stage IX to stage 0, a pulse is transmitted on lead **D1'** into the tens counter **D2**. In practice means are provided to delay this pulse so that it will not conflict with the pulses arriving at the tens counter over line **D22**, as will be shown later, so that this pulse will be added to the 6 pulses arriving on line **D22** to produce a total of seven pulses transmitted to the tens counter **D2** during the addition time under consideration; since the tens counter originally registers at stage IV, the seven successive pulses it receives will bring it around to register at stage I to provide the second digit of the sum 510, and a pulse will be transmitted over line **D2'** as the tens counter passes from stage IX to stage 0. This last pulse, added to the one pulse coming over line **D23** moves the hundreds counter **D3** from stage III to stage V, the whole counter will now carry the sum 510 instead of the original quantity 342, and the addition is completed. The counter shown can carry numbers up to 999.

In the ENIAC counters are provided on each accumulator to carry ten digits. Neon lamps, as shown in FIG. 5, are provided on the front panel of each unit to show the stage which is energized in the abnormal state at any time, that is, to show the number carried by each counter.

1.3.2. *Elementary Subtraction (FIGS. 16A and 16G)*

Referring now to FIGS. 16–A and 16–B, we shall now consider the operation of subtraction with the same two numbers as before. The 3-digit counter is assumed to be carrying the same number as before, namely, 342. It is

desired to substract the number 168, which was added in the previous example.

The subtraction of 168 from 342 is indicated below in conventional fashion:

(2)

$$\begin{array}{r} 342 \\ -168 \\ \hline +174 \end{array}$$

In some conventional computing machines subtraction is accomplished by running the digit counters backward. In our device, it is considered easier to eliminate this complexity, which we do by adding the so-called "tens complement" of the subtrahend, as is well understood in this art. The tens complement of the number 168 is obtained by subtracting it from the suitable power of 10, as indicated below:

(3)

$$\begin{array}{r} 1000 \\ -\ 168 \\ \hline \text{M } 832 \end{array}$$

The letter M before a number indicates that the number represents the tens complement of the number with which we are actually concerned and that its addition to another number represents a subtraction, as indicated below:

(4)

$$\begin{array}{r} \text{P } 342 \\ \text{M}832 \\ \hline \text{P } 174 \end{array}$$

It will be noticed that the actual sum of the above two quantities is 1174, but even when there is a carry-over pulse from the hundreds counter, as in the above example, the sum would read simply as 174 because the thousands digit would lack a counter to carry it. Actually the ENIAC does register the carry-over pulse from the last counter, but not on a digit counter; it registers this carry-over pulse on a PM counter (see FIG. 4) and uses it to provide the difference quantity (174 in this case) with the proper P or M indication to show whether this difference represents a positive (P=plus) or a negative (M=minus) quantity. If a negative quantity, it should be kept in mind that it is actually a tens complement, that is, any number on the ENIAC preceded by an M represents the tens complement of another number, and this latter number is obtained by subtracting the former number from the suitable power of ten.

To revert to FIG. 16–B, with the decade counters carrying the numbers 342 as before and with the PM counter set at P, if it is desired to subtract 168 from 342, the 3 lines D'3, D'2 and D'1 carry the numbers 8, 3 and 2, respectively (see Examples 3 and 4) and a fourth line D'4 carries a PM pulse (actually any odd number of pulses), all together representing the complement M832, which really signifies the quantity −168, as explained above (how the complement is obtained by the ENIAC will be explained).

When this quantity M832 is added to the quantity 342 carried by the counters, in exactly the same fashion as explained in connection with the preceding figure, the counters will then carry the number 174 (see Example 4). The odd number of pulses coming in on line D'4 will change the setting of the binary PM counter from P to M (if the odd number is greater than 1, this will happen several times, but the last time will necessarily leave the counter on M); however, the carry-over pulse from the tens counter, representing the addition of 3 and 8, will shift the PM counter back to P, so that the final value appearing on the counters will be P174, which is the correct value for the subtraction.

The above principle is equally applicable to a subtraction which results in a minus quantity. For example:

(5)

$$\begin{array}{r} 342 \\ -557 \\ \hline -215 \end{array}$$

On the ENIAC, the numbers −557 would be represented by its tens complement M443 (how this is derived by operation of the ENIAC will be shown later) as follows:

(6)

$$\begin{array}{r} 1000 \\ -\ 557 \\ \hline \text{M } 443 \end{array}$$

This tens complement would then be added to 342, as follows:

(7)

$$\begin{array}{r} \text{P}342 \\ \text{M}443 \\ \hline \text{M}785 \end{array}$$

The answer thus is shown to be a negative number and is obtained by subtraction from 10^3, as follows:

$$\begin{array}{r} 1000 \\ -\ 785 \\ \hline 215 \end{array}$$

If it is desired to subtract 215 from some quantity in the next succeeding step, it would not be reconverted, but the quantity M 785 would be added directly in said step.

It will be noted that in this case the answer carries the sign M because there is no carry-over pulse from the hundreds counter, so that this sign carries out correct in the case of either a minus quantity or a plus quantity resulting from a subtraction.

1.3.3. *Elementary Cycling Unit (FIG. 15A)*

In order to show how the pulses representing the numbers 168 may be put on a digit tray bearing lines **D21**, **D22**, and **D23** in FIGURE 15, it is necessary first to describe the essential elements of the cycling unit shown generally in FIGURE 15 but in somewhat greater detail in FIGURE 15–A. The cycling unit is the device which periodically provides pulses which represent digits and other pulses (gates) which synchronize control and permit programming of other units of the ENIAC.

With reference to FIGURE 15–A (a hypothetical use of some of the basic elements), the block **C0** represents a standard quartz crystal oscillator, which may be of any known design, which emits, for example, 100 kc. sine waves. These are shaped by pulse standardizer **C3** (see FIGURE 12) into pulses about 2 microseconds in duration spaced at a 10 microsecond interval. The fundamental unit for the ENIAC, one pulse time, is thus established at 10 microseconds. The general shape and spacing of these pulses as actually used is shown at the 10 P line on FIGURE 2.

These pulses are conducted through lead **C1** to a 20-stage ring counter **C2** (called the cycling unit ring), which is generally similar to the decade ring counter in its operation—that is, each successive pulse emitted by pulse-former **C3** advances the ring one stage. When any particular stage is reached, a pulse can be emitted from that stage (as was explained in Sec. 1.2.5), which can be used to gate a flip-flop or can be used in some cases directly as a digit pulse or a control pulse. For example, when stage 0 is reached, it can emit a pulse on line **C4** which will set flip-flop **C5** to put a positive potential on line **C6** to the gate tube **C7** so that **C7** will pass all pulses from **C3** on to line **C8**. This condition will last for 10 pulse times at which time stage 10 of the cycling ring will be energized, and a reset pulse will therefore be

emitted on line C9 to reset flip-flop C5 and remove the gating voltage from C7 so that no more pulses from C3 will pass along line C8 until the cycling ring again reaches stage 0, when the procedure will be repeated. As there are 20 stages in the cycling ring, 10 successive pulses will be transmitted on line C8 followed by no pulses for the next 10 pulse times, then another 10 pulses, etc. The duration of 1 complete cycle on ring C2 is referred to as one addition time throughout this specification. With the 100 kc. oscillator shown, one addition time will be 20 pulse times of 10 microseconds each. The addition time is therefore $^{200}/_{1,000,000}$ second or $1/5000$ second in duration.

The series of 10 pulses produced each addition time as described above (and hereinafter called "tens pulses" or 10P) is fed into each of three decade rings of a counter C10 shown in FIGURE 15. This counter is shown as registering the number 168, and it will be shown how this number is transmitted in any given addition time, out along lines D21, D22, and D23.

It will be noted that when the tens pulses arrive at counter C10, each ring of the counter is stepped up ten times and finally stops again at the same number 168 because the counter, for this purpose, does not carry-over from one ring to another. Each ring of the counter C10 is provided with a lead, C11, C12, and C13, respectively, which transmits a pulse to set flip-flops C14, C15, and C16, respectively, as each ring passes from stage IX to stage 0 due to reception of the tens pulses.

A line C18 is provided, similar to C8, for the transmission of pulses from the cycling ring, except that its flip-flop C20 is reset after 9 pulses have been passed, instead of 10 pulses as in line C8; and for the hypothetical case of FIGS. 15 and 16, these 9 pulses (hereinafter termed the "nines pulses" or 9P) are assumed to be passed through a delay line C24, so that they are sufficiently out of time phase with their corresponding 10P, as schematically shown in the diagram. (Actually in the ENIAC the 10P pulses are delayed 90 degrees from phase with the 9P pulses.) These nines pulses are passed to gates C21, C22, and C23, simultaneously so that they will appear on lines D21, D22, and D23 if each gate is properly conditioned by a positive voltage from its associated flip-flop C14 to C16. *During a given addition time* (cycle of 20 pulse times) each gate C21 to C23 becomes so conditioned only after its associated counter has passed from stage IX to stage 0.

Considering first the units ring of C10, which is energized at stage VIII (as indicated in the drawing) at the beginning of the addition time under consideration; after pulses one and two of the tens pulses have arrived, the units ring has just passed through stage IX to stage 0, and flip-flop C14 has thus just been set, which opens gate C21. Almost immediately thereafter (for example, 0.5 microsecond) that one of the nines pulses which is numbered 8 in FIGURE 15 (i.e., the *second* nines pulse) arrives at gate C21, and is passed through to line D21 (the preceding nines pulse was of course not passed). The rest of the nines pulses occurring during this addition time (8 pulses) pass through to line D21. A few pulse times (shown as 8 pulse times) after the last nines pulse, the cycling ring C2 has reached stage 17 and a reset pulse is gated through C29 and transmitted on line C30 to reset the flip-flops C14, C15 and C16 so that they are ready for the next operation. While 8 pulses were being transmitted on line D21, by a similar process 6 pulses were being transmitted on line D22 and 1 pulse on line D23. It is thus shown how pulses corresponding to the number carried by counter C10 may be transmitted on the digit lines associated with the counter during one addition time. With the arrangement shown, this operation would be repeated each addition time, and the number 168 would be added to the total kept by the counter D1 to D3 5000 times each second. In practice transmission of the number will be controlled either manually or by program pulses from other parts of the machine, as will be shown later.

1.3.3.1. (*FIGS. 16–A and 16–B.*) *One Addition Time Operation*

A manual means for energizing the cycling ring for one addition time is shown in FIGS. 16–A and 16–B, in which corresponding parts are given the same reference character as in FIG. 15. In this case the output from pulse former C3 is passed to two gates C40 and C42, the latter of which is normally conducting, but which is blocked when a pulse from stage 19 is passed on line C44 from the anode circuit of the normally nonconductive tube section in the stage 19. Push button C56 controls a special pulse former C58 which passes a pulse approximately two pulse times in duration on line C60 when the push button is pressed. The reason for so wide a pulse is to insure that conditioning of gate C40 lasts long enough to coincide with the arrival of at least one pulse from C3. At this time the cycling ring will be at stage 19 (why this is so will soon become apparent). The passage of a pulse from C3 through gate C40 to the input of stage 0 of the cycling ring along line C62 will change the setting of the cycling ring from stage 19 to stage 0. This will remove the blocking bias from gate C42 and permit the next 19 pulses from C3 to pass through gate C42, stepping the cycling ring C2 along until it comes back to stage 19, at which point the blocking bias on line C44 becomes effective to block gate C42 and prevent the passage of more pulses to the ring until the push button is again pressed to provide a pulse for stage 0.

The special pulse former C58 may be of any suitable design for forming a gating pulse of about 20 microseconds' duration each time the button is pressed, such as a condenser discharge device; however, we prefer to employ a flip-flop in which the normally negative output is used to reset the flip-flop immediately after it is set, as will be shown later in the more detailed description of the ENIAC.

From the foregoing description, it will be evident that when the push button is pressed, with the rest of the circuit as shown in FIGURES 15 and 16, the number 168 will be added to number 342 on the counter shown in FIG. 15 to give 510. If the push button is pressed a second time, the number 168 will again be added to 510 to give 678, etc. If the counter C10 is reset to carry some other number than 168, this number will be added to the total when the button is next pressed. Thus is shown the principle whereby simple addition is performed on the ENIAC.

1.3.4. *Production of Complementary Pulses for Subtraction*

It will now be shown how the complementary pulses previously described (for use in subtraction) are obtained. The previous description of subtraction (see sec. 1.3.2) showed how tens complements are used for this purpose. In the ENIAC, we actually transmit the complement with respect to nine, instead of with respect to ten, and then transmit one more pulse in the 10° (i.e. farthest to right) decade place to produce the tens complement of the transmitted number. That is, the pulses first transmitted are those for

$$\sum_{i=0}^{9}(9-a_i)\cdot 10^i$$

after which one additional pulse in 10° decade place is transmitted.

The terms $9-a_i$ are called nines complements. This is a well-known procedure in the computing machine art and we do not broadly claim the use of nines complements. For example, the 10's complement of 168

(see Example 3 in sec. 1.3.2) is M832 on the ENIAC. Actually we transmit first the 9's complement M831,

(8)

$$\begin{array}{r} 999 \\ -168 \\ \hline M831 \end{array}$$

and then one additional pulse

(9)

$$\begin{array}{r} M831 \\ +\quad 1 \\ \hline M832 \end{array}$$

giving the desired 10's complement.

We shall now show, in connection with FIG. 16, how this is done.

The lines C8 and C18 bearing the 10's pulses and the 9's pulses, are the same as in FIG. 15. The counter C10 is assumed to be bearing the same number 168 as before. It is desired to transmit the contents of this counter (number 168) to some other unit, for example, the counter shown in FIG. 16–B during the addition time under consideration. During this addition time switch C46 (the "add" switch) will first be assumed to be closed and switch C47 (the "subtract" switch) assumed to be open. Closing of "add" switch C46 conditions gates C48 and C49 for the passage of nines pulses on line C51 and tens pulses on line C55, as previously described. At the same time a 2-stage or binary counter C54 is provided for passing the proper indication of P or M as explained in 1.2.4.

The subtract and add gates (C56 and C57 respectively) of the PM unit are controlled by stages P and M respectively of the PM counter C54. When a positive number is stored for transmission (as in the present example) a positive voltage from stage P holds gate C56 open but no 9P (nines pulses) are emitted over the PM lead D'4 of the "subtract" trunk because the gate C50 is closed preventing their appearance on the line C52 at the input to the gate C56; no pulses are transmitted over the PM lead D4 of the "add" trunk since gate C57 is closed. If the sign of the stored number were M, gate C57 of the "add" line would be conditioned to pass 9P (nine pulses) from the line C51 to the "add" trunk D4 and gate C56 of the "subtract" line would be conditioned so that no PM pulses would be transmitted through to the "subtract" line. Note also that if the counter were conditioned for reception to perform addition or subtraction, the carry-over pulse from the last digit ring on the left would be fed to the PM counter, to perform the function previously explained of keeping the sign correct resulting from addition or subtraction.

The above explanation only amplifies the previous explanation of addition to explain the PM function. We shall now continue with the process of subtraction.

For subtraction, we assume that the "subtract" switch C47 is closed and "add" switch C46 is open, so that the 9P now pass through the gate C50 to line C52 and the gate C56. Considering for example, the first or units ring of counter C10, which ring bears the number 8. After two of the 10P have arrived, the units ring has just passed from stage IX to stage 0, and the flip-flop C14 has just been set. While the first two of the 10P are coming in, the flip-flop C14 conditions only the gate C'21 on the "subtract" (or S) line, therefore, the first of the 9P (the one numbered "9" in FIG. 15) is passed through on line D'1, thus producing the nines complement of 8 on the "subtract" line associated with the units counter as indicated by the pulse time chart associated with the lines. If the "add" (or A) switch C46 were also closed, the following 8 pulses of the 9P would go out on "add" line D21, but if "add" switch C46 is opened, these pulses do not get through gate C48. The reason that the following 8 pulses would not go out on line D1 is of course that the flip-flop C14 is set when the units ring moves from stage IX to stage 0, as previously explained, so that gate C'21 can no longer pass pulses from line C52, while gate C21 is at the same time conditioned by the flip-flop to pass pulses from line C51. While "subtract" switch is closed, it should be noted that the 9P are also passing through gate C56 to line D'4, due to the setting of the PM counter, as previously explained.

An example has thus been provided of an elementary circuit for producing a given number or its nines complement, together with the proper sign indication. The principle shown is the one used in the ENIAC, although the details of the ENIAC necessarily differ somewhat from those shown above due to the much greater complexity of the ENIAC.

To convert the nines complement into tens complement an additional pulse is provided on the units line of the outgoing "subtract" circuit after the last 9P. This is accomplished by gating a 1'P (see FIG. 2) through gate C53 by means shown later to line D'1. As the 1'P occurs one pulse time later than the last of the 9P, this pulse cannot conflict with any of the digit pulses, but only adds one more pulse to connect the number carried by the "subtract" trunk from a nines complement to a tens complement. It will be obvious that a negative number can be set up in counter C10 as readily as a positive number; it is merely represented by its 10's complement on the counter. To use our example again, −168 would be set up as M832. In this case, when it is transmitted additively (over the "add" trunk) the digit 832 will go out over lines D23, D22, and D21, respectively, while 9P will be passed through gate C57 to line D4, because of setting up the M counter instead of the previous P counter. Similarly, if M832 is transmitted subtractively (over the S trunk), it will come out P167 on the S digit lines, then the additional 1'P is added in the units place, as before, to give P168, which is correct, for subtraction of −168 is the same as adding +168.

1.3.5 *Elementary Multiplication*

Process employed.—The multiplication process employed in the ENIAC differs somewhat from the usual manner of multiplication with pencil and paper, and will therefore be described first; later it will be shown how the machine performs this method.

Considering the same two numbers we have used in previous examples, we show below the usual manner of multiplication:

(10)

$$\begin{array}{r} 168 \\ 342 \\ \hline 336 \\ 672 \\ 504 \\ \hline 57456 \end{array}$$

This can equally well be done in a slightly different order:

(11)

$$\begin{array}{r} 168 \\ 342 \\ \hline 504 \\ 672 \\ 336 \\ \hline 57456 \end{array}$$

The method of Example 11 can be carried out with partial products, i.e., in the first step of the multiplication we multiplied 3 by 8 in Example 11, and wrote the 4 (of the product 24) under the line, and carried the 2 for later addition to the product of 3 by 6. Instead of carrying the 2 mentally, it can be written down as a separate partial product, so:

(12)

$$\begin{array}{r} 168 \\ 342 \\ \hline \end{array}$$

Left hand partial product	Right hand partial product
2	4

The next steps of multiplying 3×6 and 3×1 are similarly written down:

(13)

168
342

012 384

When we multiply 168 by 4 (the second digit of 342), we shift one place to the right, following the general method of Example 11; and similarly with 168×2:

(14)

168
342

012 384
023 442
011 226

01441 43046=Right hand partial product
+14410=Left hand partial product×10
57456=Total product

It will be noted in the above example that the left-hand partial product is multiplied by 10 since it represents the tens part of the product.

The above method is used in the ENIAC.

In multiplying by this method, we use (instead of the conventional multiplication table) a set of special "partial products" tables set up so that for each number of the multiplier there will be a left-hand and a right-hand partial products table. For example, considering the tables of 3 to 5, respectively:

×	L.H. Prod.	R.H. Prod.	L.H. Prod.	R.H. Prod.	L.H. Prod.	R.H. Prod.
1	0	3	0	4	0	5
2	0	6	0	8	1	0
3	0	9	1	2	1	5
4	1	2	1	6	2	0
5	1	5	2	0	2	5
6	1	8	2	4	3	0
7	2	1	2	8	3	5
8	2	4	3	2	4	0
9	2	7	3	6	4	5

We set up a "function table" for each digit which in two separate places sets up values corresponding respectively to the left-hand and the right-hand partial product resulting from the multiplication of each digit from 1 to 9 by every other digit from 1 to 9, similar to the above tables for numbers 3, 4, and 5. How this is done will be shown below.

1.3.5.1. *Multiplier-Selector Function Table*

FIG. 17 is a simplified schematic showing of the essential circuits of a high-speed multiplier similar to that used in the ENIAC.

The portion inclosed in the block **M10** is called the multiplier selector and consists of a 3-place counter fed by static cable **M12** which leads from an accumulator bearing the multiplier, which will be taken as 342, in order to carry out the example given in the preceding section. Counters **M1**, **M2** and **M3** carry the hundreds, tens and units (places) digits of the multiplier number respectively, which are represented by blacked-out gates 3, 4 and 2 respectively. These gates are in the conductive state throughout the multiplication, which consumes one addition time for each digit in the multiplier, plus several extra addition times for control, sign and other operations which will be explained in connection with the complete multiplier diagram, but not at this point. The present diagram also omits the usual buffer tubes, transmitters, etc., in the interest of simplicity, as it is here sought to explain only the essence of multiplication as performed by the ENIAC, and not to show a complete working circuit.

Connected to the respective places of multiplier selector **M10** are the leads from a stepping counter **M4**, similar in construction to the other stepping counters previously described in connection with the accumulator, and arranged to activate decade counter **M1** during the addition time when stage 1 of the stepping counter **M4** is energized; to activate **M2** during the next addition time, when stage 2 of the stepping ring is energized; and counter **M3** during the next addition time. A fourth stage is shown, which may be used to terminate the multiplication. It will be understood that the complete multiplier selector used in the ENIAC has ten decade counters sufficient for a ten-place multiplier, and a corresponding number of stages in the stepping ring.

1.3.5.2. *Multiplier-Permanent Function Table*

We shall consider first what occurs during the addition time when stage 1 of the stepping counter **M4** is energized. During this interval ($\frac{1}{5000}$ second) stage 3 of place **M1** is activated, so that its corresponding horizontal bus bar, also numbered 3, is activated. This bus bar crosses a number of vertical busses in close proximity thereto, but out of contact therewith except where connection is made between the horizontal bus and a vertical bus by a respective fixed resistor, R, permanently soldered (or otherwise connected) to the busses. These resistors R are of such value as to impress a suitable blocking bias from the horizontal bus on those gates **M6** to which they lead, but are sufficiently high in resistance value so that the voltage impressed on a vertical bus will have diminished sufficiently (due to the IR drop resulting from any "back circuit" currents through other resistors R associated with any given vertical bus) along any other path than the intended one from any energized vertical bus to other horizontal busses, so that no other gates **M6** will be blocked than the ones associated with the particular vertical busses which are energized.

The vertical busses are divided into two main groups **M14** and **M16** which constitute permanent function tables, and are connected to respectively give the left-hand partial products and the right-hand partial products of the numbers represented by the respective horizontal busses. The horizontal busses run across both function tables.

Each table has a number of gates, **M6**, previously referred to, each of which is energized during each addition time by pulse lines **M6'** connected to the cycling unit (not shown), each gate being connected to one pulse line so as to be energized by the 1P, 2P, 2'P or 4P each addition time. In other words, the line bearing the 1P receives and conducts one pulse to its connected gates during each addition time; the line bearing the 2P receives the next two pulses emitted from the cycling unit; the line bearing the 2'P receives the next 2 pulses emitted from the cycling unit after the 2P; and the line bearing the 4P receives the next 4 pulses. By combining the outputs of these lines in various combinations, any number of pulses from one to nine can be procured during one addition time. The outputs of these pulse lines are conducted to the respective gates **M6** and will pass through the gates unless the gate is blocked by a biasing voltage derived from the horizontal bus which is activated during any particular addition time, and then only if that horizontal bus is connected to the vertical bus from the gate in question by a resistor R.

The permanent function tables **M14** and **M16** are shown in FIGURES 17 as containing groups of vertical busses associated with the numbers 2, 6, 7 and 8 for function table **M14**; and numbers 1, 6, and 8 for function table **M16**. It will be understood that ordinarily there will be a group of vertical busses for each digit needed, but in this case we show chiefly the numbers needed to work out the example which has been given. During the addition time when stage 1 of **M4** is energized we shall perform the multiplication indicated in preceding Example 13, that is, we shall multiply 168×3. During this addition time horizontal bus 3 is activated. Considering first the vertical bus associated with number **2** of function table **M14**, it will be noted that this is connected by a resistor R to horizontal bus 3. This verti-

cal bus leads to a gate associated with the 1P pulse line and if it were not blocked by the biasing voltage derived from the vertical bus it would pass 1 pulse through on line M20; however, due to this voltage no pulses will pass through. Inasmuch as this vertical bus is associated with the left hand partial product of the multiplication of the number 2 by the digits respectively associated with the horizontal busses, it is obvious that no pulses should be issued for any number less than 5, as the product of 2 and 5 is 10, of which the left hand partial product is 1; but if any horizontal bus from 5 to 9 is activated, one pulse should be emitted from line M20 and it will be noted that this would occur, since the horizontal busses from 5 to 9 have no resistors R connecting them to the vertical bus. In the right-hand table M16 the product of 3×1 will produce 3 pulses in line M30, as will appear.

Considering next the multiplication of 3 and 6, the product, 18, would be represented by a 1 in the left hand partial product side and by an 8 in the right hand partial product side. It will be seen that these conditions are complied with since of the 3 vertical busses associated with number 6 in M14, only the one associated with the 1P will permit pulses to pass through to line M21 as the other 2 gates, 2 and 2' associated with number 6 are blocked by being connected (through resistors R) to the energized horizontal bus 3. On the right hand function table M16 horizontal bus 3 is not connected to any of the vertical busses 2, 2' and 4 which are associated with number 6 and therefore the sum of these pulses amounting to 8 pulses will be passed from the pulse lines through gates M6 to conductor M31 of the right hand multiplicand selector. Thus it will be seen that line M21 associated with number 6 in the left hand partial products table emits 1 pulse to the left hand multiplicand selector, while line M31 associated with number 6 of the right hand partial products table emits 8 pulses in the right hand multiplicand selector. This satisfies the conditions for multiplication of 3×6.

In similar fashion each line M20, M21, M22, M23 etc., emits pulses corresponding to the left hand partial product of 3 by each of the numbers of the table (only numbers 2, 6, 7 and 8 are shown in the drawing), and similarly lines M30, M31 etc., emit numbers corresponding to the right hand partial product. It will be noted that these pulses are emitted simultaneously from all lines M20 to M32 during the one addition time when horizontal bus 3 is energized. During subsequent addition times other horizontal busses may be successively activated, and during these times lines M20 to M33 will therefore emit pulses corresponding to the partial products of the number associated with the respective activated horizontal bus by all of the numbers associated with the vertical busses, although only selected ones of those are utilized, as explained below.

1.3.5.3. *Multiplicand Selector*

There is a left hand multiplicand selector M40 and a right hand multiplicand selector M42 for selecting respectively the proper left hand and right hand partial products. These products are fed into these selectors through lines M20, M21, etc., and M30, M31, etc., which lead to respective horizontal busses in the multiplicand selectors, said busses being associated respectively with the same numbers as those in the function table from which the products come. In the left hand selector M40 we show only busses for numbers 2, 6, 7 and 8; and in the right hand selector for numbers 1, 6, 8 and 9, but it will be understood that in a complete selector all of the missing digits will also be represented by suitable bus bars and gates. Considering only the left hand selector, it will be noted that each horizontal bus bar leads to a horizontal row of gates. As these gates are arranged in rectangular formation they provide vertical rows as well as horizontal rows. These vertical rows represent digit places in the same manner as do vertical rows M1, M2, and M3 of multiplier accumulator M10; and are respectively associated with the leads from static cable M44 from like stages of the Multiplicand accumulator. The right hand vertical row M46 represents the units places; the one to its left, M48, represents tens places; M50 represents the hundreds place, etc. Since it is assumed in our example that the multiplicand is 168, in units column M46 the gate corresponding to number 8 will be energized; in the tens column M48 the gate corresponding to number 6 is energized (this is represented by darkening the square corresponding to the gate); in column M50 there is no gate corresponding to 1 because the left hand partial product resulting from the multiplication of any digit by 1 is less than 10 and therefore does not have a left hand partial product, so that no horizontal bus (or horizontal row of gates) is needed for 1 in the left hand partial products selector.

The right hand multiplicand selector is of the same construction as the left hand one, and is electrically associated with the right hand permanent function table M16 on the same principle as that involved in the association of the left hand multiplicand selector with the left hand table M14. The vertical bar groups 1, 6 and 8, shown, of those from 1 to 9, are connected by resistors R to the horizontal bars from the multiplier selector M10, but in a different relation, designed to produce the right hand partial products of the same multiplications from which the left hand partial products are derived in the table M14. Also this selector is set up with gates to hold the digit 1 as well as the remaining digits, and the whole multiplicand is set on the gates of this selector as shown.

The multiplicand remains the same throughout the multiplication while it is successively multiplied by respective digits of the multiplier; therefore, the same gates in both multiplicand selectors remain conditioned throughout the multiplication, in this case, at least three addition times, and possibly more, depending on the manner in which the multiplication set up is cleared.

Reverting again to the condition when stage 1 of counter M4 is energized, we have seen that conductors M20 to M23 will transmit respectively 0, 1, 2, and 2' pulses to the horizontal busses of the selector M40 associated with numbers 2, 6, 7 and 8 respectively. Considering vertical units row M46 first, we note that only the gate corresponding to number 8 is conditioned. This gate is also associated with line M23 which, as we previously noted, will pass 2 pulses during this addition time. These 2 pulses will therefore pass down conductor M56 which thus transmits the correct left hand partial product resulting from the multiplication of 3 and 8 (see Example 12). In the right hand selector the horizontal bus corresponding to number 8 passes 4 pulses during this addition time. These pulses are transmitted only to the number 8 gate of the vertical units column and thence are transmitted to line M64. These 4 pulses represent the right hand partial product of preceding Example 12.

In this fashion, during this addition time the lines leading from the left and right hand selectors M40 and M42 will transmit the correct number of pulses representing the left and right hand partial products resulting from the multiplication of 168×3 as shown in Example 13. During the next addition time stage 2 of stepping counter M4 will be energized, which will activate horizontal bus 4, representing the second digit of number 342 and therefore the vertical busses corresponding to the proper partial products of 168×4 will be energized so that conductors M56 to M68 will carry the second horizontal rows of partial products shown in Example 14. During a third addition time the partial products of 168×2 will similarly be transmitted (due to stepping of counter M4 to its third stage), so as to repre-

sent the third horizontal rows of partial products in Example 14.

1.3.5.4. *Multiplication Shifter*

It will be noted that in the example the second horizontal row of partial products is shifted over one place to the right, and the third row shifted another place to the right. Means must be provided for correspondingly shifting the partial products in our multiplier. To accomplish this we provide left and right hand shifters M80 and M82 respectively. These consist of a rectangular arrangement of gates of which the horizontal rows correspond to addition times 1, 2 and 3 of counter M4 while the vertical rows are conditioned during each addition time by a number of pulses for each row corresponding to the respective digits of the left and right hand partial products as emitted by corresponding vertical rows of gates in selectors M40–M42 in the manner previously described. The outputs of the respective gates of the shifters are not connected in vertical or horizontal rows as heretofore, but in the shifter they are connected in diagonal parallel rows as shown in the drawing.

Each of the gates in the shifters M80 and M82 is of the type shown in FIGURE 6, and comprises an electronic valve having a pair of separate input circuits connected with independent control grids and jointly influencing the flow of current to a common anode. The left hand shifter array is made up of the gates M801–M812, inclusive, while the right hand shifter comprises the gates M820–M828, inclusive.

In the left hand shifter M80, the gates M801, M802, M803 and M804 constitute the first horizontal row, each gate having one of its two inputs excited from stage 1 of the counter M4. The second horizontal row is made up of the gates M805, M806, M807 and M808, each having one of its two inputs excited from stage 2 of the counter M4. The gates M809, M810, M811 and M812, each having one of its two input grids excited from stage 3 of the counter M4, constitute the third horizontal row. The gates M801, M805, M809 with their second input grids connected in common to the line M62 make up a first vertical row in the shifting array; the gates M802, M806, and M810 have their second input grids connected in common to the line M60 to constitute a second vertical row; the gates M803, M807, M811 with their second input grids connected in common to the line M58 make up a third vertical row; and the gates M804, M808 and M812 make up the fourth vertical row of the left hand shifter array.

The anode of gate M801 feeds the left hand shifter lead 7 to the product accumulator, while the anodes of the gates M802 and M805 feed left hand shifter lead 6. The left hand shifter lead 5 is linked to the anodes of the gates M803, M806 and M809, and the left hand shifter lead 4 is connected with the anodes of the gates M804, M807 and M810. Excitation for the left hand shifter lead 3 is derived from the anodes of the gates M808 and M811, which excitation for the left hand shifter lead 2 comes from the anode of the gate M812.

The right hand shifter array M82 is made up of similar gates arranged in like manner, but connected to excite the right hand product accumulator. The first horizontal row in the right hand shifter array is made up of the gates M820, M821 and M822 with one input grid of each excited in common from the first stage of the counter M4, while the second horizontal row includes the gates M823, M824 and M825 each having one of its input grids excited in common from stage 2 of the counter M4. The stage 3 of the counter excites one input grid of each of the gates M826, M827 and M828 constituting the third horizontal row of gates.

The second input grids of the gates M820, M823, M826 are connected in common to the line M68 and form a first vertical row of gates, a second vertical row of gates being made up of the gates M821, M824, M827 having their second grids excited in common from the line M66, while a third vertical row consists of the gates M822, M825 and M828 with their second input grids connected in common to the line M64.

The right hand shifter lead 5 to the product accumulator is fed from the anode of the gate M820, and the right hand shifter lead 4 to the product accumulator receives signals from the anodes of the gates M821 and M823. The anodes of the gates M822, M824, and M826 are linked to the right hand shifter lead 3 to the product accumulator, while the anodes of the gates M825 and M827 drive the right hand shifter lead 2 to the product accumulator. The right hand shifter lead 1 to the product accumulator is connected with the anode of the gate M828.

Considering again the addition time during which number 168 is multiplied by 3, we have shown how as a result of this operation the vertical leads of left hand multiplicand accumulator M40 will transmit during this addition time to left hand shifter M80 the following numbers of pulses on leads indicated in the left column, and the lines on which these will leave the shifter are shown in the right hand column.

(15)

[Left hand shifter (addition time 1)]

Lead	Pulses	Out on Shifter lead
M62	0	7
M60	0	6
M58	1	5
M56	2	4

Since only the lowermost shown horizontal row 1 of gates in the shifter is energized during this addition time, these pulses will be emitted only on the respective diagonal leads of the shifter which are connected at this time to the gates of horizontal row 1. As shown by the above Table 15, no pulses will be emitted on diagonal lead 7 of the shifter at this time because no pulse comes in on lead M62 at this time. The same is true for diagonal lead 6. On diagonal lead 5, 1 pulse will be emitted because, as previously shown, 1 pulse is transmitted to lead M58 by the left hand multiplicand selector during this addition time. Similarly 2 pulses are emitted on diagonal lead 4 of shifter M80. At the same time right hand shifter M82 is receiving the right hand partial products corresponding to 3 times 168 from leads M64 to M68. These, as previously shown, are as follows:

(16)

[Right hand shifter (addition time 1)]

Lead	Pulses	Out on Shifter lead
M68	3	5
M66	8	4
M64	4	3

All of these pulses are transmitted to the appropriate decades of suitable accumulators associated with the respective shifters. During the second addition time, multiplication of 4×168 is performed and sets of pulses are correspondingly transmitted to the left and right hand shifters as represented on the following table:

(17)

Left hand shifter (addition time 2)			Right hand shifter (addition time 2)		
Lead	Pulses	Out on Shifter lead	Lead	Pulses	Out on Shifter lead
M62	0	6	M68	4	4
M60	0	5	M66	4	3
M58	2	4	M64	2	2
M56	3	3			

It will be noted that because horizontal row 2 of the shifters is activated during this addition time the number transmitted down each vertical lead of the shifter is emitted not on the same diagonal lead as before, but shifted over one place to the right. For example, on the right hand shifter, considering lead M64, during the first addition time 4 pulses were transmitted down this lead, out through the lowermost gate to which lead M64 is connected and thus to diagonal lead 3 of the shifter. During the second addition time 2 pulses are transmitted down lead M64 to the second gate from the bottom (since horizontal row 2 is activated) and out on diagonal lead 2 of the shifter, which at its terminal part is located one position further to the right than the lead to which the digit pulse first transmitted from M64 was delivered. By referring to Example 14, it will be seen that this is exactly what is required for proper addition of the right hand digit of the right hand partial product in order to comply with the procedure shown in the example; namely, the digit in the lower horizontal row has been shifted over one place. In similar fashion, every succeeding digit from M64 is shifted one place to the right each addition time. It will also be noted that when the sums of the left hand partial product and right hand partial product as emitted by the 2 shifters are added, the left hand sum should be shifted one place to the left under the right hand partial product, and thus be multiplied by 10. This is accomplished very simply by combining the output of the leads of shifter M89 with the outputs of leads of the same numbering from M82, as will be more fully shown in the detailed description of the high speed multiplier.

The leads from the shifters M89 and M82 are numbered consecutively and lead to decades of the same order in the product accumulator not shown in FIGURE 17. By omission of use of a lead number 1 from the left hand shifter, and always transmitting the left hand partial product so that its rightmost digit is carried on the No. 2 lead, when this partial product is transmitted to the product accumulator over leads as numbered to decades of corresponding number, the whole partial product is one place to the left of the unit decade in the accumulator with the equivalence of multiplication by ten.

For the present, it is sufficient to state that the leads from the two shifters as numbered are connected to the digit inputs of two accumulators, and the partial products are added in these accumulators, as received, in the fashion previously described for accumulators.

When one or both of the factors of the multiplication is a negative number, it is represented in the ENIAC by its tens complement, and the product will issue as a tens complement if it is a negative number, as will be explained later in the detailed description of the high speed multiplier.

1.3.6. *Elementary Division*

1.3.6. *Process Employed*

In the ENIAC, division is performed by successive subtraction. We shall first consider a very simple example:

$$\frac{36}{3}=12 \tag{18}$$

This could be performed by subtracting the quantity 3 from 36, then again from the remainder, 33, etc., and adding one unit in the quotient each time such subtraction is performed. Twelve such subtractions would then reduce the numerator remainder to zero, and the answer would thus be 12.

To reduce this labor we could multiply the denominator, 3, by 10, and subtract the product 30, from the numerator 36, noting the quantity 10 in the quotient; the remainder is 6, and from this we subtract 3 two more times to reduce the remainder to zero, adding one unit

to the quantity for each subtraction to give the total quotient, 12 as shown below:

(19)

$$\begin{array}{l} \overset{(a)\ (b)\ (c)}{10+1+1=12} \\ 3\overline{)36} \\ \quad 30\,(a) \\ \quad\overline{\quad 6} \\ \quad\ \ 3\,(b) \\ \quad\overline{\quad 3} \\ \quad\ \ 3\,(c) \\ \quad\overline{\quad 0} \end{array}$$

This is essentially the method employed in the ENIAC, except for one thing: the ENIAC does not know when to stop subtracting 30, unless it has produced an overdraft, by subtracting 30 from a remainder which is less than 30, so that the sign of the remainder changes after this subtraction is performed. When this occurs, the change in sign of the numerator remainder from plus to minus (or from minus to plus in some cases) is shown on the PM circuit of the ENIAC as a change from P to M, and this signal can be used to shift the remainder over one place. However, the partial quotient is now too large, so instead of subtracting the denominator term in the subsequent operations, we add it, and for each addition subtract one unit in the next decade place of the quotient as shown below:

(20)

$$\begin{array}{l} \overset{(a)\ (b)\ (c)\ (d)\ (e)\ (f)\ (g)\ (h)\ (i)\ (j)}{10+10-1-1-1-1-1-1-1-1=20-8=12} \\ 3\overline{)36} \\ \quad -30\,(a) \\ \quad\overline{\quad\ 6} \\ \quad -30\,(b) \\ \quad\overline{\quad -24} \\ \quad\ +3\,(c) \\ \quad\overline{\quad -21} \\ \quad\ +3\,(d) \\ \quad\overline{\quad -18} \\ \quad\ +3\,(e) \\ \quad\overline{\quad -15} \\ \quad\ +3\,(f) \\ \quad\overline{\quad -12} \\ \quad\ +3\,(g) \\ \quad\overline{\quad\ -9} \\ \quad\ +3\,(h) \\ \quad\overline{\quad\ -6} \\ \quad\ +3\,(i) \\ \quad\overline{\quad\ -3} \\ \quad\ +3\,(j) \\ \quad\overline{\quad\ 0} \end{array}$$

Conversely, if the numerator is negative instead of positive, we would begin with the addition process as shown below:

(21)

$$\begin{array}{l} \overset{(2)\ (b)\ (c)\ (d)}{-10-10+1+1\ \text{etc.}=-20+8=-12} \\ 3\overline{)-36} \\ \quad 30\,(a) \\ \quad\overline{\quad -6} \\ \quad 30\,(b) \\ \quad\overline{\quad\ 24} \\ \quad -3\,(c) \\ \quad\overline{\quad\ 21} \\ \quad -3\,(d) \\ \quad\overline{\quad \text{etc.}} \end{array}$$

Actually, in the ENIAC, the numerator in Example 20 might be represented by P0036 (the extra decimal places are not shown for the sake of simplicity); the denominator would then be M9970 (representing the quantity −30 in step (*a*)); and the numbers which may

appear in the ENIAC in the course of computing Example 20 are given below:

(22)

(a) (b) (c) (d–j)

P0010 + P0010 + M9999 + M(9999×7) = P0020 + M9992 = P0012 (Ans.)

P0036
M9970 (a)

P0006

M9970 (b')

M9976 ---------- M9760 (b)

P0240 ---------- M9760

(A)		(B)	
M9970 (c)		P0030 (c)	
P0210		M9790	
M9970 (d)		P0030 (d)	
P0180		M9820	
M9970 (e)		P0030 (e)	
		M9850	

---------- (same operation 4 more times) ----------

P0030	M9970
M9970 (j)	P0030 (j)
P0000	P0000

NOTE.—In step (*b'*) the numerator remainder is shifted over one decimal place to the left (i.e., multiplied by ten) in a 'Shift" accumulator and then the complement of this quantity is returned to the numerator accumulator as shown in step (*c*) of column (A). This is obviously exactly equivalent to shifting the denominator one place to the right and changing its sign, as was done in step (*c*) of Example 20. The operation may be performed in the above manner in the ENIAC if it is more convenient to leave the denominator quantity unchanged; or it may be performed as shown in column (B) above if the sign of the shifted numerator remainder is not changed, in which case the denominator sign must be changed. The following examples of elementary machines will show, in FIG. 18, the method of column (A), and in FIG. 19 the method of column (B).

1.3.6.2. *Elementary Divider—Positive Quantities Only*

FIGURE 18 is a highly simplified and schematic showing of a divider using the basic principles employed in the ENIAC but capable of handling positive quantities only.

For this purpose 4 standard accumulators are required—one each for the numerator (B1), denominator (B2), quotient (B3) and a shift accumulator (B4) whose function is to shift the numerator remainder over one place (that is multiply it by 10) whenever an overdraft occurs. The first, second and fourth accumulators are shown connected by a digit tray B5 containing a conductor for each digit and one for the PM sign (as is standard for the ENIAC); however, the cable from the digit tray to the "receive terminal" of the shift accumulator (B4) (shown as the alpha terminal), contains a shifter B34, that is, each lead of the digit tray is connected by the shifter to the next higher lead of the alpha terminal, so that the quantity received from the digit tray is in effect multiplied by 10 as it enters the shift accumulator and is registered there as 10 times the quantity transmitted to the digit tray by the numerator accumulator B1.

Referring to FIGURE 18 is a program pulse for initiating division is received at terminal B6 and is conducted to transceiver B8 on lead B10. The program pulse also passes directly along lead B12 to quotient place ring B14 to move this from the normal off position to place 1. The program pulse also passes to a receiver B15 which initiates the first operation; namely, the one corresponding to step (*a*) in Example 19.

It is assumed that at the beginning of the division operation the numerator accumulator B1 contains the numerator; for example, the number 36 and the denominator accumulator B2 is assumed to carry the denominator multiplied by the proper power of 10 so that the first subtraction will be the correct magnitude. For example, as the denominator is 3 and the numerator is 36, the denominator will carry the quantity 30 instead of 3. It will be explained later how the correct settings for the initial subtraction steps are obtained in practice.

To continue with FIGURE 18, the arrival of the initial program pulse at receiver B15 simultaneously conditions the numerator accumulator B1 on line B18 to receive, and the denominator accumulator B2 on line B20 to transmit subtractively. This will perform the operation of stage (*a*) in Example 20 and will leave a remainder of 6 in the numerator accumulator. At the same time quotient accumulator B3 has been conditioned on line B22 to receive, by transmitting an appropriate signal from terminal Q-alpha of B15 and another signal has been transmitted on line B24 to gate a 1P pulse through the gate controlled by stage 1 of the quotient place ring out along quotient cable B26 which connects each place of the place ring B14 to the corresponding decade of the quotient accumulator B3, to register the digit 1 in the suitable decade place of the quotient accumulator. Thus the first subtraction corresponding to place (*a*) of Example 20 has been performed and the quantity corresponding to 10 has been registered in the quotient accumulator. As there is nothing to stop it, the same operation will be performed during the next addition time of the division, and the operation corresponding to stage (*b*) of Example 20 will be performed in the same fashion as described above. However, this time there is a difference in that the numerator remainder now changes from positive to negative (corresponding to quantity minus 24 in Example 20(*c*)). This produces a signal of the static PM output B28 of accumulator B1 which gates a CPP through gate B30 to reset receiver B15 and to stimulate receiver B32. Receiver B32 now conditions accumulator B1 through line B36 to transmit the numerator remainder (minus 24) additively and simultaneously through line B5. B37 conditions the shift accumulator B4 to receive on its alpha circuit through shifter B34 whereby it receives the numerator remainder multiplied by 10.

Energization of line B35 also sets flip-flop B39, which gates a CPP through B38. This is passed through a suitable delay line B41 to the upper half of receiver B32; due to this delay the CPP arrives just after a CPP from B43 has reset the lower half of B32, and sets the upper half so that the next addition time after the shift accumulator receives the numerator contents, it is stimulated to return them to the numerator, properly shifted, by transmitting subtractively due to stimulation of line B40.

It is thus shown how after an overdraft the numerator remainder sign can be changed and the numerator remainder can be shifted one place to the left relative to the denominator as required in the performance of step (*c*) of Example 21 or 22.

In order to provide the correct quotient value when the overdraft occurs, stimulation of line B40 is caused through line B44 to gate a CPP through gate B46 and normally open gate B47 to produce a pulse on line B48 to advance the quotient place ring one place which will correspond to place (*c*) in Example 20 and at the same time stimulate receiver B15 to cause a repetition of the operation initially, described. Since an overdraft has occurred, the sign of the digit added in place (*c*) of the example must be different from the sign of the digit in place (*b*). This is accomplished by transmitting the 10's complement. The manner in which this is done will be described in detail in the next example. At this point it will be sufficient to say that transmittal of a CPP through gate B45 is also utilized to produce the 10's complement of the desired quotient place digit instead

of the digit itself, so that the quantity is subtracted instead of being added.

This procedure will then be repeated until the last place in the quotient place ring is reached. This time line B52 will be stimulated to block gate B47 and also to permit the CPP from gate B46 on line B54 to pass through to line B56 to both clear the numerator ring to zero and reset transceiver B8 and cause it to emit the next program pulse on line B58.

The above description is obviously superficial and schematic and is intended only to illustrate the general mode of operation employed in division rather than to depict a complete and operative device in any sense. The following section will describe a schematic but more complete unit to illustrate the manner in which division of quantities which may have different signs is performed. Finally, in a later section a full and complete description of the divider used in the ENIAC will be given. This will include features enabling selection of the desired number of decade places employed, round-off of the last significant figure, interlock with other arithmetical units, and other features useful or necessary to the operation of a practical device.

1.3.6.3. *Elementary Divider—Signed Quantities*

FIGURE 19 is a schematic drawing showing the manner in which division of signed numbers can be performed. It must be kept in mind of course that a negative quantity is always represented in the ENIAC by its 10's complement during the process of computation. In FIGURE 19 the same four standard accumulators are used as in the previous example. These are represented by blocks G42, G44, G46 and G48 for the quotient accumulator, numerator accumulator, denominator accumulator and shift accumulator respectively. The numerator and denominator contents are assumed to be correctly set up in their accumulators.

A program pulse enters on line G1 and is transmitted to transceiver G2 and to line G3. This pulse is used to initiate a number of events in the divider. It excites gate G6 to transmit a signal to numerator ring G12 if the contents of the numerator are negative. The conditioning potential for G6 is transmitted along one conductor of static cable G10 from the PM counter of this accumulator so that if the contents of the accumulator are negative, the numerator ring G12 will be stepped and the output of H2 will become positive. The initiating pulse similarly is gated through G7 if the denominator contents are negative to set the flip-flop G11 and reverse the polarity of its outputs to G17 and G18. These operations determine whether the denominator contents are to be transmitted additively or subtractively to the numerator for the initial difference step. The initiating pulse also sets flip-flop G13, which passes a CPP the following addition time to line G50 to set the flip-flop G8 to stimulate the numerator accumulator to receive the contents of the denominator accumulator for performance of the first step; this pulse also passes along line G50 to the correct one of gates G35 or G36 to stimulate either additive or subtractive transmission of the aforementioned denominator contents in accordance with the correct sign determination, as will be explained below.

If the numerator contents are negative, ring G12 has been stepped and the static line G14 is stimulated positively; if the numerator is positive the ring has not been stepped and static line G15 is correspondingly stimulated. At the same time line G17 or G18 is stimulated positively depending on the sign of the denominator as previously explained. These sets of static lines are associated with a sign indicating matrix composed of four gates G27, G28, G29, and G30. Only one of these gates will be stimulated to conduct by both of its grids associated with the numerator and denominator lines. We have four possible situations for the matrix:

(23)

N sign	D sign	Matrix Gate on—
+	+	G30
+	−	G29
−	+	G28
−	−	G27

From the above chart and FIG. 19 it can be seen that when the numerator and denominator signs are alike, line G32 is energized negatively and when the signs are unlike line G33 is so energized; this in turn allows only G35 or G36 respectively to pass a pulse from line G50 to receiver G40 to energize either terminal D_S for subtractive transmission or terminal D_A for additive transmission of the denominator contents. Both of these terminals are connected through conductors of static cable G41 to denominator accumulator G46. It should be noted that in accordance with Examples 20 and 21, if the numerator and demoniator signs are like, it is necessary to transmit subtractively; and if unlike, to transmit additively. This is true in Example 22 where the denominator is transmitted subtractively in step (*a*) and is equally true if the denominator is negative and the numerator positive, in which case additive transmission of the negative denominator results in a remainder which is the *difference* of the numerator term and the denominator term. It is thus seen that the sign indicating matrix results in the correct transmission from the denominator accumulator.

The same pulse which causes the denominator to transmit additively or subtractively (D_A or D_S on G40) is transmitted from line G50 to the add-subtract flip-flop, G8, to condition the numerator accumulator to receive, which is done by a signal transmitted from terminal $N\gamma$, of flip-flop G8 on one conductor of static cable G10. Thus the quantity transmitted by one denominator will be conducted on digit tray G57 through the γ receive circuit of numerator accumulator G44. This transmission will take place during the second addition time.

We shall now consider the matrix consisting of gates G22, G23, G24 and G25, which is the overdraft matrix and which is fed in part by the output of the numerator ring G12 just like the sign indicating matrix, and in part by the static output of the PM ring in the numerator accumulator G44. When the PM sign of the numerator (or its remainder) changes indicating an overdraft, the potential on lines G37 and G38 is reversed causing a different gate of the matrix to conduct, since the signal received from the numerator ring has not changed at this time. This changes the stimulation from the NO (no overdraft) line to the O (overdraft) line. After the overdraft circuit is so stimulated, one consequence will be that the numerator ring G12 is changed (by a CPP through gate G26 as is explained below) so that for the next following subtraction step (of denominator from numerator remainder) the matrix will again signal no overdraft (NO) and will remain in this position until another overdraft occurs. It is thus seen that the overdraft matrix compares the current sign indication of the contents of the numerator accumulator (over the static PM leads) with the sign of the contents of the numerator resulting from the previous subtraction (which is given by the numerator ring G12). Whenever these signs differ, an overdraft has occurred, and the circuit reacts accordingly, as explained above.

During the time that step (*a*) of our division is being performed by the action indicated above, the first digit must be inserted into the quotient accumulator in the proper decade place and bearing the proper sign. To accomplish this the quotient accumulator is conditioned to receive its first digit. This is performed by the second

output of the flip-flop G8, which gates a CPP through gate G9 to receiver G51 whose output terminal Q_γ is now energized through static line G53 to condition the quotient accumulator G42 to receive on its γ digit input terminal, which receives the appropriate quotient increments (of either sign) through cable G72' from terminal G72. At the same time the second output of receiver G51 is utilized on line G52 to condition gates G54 and G55. If the current addition or subtraction did not produce an overdraft, gate G54 will be opened and gate G61 will be conditioned by inverter G56 to pass a CPP to initiate the next add-subtract cycle. This CPP goes out on line G50 to set G85, G35 or G36 as previously described. If there has been an overdraft, then gate G55 conducts, starting a shift cycle. Note that gate G55 and G56 are normally open and are closed by a signal on their respective lines, so that the signal from line G52 will *not* pass through the gate which is stimulated.

We have thus shown how the add-subtract cycle is established and is repeated by a pulse through gate G61' during successive addition times until an overdraft occurs, when a shift signal is transmitted through gate G55 to initiate a shift as will be shown below.

When an overdraft occurs, the signal through gate G55 conditions gate G58 to pass a CPP to line G59 which stimulates receiver G60, one terminal (N) of which stimulates line G80 to open gate G26 to pass a CPP to cycle the numerator ring G12, as was previously explained; it also (on terminal N_A) conditions the numerator accumulator G44 to transmit, and (on terminal S_a) the shift accumulator (on line G57) to receive the number transmitted from G44. After transmitting its contents, the numerator accumulator G44 is cleared by the clear signal from terminal NC of G60 so that it will be ready to receive the shifted complement of the value which it transmits to the shift accumulator, as in step (*c*) of Example 22. The signal from the numerator terminal (N) of G60 also passes down line G80 to open gate G16 which permits the next 1'P pulse from gate G5 to advance the quotient place ring G64, which must be done each time there is an overdraft, as shown by Examples 19 through 22; gate G5 is open to pass this 1'P because the initial pulse which was transmitted along line G3 also set the transceiver G2, to stimulate line G4, which opens gate G5.

The potential on line G80 also opens gate G63 to pass a CPP to set receiver G43. This conditions three of the four output lines from G43 to stimulate the shift accumulator G48 to transmit additively and then clear, while the numerator accumulator is conditioned to receive the transmitted quantity as will be apparent from inspection of the drawing. The shift accumulator is made to transmit additively in this case instead of subtractively as in FIG. 18 because the overdraft which initiated the shift also caused the numerator ring to cycle, as previously explained, and this reversed the polarity of line G14 and G15, which changed the output of receiver G40 to change the sign of transmission from the denominator receiver. Since the sign of the denominator has been thus changed on overdraft, it is not necessary in this case to change the sign of the numerator. The fourth output line, G47, from receiver G43 opens gate G85 to admit a CPP from gate G79; this latter gate is opened by a static potential from line G4, as long as the transceiver G2 remains set.

The CPP from gate G85 passes up line G50 to set flip-flop G8 and pass either gate G35 or gate G36 each addition time, just as did the CPP's from gate G61 when gate G54 was open. Note that flip-flop G8 and receiver G40 are reset immediately after functioning so that a new CPP is required each time they are to operate.

Setting of flip-flop G8 as above described starts the add-subtract cycle again. This is proper since the events which are called for after an overdraft have now occurred; namely, shifting of the numerator remainder one decimal place, together with a change in sign of the denominator so that the subsequent algebraic addition of numerator remainder and denominator is in accordance with Example 22–B.

It will be seen that the above described operations will continue, with the quotient ring advancing one step toward units place with each overdraft, until the division has been performed and is terminated as will be described below.

The initial pulse which was transmitted along line G3 set transceiver G2 to stimulate line G4 and pass a 1'P through gate G5 each addition time to cycle quotient place ring G64 if gate G16 is open. It is assumed that we start the division process with the quotient ring G64 in place 1. Each time that a subtraction is performed from the numerator remainder (e.g., in steps (*a*) and (*b*) of Example 22), it is desired to add or subtract one unit in the proper decade place of the quotient accumulator G42. This is accomplished by means of a CPP passing through gate G65 or G66, depending on whether the signs of the numerator and denominator are like or unlike; if they are like, the +1 line G68 is stimulated to pass a 1P through gate G69 which passes down line G70, through the gate G71 which is associated with the energized stage of ring G64 (in this case stage 1), and out on the associated line of digit cable G72 (in this case line 9). All the other output lines of G72 will carry no pulses, so the quotient, after the first addition time will carry P0100 . . . to as many places as there are active stages of the quotient place ring. Each addition time thereafter, another digit pulse will be added to the same decade place of the quotient accumulator, until an overdraft occurs, when a new sequence of events is initiated by stimulation of line G80. This permits a 1'P to pass through gate G16 to step the quotient place ring one step. At this time, the numerator ring G12 also responds to the change in sign of the overdraft to cause the sign indication matrix to stimulate that one of lines G32 or G33 which was not previously stimulated, thereby changing the actuation as between the +1 line G68 and −1 line G67. Assuming the +1 line was previously actuated, the −1 line G67 is now actuated to produce successive subtractions in the next stage of the quotient accumulator until the overdraft is wiped out. These subtractions are produced, as in all ENIAC subtraction, by addition of the 10's complement. This is done as follows: stimulation of line G67 causes gates G73, G74 and G75 to pass 2P, 2'P, and 4P respectively to the energized gate G71 of the quotient place ring G64, and thus pass 8 pulses down the energized line of cable G72 whose number corresponds to the active stage of the place ring G64. All of the other gates G71 of the ring, not being energized, do not pass the 8 pulses, but in these stages the gates G81 are stimulated so that they will pass the 9P from line G83, G84 to each place conductor except the one whose number corresponds to the active stage.

In Example 20, let us assume that we are at step (*c*), in which case the quotient accumulator contains the value P0200 . . . , which was produced as the result of steps (*a*) and (*b*); we wish to add the quantity −0010, representing the number −1; this will be added in the quotient accumulator first as M9989 . . . corresponding to the action described in the previous paragraph; one pulse time later the 1'P is gated through G76, down line G82 to the last decade place on the right, to change the total transmitted during this addition time to: M9990 . . . which represents the number −0010 . . . . This value added to P0200 . . . gives P0190 . . . and the same operation repeated seven more times, or until the remainder is zero, will give P0120 . . . which is the desired answer.

Cable G86 is shown with conductors leading to stages 3, 5, 7 and 9 of the place ring, for the purpose of terminating the computation at any desired one of these stages. By setting switch G87 at the desired number, when that stage of the ring is reached, a signal will be transmitted from that stage through switch G87 to the transceiver G2. As will be shown in detail in the description of the full

divider, this signal can be made to clear the transceiver and at the same time send out a program pulse on line G88 to initiate the next desired operation; while removing the signal from line G4 will serve, through inverter G91 to clear the place ring, by a "clear" pulse on line G92; a similar pulse on line G93 will reset the units G12 and G11 so that the divider will be ready to perform another division.

1.3.6.4. *Square-Rooting—Process Employed*

Square rooting in the ENIAC is performed by a process very similar to that used in division as explained in 1.3.6.1, namely, the use of successive subtraction, except that the quantity subtracted from the square remainder is increased by two at each subtraction.

Let us first consider the following table:

(A)

(1) n	(2) $(2n+1)$	(3) difference $(2n+1)-(2(n+1)+1)$	(4) n^2
0	1	2	0
1	3	2	1
2	5	2	4
3	7	2	9
4	9	2	16
5	11	2	25
n	$2n+1$	2	n^2

Since $(n+1)^2=n^2+2n+1$, it is obvious that, beginning with the number 1, whose square is also 1, we can build up the square of each succeeding digit by finding $2n+1$, which for each successive digit is done by adding the number 2 to the preceding number in column (2) above. This results from the fact that for any two successive digits, n and $n+1$, the difference of the value in column (2) will be $2(n+1)+1-(2n+1)=2n+2+1-2n-1=2$. Having thus obtained the value 3 for $2n+1$ where $n=1$, we add this to n^2 (or 1) which we have from the preceding step, and get 4 for the square of 2 (or $n+1$). In the same way we can build up the square of any digit by successive steps.

It will be obvious from the above, that if, conversely, we subtract from any quantity, first a single unit, then from the remainder three, then 5, etc., corresponding to the successive values of $(2n+1)$ in column (2) of Example A, then we are subtracting a function of the square root of the original number. For example, consider the number 16:

(B)

16
−1 (1)
15
−3 (2)
12
−5 (3)
7
−7 (4)
0

It is thus seen that 4 steps (corresponding to $n=4$) reduces the minuend to zero corresponding to the statement that the square root of 16 is 4 with no remainder. If the original number were 17 instead of 16, it is obvious that there would be a remainder of one unit, indicating that a larger number than 4 is the square root of 17.

The remainder can be evaluated decimally by shifting over one place to the left and utilizing the fact that

$$(n+.1)^2=n^2+\frac{2n}{10}+\frac{1}{100}$$

and

$$(n+.01)^2=n^2+\frac{2n}{100}+\frac{1}{1000}$$

etc., as will be apparent from the following example:

(C)

17.89
−1.00 (1)
16.89
−3.00 (2)
13.89
−5.00 (3)
8.89
−7.00 (4) $=n$, therefore $\frac{2\times4}{10}=.8$, $+.01=.81$
1.89
−0.81 (4.1)
1.08
−.83 (4.2) $=n$, therefore $\frac{2\times41}{100}$ $n=.084+.0001=.0841$
.2500
−.0841 (4.21)
.1659
−.0843 (4.22)
.081600
−.008441 (4.221)
.073159
.008443 (4.222), etc.

For practical reasons which will be more readily understood when the detailed square-rooter is described, the ENIAC actually performs its operations not as shown in Example C, but as in Example D below. In this process, odd numbers successively increasing (and accumulated in a separate answer accumulator) are subtracted from the decreasing remainder in the radicand accumulator until an overdraft occurs. The radicand remainder is then shifted, as in division, relative to the subtrahend, which is now successively added in the form of odd numbers successively decreasing, until another overdraft occurs. This process produces twice the square root, since the answer is altered by two units after each addition or subtraction occurs. The shift sequence also provides for the subtraction or addition respectively of one unit first in the highest decade place and then in each decade place to the right just before the shift operation takes place, as will be seen below in finding the square root of 29,241, which is 171.

$\overline{171}^{\,2}=29,241$

(D)

Radicand	Answer $(2n)$	Difference
+29,241	100	+200
−10,000		
+19,241		
−30,000	300	+100
−10,759	(sign changes, so answer accumulator adds one unit in 100's decade place and begins successive subtractions in 10's decade place, while subtrahend is shifted)	
+3,900	400	−10
−06,859	390	−20
+3,700	370	−20
−3,159		
+3,500	350	−10
+0,341	(shift produces 340+1=341, due to sign change, as above)	
341	340	+1
0	341	+1 (due to sign change)
	$342=2n$; $n=171$, Answer	

Since the operation of the square rooter resembles so closely that of the divider, no further explanation of ele-

mentary square rooting will be given at this point, as the reader should now be able to follow the detailed description of the square-rooter in Chapter VI without difficulty.

1.3.7. *Elementary Function Table*

1.3.7.1. *Basic Principles Employed*

The units of the ENIAC so far described are primarily arithmetical units; that is, they perform the ordinary operations of arithmetic such as addition, multiplication, etc., and these units are also provided with a certain amount of programming equipment whereby they can exercise some control over the sequence in which these operations may be performed.

In the course of solving many mathematical problems, it is often necessary, at some intermediate stage of the solution, to refer to previously prepared tables which give the values of some needed function. Common examples of such tables are tables of trigonometric functions (such as sines and tangents), tables of logarithmic functions, etc. Of course, the ENIAC could in many cases be set up to generate the desired function mathematically, instead of looking it up on a table; however, this might often tie up a large number of the computing units of the machine which would be needed elsewhere in the problem. In addition to such transcendental functions, a given problem may require the use of a table of arbitrary functions representing an empirically or experimentally determined relationship for which no mathematical formula is known or readily available. An example of this is the "drag function" in exterior ballistics, which represents the retarding force on a projectile due to air resistance, at various velocities. Particularly in the transsonic region (i.e., near the velocity of sound for a given atmospheric temperature and pressure) this drag force varies in a fashion which is very difficult to portray by formula, but which can be readily plotted and tabulated for the various values of projectile velocity.

The ENIAC is provided with means for storing in tabular form the above types of information, and with programming means whereby any given stored value may be looked up and transmitted to an accumulator or other arithmetical unit for further use. This is called the function table, of which the ENIAC has three. If the problem calls for the drag force exerted on a projectile at a given velocity, and a function table has been set up with the proper values, then, when a number representing the velocity is fed into the function table, it will transmit another number representing the drag force at that velocity.

A general description of the function tables has been given in the introductory part of this specification under the heading of "Memory."

Since each function table can store only about 100 values, it is obvious that the steps between adjacent stored values must be rather wide, as each function value stored by the table corresponds to only two significant figures of the argument. A higher degree of accuracy than this is often required.

Assume that the function table is set up to give values of a function corresponding to the numbers 1 to 100 and we need to know the value of the function corresponding to P67320. We have several alternatives. If the work calls for a low order of accuracy of the function, we can simply take the value corresponding to P67000; that is, look up the value corresponding to 67 on the table. (It is of course assumed that the correct order of magnitude of the function was maintained in setting up the table so that the value for the setting 67 really represents that for the number 67000.)

Now, let us assume, in connection with the above example, the following values of the function table in the neighborhood of argument value P67000.

(24)

Arg. value x		Function value y	
x_0	67	0072500	y_0
x_1	68	0074500	y_1
x_2	69	0076000	y_2

It will be seen that we are thus assuming, in our example, a non-linear relationship, which is the general case.

In the example given, if, for the argument value of 67320, we take instead the value of 67000, the corresponding function value 0072500 will be accurate to within about 1%, which may be sufficient for the purpose. If greater accuracy is required, we must resort to interpolation. The simplest method is linear interpolation (which is most commonly used by engineers and surveyors in interpolating logarithm or sine tables). This consists in utilizing not only function value corresponding to 67, (0072500) but also that corresponding to 68 (or 0074500), finding the difference (0002000) and multiplying it by the desired proportional part of the difference between the table argument value and the desired argument value, or in this case $0002000 \times .320 = 0000640$. This quantity is then added to 0072500.

(25)

0072500
0000640

0073140

which is much more accurate than the value 0072500.

The ENIAC function table can be set up to produce not only the value corresponding to the first two significant figures (as 67 in the example), but also the value corresponding to the next higher setting of the function table (as 68 in the example).

It is possible to interpolate still more accurately by using three argument values from the function table and, in effect, finding the equation of a curve (in practice, a parabola) which will fit the three points, then finding a point on this curve corresponding to the argument desired. For example, assume that the three points are those given in Table 24, we will plot them as shown in FIG. 20.

In so passing a curve through a given number of points, it is easiest to take for $f(x)$, the simplest function of x which satisfies the conditions. In the case where we used two points, this was a line. In the more general case, where n points are used, we may pass a curve through the points such that:

$$y = p_0 + p_1 x + p_2 x^2 + \ldots + p_{n-1} x^{n-1} \tag{26}$$

which is a conveniently simple curve to satisfy the conditions. Of course, the curve grows more complicated as we add points, but in most cases it also grows more accurate as we add points.

For the case where we use three points, the curve becomes a parabola for then the equation reduces to the following form:

$$y = a + bx + cx^2 \tag{27}$$

which is the equation of a parabola.

Referring to FIG. 20, we shall now state the equation of a parabola through any points (xy) in terms of x_0, y_0, and the differences $\Delta y_0 = y_1 - y_0$ and $\Delta^2 y_0 = \Delta y_1 - \Delta y_0$, and the difference (h) between x_0 and x, for the case where Δx (equal to $x_1 - x_0$ or $x_2 - x_1$) is assumed to be constant (as it is in the function table).

$$Y_x = Y_{(x_0 h)} = y_0 + h\Delta y_0 + \frac{h(h-1)}{2}\Delta^2 y_0 \tag{28}$$

This is a well-known equation, whose derivation may be found in any standard text such as Millar's "Higher Math.," Longmans, Green and Company, 1922, page 312 (Equation 7).

It will be noted that Equation 28 is an extension of the interpolation methods previously described. For example, if one point is used,

(29) $y_x=y_0=0072500$

If 2 points are used, we have linear interpolation:

(30)
$$\begin{aligned} y_x &= y_0+h\Delta y_0 \\ &= y_0+h(y_1-y_0) \\ &= y_0\times(1-h)+hy_1 \\ &= 0072500(1-.32)+.32\times 0074500 \\ &= 0049300+0023840 \\ &= 0073140 \end{aligned}$$

which checks with Example 25.

An equation of the form of Equation 26 can be developed in the following manner by substituting in Equation 28 for the first and second differences $\Delta y_0=y_1-y_0$; $\Delta^2 y_0=(y_2-y_1)-(y_1-y_0)$ in terms of y_0, y_1 y_2:

(31)
$$\begin{aligned} y_x &= y_0+h(y_1-y_0)+\frac{h(h-1)}{2}\times(y_2-2y_1+y_0) \\ &= y_0+y_1\left[h+\frac{h(h-1)}{2}(-2)\right] \\ &\quad -y_0h+y_0\left[\frac{h(h-1)}{2}\right]+y_2\left[\frac{h(h-1)}{2}\right] \\ &= y_0\left[1-h+\frac{h(h-1)}{2}\right]+y_1[h-h(h-1)]+y_2\left[\frac{h(h-1)}{2}\right] \end{aligned}$$

(32)
$$= y_0\left[\frac{(h-1)(h-2)}{2}\right]-y_1[h(h-2)]+y_2\left[\frac{h(h-1)}{2}\right]$$

The reason for putting the 3-point interpolation equation into the form of Equation 32 is that it shows in simple form the relationship between the three function values (y_0, y_1, y_2) which may readily be obtained from the function table, and the coefficients by which these values are to be multiplied for 3-point interpolation; these coefficients being derived in terms of the known difference between the value of x and (x_0, x_1, x_2). In our example h would be the difference between 67000 and 67320, or in other words, the last three places of the argument. Isolation of these desired digits can be accomplished in the ENIAC by having the digit leads carrying these three numbers (or any other numbers representing h) connected to special adapters.

It must be kept in mind that in carrying out 3-point interpolation, the function table only furnishes the values of y_0, y_1, and y_2 when x_0 is put into it. The value of x_0 in our example is obtained from those digit lines carrying 67, while the digit lines carrying 320 (of the total argument 67320) are used to obtain the coefficients (h, $h-1$, $h-2$) in step (32). The actual arithmetical manipulation needed to carry out step (32) is not performed by the function table, but by properly programming the necessary external accumulators and the high-speed multiplier.

An example of the unit connections and programming necessary to perform two-point (or linear) interpolation will be given later. The programming for 3-point interpolation according to step (32) is similar in principle to that for 2-point interpolation but involves more complicated connections. In the computation of firing tables for ordnance weapons, four-point Lagrangian interpolation may be found useful in order to obtain the required accuracy. It is obvious that by properly programming the ENIAC in accordance with the principles discussed above, any of the well-known methods of interpolation may be employed.

1.3.7.2. *Other Uses of Function Table*

In addition to the above-described uses of the function table, several other uses are possible. They may be used for the storage of any groups of constants which must be introduced into the other parts of the machine at high speed. In problems where the ordinary program controls of the ENIAC are insufficient, it is possible to employ the table as a 104 position program selecting device using its outputs to initiate program circuits rather than feeding the outputs into digit channels. A function table may be used, therefore, to sequence operations, or chains of operations, which may be initiated in sequence or chosen at random depending on the value of the two pulse groups introduced as argument into the table. These pulse groups may be obtained either from the program circuits or from the digit circuits of the machine.

1.3.7.3. *Elementary Function Table*

The following description refers to FIGURE 21 which is a simplified block diagram of a function table employing the same principle as the function table of the ENIAC, but highly simplified to show only those components essential to an understanding of the general mode of operation.

1.3.1.4. *Program Controls*

The program controls are generally indicated in FIGURE 21–A illustrating argument selector.

A program pulse from any suitable external source initiates the operation of the function table by entering on line **T1**, and is conducted to transceiver **T2** and to **T3** where after passing through a suitable inverter **T5** it is conducted to switch **T6**. This switch has two settings for Clear or Not Clear signal, each setting passing the initiating pulse through a suitable pulse transmitter **T7** to either output terminal **T8** or **T9**, one of which may be used with the transmitting accumulator when its argument is to be cleared and the other when the argument is not to be cleared. The initiating pulse is also transmitted on line **T11** or **T12** to set flip-flop **T13**, the slow output of which is used to condition gates **T14**, **T15** and **T16**, **T16**; gate **T16**, **T16** passes a CPP to reset flip-flop **T13** the following addition time; **T14** and **T15** will, in this next addition time, pass two digits corresponding to the argument value x in table (24), for example, 67, which are stored in the argument accumulator, generally as the result of a previous computation. Assuming the argument to be 67, then six pulses will be transmitted during this next addition time on line **T17** and seven pulses will be transmitted at the same time on line **T18**. In addition, one extra pulse will be transmitted to the units ring if operations switch **T19** is set at zero, as shown, so that in this event, the argument ring will be energized at 68 rather than 67. In order to explain this, the operation switch will now be described:

1.3.7.5. *Operation Switch (T19)*

This switch has three positions labeled —1, 0, +1 respectively, and is provided so that when an argument value x, is fed into the function table, the table will emit the function value corresponding to ($x-1$), x, or ($x+1$), depending on the position of the operation switch. This permits three-point interpolation to be performed, as described in the preceding section. If the switch **T19** is set at the —1 position, no extra pulses are transmitted to the units ring, and in this case if the number 67 is received, the argument ring **T21** will register the number 67. The output of the argument ring is wired to table input gates which have 102 terminals which run to 102 function lines, each of which is set for a particular function value y, corresponding to the argument value x received from the argument ring. Each of these terminals is wired, not to the correspondingly numbered place of the argument ring **T21**, but to the next higher number of the argument ring. For example, terminal 67 of the table input gate is connected to place number 68 of the argument ring, terminal 66 to place 67, etc. Thus when the number 67 is entered on the argument ring T21, if the operation switch **T19** is set at —1, then terminal 66 of the table input gates is

energized so that the function corresponding to $x=67-1$ is emitted. Now, if operation switch T19 is set at zero, line T24 has been energized from the slow output of transceiver T2, and this line is connected (through an inverter) to gate T25 to pass a single pulse during the next addition time to the units ring to step it up one more place, so that if 67 is on the argument ring now registers 68 instead of 67. Actually, the one pulse is passed by gate T25 each addition time that transceiver T2 is energized but it can pass gate T27 only when that gate is conditioned and this occurs only during the next addition time after the argument 67 has been received, due to the action of the program ring T31 which will now be described.

1.3.7.6. *Program Ring.*

Ring T31 is shown with five stages (in the ENIAC it has thirteen stages). During the first addition time of operation, when the argument is received from the argument accumulator (not shown), program ring T31 is the stage −2. Toward the end of this time, gate T28 passes a CPP to advance the program ring T31 to stage −1. At this time line T22 is energized to condition gate T27 to pass the extra pulse from gate T25 through to the units ring. Each addition time thereafter the program ring is stepped one stage by a CPP until the ring is cleared back to stage −2 at the conclusion of the function selection, as will be later described.

Returning to the operation switch T19, it will be clear by now that if this switch is set at 1, then two pulses will be added to the argument ring registration, which will now be 69 instead of 67, while terminal 68 of the table input gate will be correspondingly energized.

It must be noted at this point that the elements so far described will not produce three successive function values to give points x_0, y_0, x_1, y_1, and x_2, y_2, but will only give any one of these points, depending on the setting of operation switch T19. To get a second point, another transceiver must be used which will ordinarily be stimulated by a program pulse from transceiver T2 after the first function x_0, y_0 has been transmitted. The ENIAC function table is provided with eleven program controls similar to the one described, each one including the program controls shown, such as transceivers, operation switches, argument C or NC switches, etc., and all program controls being associated with the same program ring T31. To get three successive points x_0, y_0, x_1, y_1 and x_2, y_2 for interpolation, three program controls of the function table must be used, one of which has its operation switch set at −1, the second at zero, and the third at 1 and they must be programmed to emit the desired function values at the proper times.

It will also be noted that the operation switch and connections shown will not give three points required for Example 32, which calls for x, $x+1$ and $x+2$ respectively, but instead, for an argument value x, will give $x-1$, x, and $x+1$. This second arrangement is more generally useful than one for the x, $x+1$, $x+2$, and is here described because it corresponds more closely to the actual arrangement used in the ENIAC. However, it would obviously be a simple matter to provide for x, $x+1$, $x+2$ by connecting each table output gate terminal to the corresponding number of the argument ring, instead of to the next higher one as shown.

1.3.7.7. *Table Input Gates*

It has been noted that the table input gates T22 have 102 terminals connected to 102 busses so that one bus may be energized corresponding to each number registered by the argument ring. Actually, 102 busses are provided instead of 99 to take care of the 1 and −1 condition as bus −1 must be connected to the 0, 0 registration of the argument ring to carry out the described system for 100 places on the function table, which actually provides 3-point interpolation only for numbers 0 to 99. The −1 bus then gives the function for $x-1$ when $x=0$ by being connected to 0, 0 registration, and the 100 bus provides similarly for $x+1$ when $x=99$. The means for accomplishing this are similar to the corresponding selector means described in connection with the multiplier, and consist of 102 gates TG1 to TG100, each acting as a switch for the correspondingly numbered busses TL1 to TL100. In order for a given gate TG– ( ) to be actuated, it is necessary that both its 10's line and its units line be energized. There are eleven of these 10's lines, which come from 10's cable T32, one line (as indicated by the appropriate number) for each place of the 10's ring. There are ten units lines which come from units cable T33 and are also numbered 0 to 9 in each decade place. All the 0's are connected together and to the zero place of the units ring; all of the 1's are likewise connected together and to the 1 place of the units ring, etc., as will be evident from the drawing. When a given number is registered on the argument ring, it will be clear from the drawing that only one outgoing bus will be energized. It will be noted that the associated outgoing busses are numbered −1 to 100 and that these numbers do not correspond to the associated argument number but to the next lower number respectively; the reason for this has been fully explained in the preceding section.

1.3.7.8. *Portable Function Table*

The portable function table, T35, has 102 horizontal busses corresponding to the terminals of the table input gates to which they connect. Only three of these (numbers −1, 67 and 100) are shown in the drawing, but it will be understood that the intervening busses are exactly similar to these three.

Each numbered horizontal bus has three switches, T36, associated therewith, and each of these is a 10-position switch, the positions being numbered from 0 to 9. The vertical columns of switches represent the respective decimal orders. The ENIAC has 12 such columns of digits switches instead of the three shown. With reference to our example, the bus 67 is shown with its switches set at 725, which is the function value (y) we assumed in our Example 27 for argument value (x) of 67. Considering the switches by columns, each digit place of each switch is connected to the corresponding digit place of each other switch in its column, e.g., the nines are all connected together through cable T38 in the hundreds column, and are also connected to the 9 place of the same column of the table output gates T40; the 8's are likewise all interconnected to each other and to the 8 place of the hundreds column, through another lead of cable T38, etc. The same is of course true for the tens column and for the units column. Assuming, then, that the argument ring registration is such that bus T67 is engaged, with the switch setting shown, in the hundreds column, digit line 7 of cable T38 will be engaged. This will make inverter T39 non-conducting and will establish a position point to condition gate T42 to pass seven pulses during the following addition time along line T43, through pulse shaper T44 to the hundreds digit terminal of output digit socket T46. In similar fashion, digit line 2 of the 10's column will at the same time be engaged to condition gate T47 to pass two pulses along tens line T48; and digit line 5 will allow five pulses to pass to unit line T49, thus setting up our function $y=725$ for $x=67$. We also provide a PM switch T51 for each horizontal bus. This can be thrown to the P position to energize the P bus T52 to pass 0P on the PM line T54; or to the M position to pass 9P on line T54, as will be apparent from the drawing. Of course, if the switch is thrown to the M position on any horizontal bus, the number set upon on the switches of that bus should be the 10's complement of the desired function value.

1.3.7.9. *Digit Pulse Gate*

The digit pulses for the table output gates T40 are derived from digit pulse gates T56, represented here by a block into which 4 pulse lines T57 from the cycling unit enter, and 10 digit lines T58 emerge. It is obvious how the pulses 1, 2, 2′ and 4 can be combined to produce the

various numbers required for the 10 digit lines T58, as an even more complex system for a similar purpose was fully explained in connection with the high speed multiplier. The detailed connections for accomplishing this are shown in FIG. 48–B for the actual ENIAC. Provision is made for both addition and subtraction by the usual ENIAC procedure of providing the 9's complement for each digit, and an extra connection pulse through gate T58' when the subtracting line 59 is engaged.

Referring again to our example, the hundreds switch for argument bus 67 is shown set for the digit 7. This energizes the number 7 conductor of 10 conductor cable T38, and therefore turns off inverter T39 of the associated 7th place in the hundreds column of table output gates T40. This permits seven pulses to pass (from line 7 of digit gates T56) during the addition time under consideration, through gate T42 to hundreds pulse line T43, and thence, through pulse shaper T44 to the output digit socket T46. During this same addition time, in similar fashion, two pulses will pass gate T47 to tens pulse line T48, and 5 pulses will pass gate T63 to units pulse line. Thus the desired function value, 725, will be transmitted from the output digit socket T46.

1.3.7.10 *Add-Subtract Circuit*

We left the program ring T31 at stage 1, which was used to pass the extra 1P from gate T25 (or 2P if operation switch T19 is set at +1). During the following addition time, the ring is advanced to stage 0, and line T66 is excited to pass a CPP through gate T67, which is applied to both of gates T69 and T71 (through an inverter). Depending on the setting of add-subtract switch T73, one of these gates T69 and T71 will pass the CPP to either "add" flip-flop T74 or "subtract" flip-flop T76, and therefore one of these flip-flops is set to energize either line T61 (for "add") or line T59 (for "subtract") to produce either the called-for function (y) or its complement, and this value will be produced at the output digit socket T46 the following addition time and each addition time thereafter until the "set" flip-flop T74 or T76 is reset.

1.3.7.11. *Repeat Circuit*

The number of addition times the above procedure (production of y at output socket) is performed depends on the setting of repeat switch T77. The two stages of this switch are connected with the last two stages of program ring T31 (the actual ENIAC has 9 such stages instead of two). When the stage is reached for which the repeat switch T77 is set, the output of that stage is conducted through switch T77 to conductor T78 to transceiver T2. This clears the transceiver and causes it to emit a clear signal on line T79 and also to emit a program pulse on line T81, which may be used to initiate some different program on another unit, or to actuate a second transceiver T2 to get another function value (y_1 or y_2) for use in interpolation, as previously described. This action of the transceiver is the same as in the standard accumulator transceiver.

The "clear" signal on line T79 gates a CPP through gate T82, which passes through an inverter, and line T83, thence to lines T84 and T86. Line T84 is used to clear the argument ring back to zero, as will be obvious from the drawing, and line T86 feeds a pulse to lines T87 and T88, the former of which is used to clear the program ring back to —2, while line T86 leads to the "reset" terminal of the add flip-flop T74 and subtract flip-flop T76.

The above described action thus resets all parts of the function table back into initial condition. It will be apparent from the drawing that flip-flop T13 was reset the next addition time, after it was set, by a CPP gated through gate T16.

1.3.8. *Elementary Interpolation—Linear*

FIG. 22 is a schematic diagram of a hook-up for performing linear interpolation of the type described in Examples 25 and 30. We shall use the same example and assume that the function table is set up according to Table 24. The problem is to obtain the function value corresponding to an argument value of 67.32. We shall do this according ot the expression:

$$(33) \qquad y_x = y_0 + h(y_1 - y_0)$$
$$= 7250 + .32(7450 - 7250)$$
$$= 7250 + .32 \times 200$$
$$= 7250 + 64$$
$$= 7314$$

We shall outline below the steps by which this operation is performed:

Six units are required (numbers correspond to those in the drawing):

1—multiplier accumulator
2—multiplicand accumulator
3—high-speed multiplier
4—product accumulator
5—argument accumulator
6—function table

No attempt is made in the schematic diagram of FIG. 22 to show the actual panels which would be used in the ENIAC. For example, the multiplier (unit #3) actually has three panels, and the product accumulator (unit #4) actually requires at least two accumulators, one for the left-hand partial product and one for the right-hand partial product. Only such units are shown here as are essential to an understanding of the principle. There are usually several ways in which the units can be connected to perform any particular complicated operation; the more complex the operation, as a rule, the greater the choice of programing and control arrangements to achieve the desired result. The connections used in a given case depend largely on the skill, judgment and experience of the user. The examples given in this specification are solely for the purpose of illustration, and are accordingly made as simple as possible. It should be clear from these examples that the ENIAC can be programmed to perform arithmetical operations in a great variety of ways to achieve the solution of any numerical problem involving a sequence of arithmetical operations (addition, multiplication, etc.) in accordance with practically any algebraic formula, at electronic speeds and without the intervention of manual or human control, once the machine has been set up and programmed; the ultimate limitation of the machine is due only to the limited number of units, lines and tubes which it is economically feasible to expend for this purpose.

Referring again to FIG. 22, it will be assumed that a pulse comes in on program line number 1 to initiate the operation. This will ordinarily result from some previous computation, but could also, of course, be manually initiated. It is also assumed that the argument accumulator (#5) contains the value P6732, as in our example, and that the digit line connections are such that the first two digits, 6 and 7, will be transmitted to the function table (#6) and the second two digits 3 and 2, will be transmitted to the multiplier accumulator (#1) when the argument accumulator is stimulated to transmit; this latter transmission includes a shifting over of the number 0032 two places (two digit lines) to the left, so that the value P3200 appears in unit #1 instead of P0032. This interconnection and shifting is of course accomplished by the use of suitable shifters. Thus, the following operations must be performed in FIG. 22 to accomplish the desired linear interpolation:

(*a*) Starting with argument P6732 in the argument accumulator:
(*b*) Transmit this on 4 digit line so as to
(*c*) Receive P67 in the function table argument input socket and
(*d*) Receive P0032$\times(10)^2$ in the multiplier accumulator.
(*e*) Transmit additively from the function table
$f(67+1)=f(68)=$P0000745
(*f*) Then transmit subtractively from the function table
$f(67+0)=f(67)=$M9999275 (−0000725)
(*g*) Receive (*e*) in multiplicand accumulator ($\times 10^2$)=P00745

(h) Receive (f) in multiplicand accumulator ($\times 10^2$) = M9927 5

(i) Result in multiplicand accumulator = P00020

(k) Multiply multiplicand and multiplier values
$= P320 \times P00020 = P0000640$ in product accumulator

(l) Transfer to the product accumulator
$f(67) \times 10^2 = P0072500$

(m) Result in product accumulator P0073140 (answer)

The program lines used in FIG. 22 are numbered 1 to 7. The seven numbered paragraphs below each describe the events that occur from the time a pulse enters the program line corresponding to the paragraph number until a program pulse enters the next line.

I. Initiating pulse comes in on line 1 and through TT9 stimulates multiplier accumulator TT1 to receive on its β circuit from digit line TT7 through a 2-place shifter (indicated by +2 in the β terminal box) so that the received number is multiplied by 100; the numeral 4 under the B indicates that the repeat switch is set for 4 repetitions (4 addition times) before an "out" program pulse is emitted to line 3. The initiating pulse on line 1 also stimulates function table TT6 to receive on its control circuit #1 through line TT8; and as previously explained in connection with the elementary function table, a signal is made available at the NC terminal; this signal is conducted through lead TT11 to stimulate the second phase of the operation. A control #1 of the function table is set for +1, the table will look up the value of $f(x+1)=f(67+1)=0000745$.

II. The pulse on program line 2 passes up lead TT12 to stimulate argument accumulator TT5 to transmit its contents additively once. The number 67, as previously explained, goes to the function table through adapter TT10 (which connects only the lines bearing the 6 and 7 to the Function Table), while the number 0032 goes to multiplier accumulator TT1; both these units were conditioned to receive by the initiating pulse on program line 1, and are still in this receptive condition. After this reception occurs the "out" signal on line TT13, from the multiplier accumulator, stimulates program line 3.

III. The pulse on program line 3 conditions multicand accumulator TT2 through line TT15 to receive on its circuit. This reception will be from digit line TT14, through a +2 shifter, so that the received number will be multiplied by 100. Digit line TT14 is connected to the digit output of the function table by line TT16, so that the function $(Y(x+1)=f(67+1)=P0000745$ is transmitted to the multiplicand accumulator TT2, where it is multiplied by 100 and received as P00745.

IV. After function table TT6 has completed the above transmission, its control #1 emits a pulse on line TT26, which is connected to both program line 4 and control #2. This stimulates control # 2 to look up

$$f(y_x)=f(67)=0000725$$

As this is to be transmitted subtractively, the function table actually prepares to transmit −00000725 or M9999275. Line TT17 connects the multiplicand accumulator TT2 to program line 4, which stimulates a transceiver of TT2, the only purpose of which is to provide a program pulse on program line 5 (through TT18) four addition times later.

V. This pulse passes through TT19 to the multiplier TT3, and the multiplier controls are set to cause (by connections not shown) accumulator TT2 to receive on the y-input during the immediately ensuing addition time. This is the same addition time during which the Function Table TT6 is to transmit (subtractively) F(67) on digit trunk TT14, and the value transmitted (M9999275) passes through the +2 shifter at the input of TT2, which already contains P00745. The resulting sum (P00020) in TT2 represents $F(68)-F(67)=\Delta y$. During the several following addition times, the multiplier causes the product to appear in TT4, by means not shown. In accordance with the multiplier control settings, only the left three digits of the number in TT1 are used in this multiplication. The product, $P320 \times P00020$, appears as P00006400. (No round-off is used.) At the end of this operation, TT3 emits a pulse to program line 6 through TT21.

VI. The pulse on program line 6 passes through TT20 to a transceiver of TT4, and through TT22 to a transceiver of TT6. TT4 is thereby stimulated to receive for 5 addition times through its y input terminals, and the function table control #3 is set up to deliver

$$F(x)=F(67)=P0000725$$

through TT15 to digit trunk line 1. As in previous operations, a pulse from NC through TT11 is used to cause TT5 to transmit the argument value to TT6 through TT10 as the first step in the Function Table operation. The digit pulses from digit line 1 (occurring during the fifth addition time) are received by TT4 through a +2 shifter, so that the y-input of TT4 the number received is P0072500. Since TT4 already has the product

$P0000640$ in it, after
$P0072500$ is received, the sum is
$P0073140$

An output on TT23 from control #3 gives a pulse on program line 7 which may be used in further work.

II. INITIATING UNIT

The initiating unit of the ENIAC is the device which contains controls for turning the power on and off, for initiating a computation, for initial clearing, and for selective clearing a group of accumulators, as well as program controls for the reader and printer. Certain devices for testing the ENIAC are also located on the initiating unit.

The following topics are discussed in this chapter: Section 2.1, starting and stopping the ENIAC power and initial clearing; Section 2.2, reader and printer program controls on the initiating unit; Section 2.3, initiating a computation; Section 2.4, selective clear program controls; and Section 2.5, testing features. The following drawing are referred to in this section:

Initiating Unit—Front View_____ FIG. 23.
Initiating Unit—Front Panel_____ FIG. 24.
Cycling Unit and Initiating Unit
Block Diagram_____ FIGS. 25–A and B.
Power System Block Diagram_____ FIG. 26.

2.1. *Starting, Stopping and Initial Clearing*

Nearly all the characteristic functions of the ENIAC depend on D.-C. power. This, however, is derived from 240 volt, 3 phase, A.-C. The latter has some immediate uses in addition to furnishing the D.-C. There are in all five principal uses for the A.-C. power. These are as follows:

(1) For the heaters of the numerous tubes of the ENIAC units.
(2) For the heaters of the rectifier tubes in the ENIAC's power supply.
(3) For the plates of the rectifier tubes.
(4) For the fans which dispel the great amount of heat generated by the preceding.
(5) For the control circuits needed in starting and stopping the ENIAC power, in furnishing protection to various circuits, and in initial clearing.

Controls for the first four items referred to above are shown in FIG. 26. The last item noted above relates to control circuits and is more explicity dealt with in FIG. 25. The control circuits govern the connection of the other items to the A.-C. lines, cause D.-C. to be supplied to the units of the ENIAC, and control the initial clearing of these units.

Program controls for these circuits are found on the initiating unit. Other auxiliary program controls and elements of the control circuits are found on the power distribution rack, the condenser cabinets, and the units of the ENIAC themselves. In this section we shall discuss the

events involved in starting and stopping the ENIAC (Section 2.1.1) and in initial clearing (Section 2.1.2).

2.1.1. *Starting and Stopping the ENIAC*

In this discussion it is assumed that the main A.-C. safety switch K1 is closed. By a "safety switch" is meant one whose opening not merely cuts off power, but actually opens all lines of the circuit controlled by the switch. We also assume here that the 2 safety switches K2 for the ENIAC heaters and those (K3) for the fans (K4) for the heaters and (K5) for the plates of the power supplies are all on. With the last 2 switches off, only the A.-C. circuits can operate; with any of the others off, neither A.-C. nor D.-C. can.

When the start button K6 on the initiating unit (see FIG. 24) is depressed, the amber pilot light goes on immediately and the following sequence of events takes place: The ENIAC heaters and the power supply heaters are connected to the A.-C. and the ventilating system is turned on. One minute later, after the heaters have had an opportunity to warm up, the plates of the power supply tubes are connected to the A.-C. Simultaneously, initial clearing, which lasts for 10 seconds, begins. After the ENIAC has been initially cleared, the green pilot light on the initiating unit goes on and the ENIAC is ready to operate.

A heaters clock K8 on the front of the initiating unit, keeps count of the number of hours that the power supply heaters are on; this starts to record as soon as the start button is pushed. On each of the remaining 39 panels of the ENIAC, there is also a heaters clock and an on-off switch for the heaters. When the A.-C. is turned on, the heaters in a panel go on only if the switch for that panel is in the "on" position. The associated heaters clock records the number of hours that the heaters of the panel are turned on.

Before a more detailed discussion of the starting sequence is given, the *elements involved* in various phases of *starting* will be pointed out on the schematic diagram of the A.-C. control circuits shown in FIG. 26 and FIG. 25–B. The elements shown in FIG. 25–A and 25–B are not in the initiating unit.

Referring to FIG. 25–B and FIG. 26, relay K9 (where respective contacts are designated K9 (1), K9 (2), etc.) and K10 connects the heaters of the ENIAC units to the 3 phase A.-C. power. Relay K11 is the power supply heaters contactor. K12, an adjustable timer which has been set for 1 minute, provides for the delay between the turning on of the power supply heaters and plates. When timer K12 has counted the specified period of time, relay K13 is activated. This relay connects the plates of the power supplies to the A.-C. so that the D.-C. is turned on when relay K13 is activated. Timer K14 which has been set for 10 seconds and relay K16, the main initial clear relay, are activated after the D.-C. is turned on. Relays K17 and K18, auxiliary initial clear relays, are each responsible for the emission of one of the signals involved in initial clearing (see Section 2.1.2). Ten seconds after timer K14 starts to count, relay K19 is activated and the initial clear period is terminated, thus bringing the starting sequence to an end.

It can be seen that in addition to the start and stop buttons on the initiating unit which operate both the A.-C. and D.-C. circuits, *separate D.-C. start and stop buttons* K21 and K22 have been provided. Through the use of the D.-C. stop button, only the D.-C. circuits (controlled by relay K13), can be turned off, leaving the A.-C. circuits unaffected. With the A.-C. power on, pushing the D.-C. start button connects in the D.-C. circuits and causes initial clearing to take place. Isolation of the D.-C. from the A.-C. circuits has been provided in order to make possible leaving the heaters turned on even when the ENIAC is not to be operated or when there is a failure (see the discussion of protective circuits below) in the D.-C. circuits. This has been done in order, by cutting down the number of times that the heaters are turned on and off, to lengthen tube life.

It is to be noted that the *operation selector switch on cycling unit must be set at continuous when the power is turned on.* In Section 2.1.2, where initial clearing is discussed, it is pointed out that when the power is first turned on, a number of flip-flops may come up in the abnormal state and it is also remarked that the resetting of these often depends on the pulses and gates emitted by the cycling unit. These pulses are not given out immediately unless the ENIAC is in continuous operation. The danger of having these flip-flops remain in the abnormal state is that, as a result, a number of tubes that should be off most of the time and on only a short period of time (i.e., tubes in circuits that have been designed for a low duty cycle) remain on for a long time and thus cause damage to themselves and other elements.

Certain protective devices included in the control circuits are also shown on FIGS. 26 and 25–B. Of these the most important are relays K26, K27, K28 and K29. The action of these will be discussed in the following paragraphs. Their distinguishing characteristics are as follows: under proper operating conditions K26 and K28 are on; K29 and K27 are off. K26 may be turned off by a thermostat or a door switch. Since it is undesirable to turn off the heaters unless it is absolutely necessary, K26 acts through a timer K32 which may be set between 5 and 15 minutes. When this time has elapsed and the trouble has not been remedied, both A.-C. and D.-C. circuits are turned off. The other three relays act without any delay but affect only the D.C. Relay K27 is turned on by the blowing of any heater fuse. This cuts off the D.-C. power supply including its heaters. Relay K28 is turned off by phase in the plate supply or under-voltage in the output of a D.-C. power supply. The effect is to turn on K29. This is also accomplished by the D.C. stop button or the failure of a D.-C. fuse. When K29 is turned on or when there is any phase failure in the heaters, the plate supply to the rectifiers is cut off, but the heaters are left on. The distinction between K28 and K29 is that there is a provision for inhibiting the action of K28 during starting. These actions will now be discussed in more detail.

Relay K26 is a master relay which controls both A.-C. and D.-C. circuits. This relay, which is activated when the A.-C. safety switch is closed, operates in conjunction with the door switches (see below), thermostats, and timer P. Found at the back of each ENIAC panel and at the front of the power supply and condenser cabinets, is a door switch. When the cover of a panel or cabinet is removed, the door switch on the panel opens, causing relay K26 to be deactivated. If, however, the door switch shunt button K31 on the initiating unit (see FIG. 24) is held down while the cover is off, relay K26 is not deactivated. Relay K26 is also deactivated when a thermostat opens as a result of the overheating of a unit. When relay K26 is not activated contact K26 (1) closes and timer K32 which is set for 5 minutes starts to operate. First its clutch K32 (CL) is thrown in, and next the motor K32 (M) is connected into the circuit through contact K32 (CL1). A warning lamp above the power distribution rack also lights. Necessary repairs can be made on the machine during this 5 minute period (which may be adjusted to as much as 15 minutes), but if the condition which caused relay K26 to be deactivated has not been corrected, then contact K32 (1) opens and relay K (9) is deactivated. This turns off both the A.-C. and D.-C. circuits. The start button on the initiating unit is used to turn the power on again after the fault has been corrected.

The door switches have been provided as a safety measure for both personnel and the machine since the opening of a panel exposes dangerous voltages (as much as 1500 volts in the case of the D.-C.) and also, by drawing air from the ventilating system to the open panel, may cause another unit to overheat.

Relay K27 protects the D.-C. circuits and the power supplies. When K27 is activated, contact K27 (1) opens so that relay K11 is de-energized. This turns off the power supply heaters and causes contact K11 (1) to open. With contact K11 (1) open, K12 is de-energized so that contact K12 (1) opens and relay K13, the D.-C. contactor is deactivated. Relay K27 is activated when a contact on one of the power supply heater fuse relays closes. This latter event takes place if a power supply heater fuse blows. If the D.-C. is turned off because K27 has been activated, the D.-C. start button on the power distribution rack must be used to turn the power on again.

The remaining protective devices shown in FIG. 25–B relays K29 and K28 with their associated devices, control only the D.-C. circuits, leaving all heaters turned on in case of a failure. If one of these circuits detects a failure and turns the machine off, the power can be turned on again through the use of the D.-C. start button. The main and power supply heater phase failure relays connected in series with timer K12 detect faults in the three phases which goes to the heaters of the ENIAC and of the power supplies. These phase failure relays are activated so that the contacts shown in FIG. 25–B are closed under proper operating conditions. In the event of a phase failure, K12 is de-energized so that contact K12 (1) opens and relay K13 drops out. As soon as the fault is repaired, timer K12 is again activated and, one minute later, contact K12 (1) closes.

Relay K29 is the D.-C. cut-off relay. When this relay is activated, contact K29 (1) opens so that relay K13 is de-energized. This results in cutting off the D.-C. power. With the A.-C. on (so that contact K9 (4) is closed), relay K29 can be picked up through the closing of the D.-C. stop button, the activation of the D.-C. fuse relays when a D.-C. fuse blows, or the non-activation of relay K28 (see the discussion of relay K28 in the next paragraph).

Relay K28 operates in conjunction with the power supply phase failure relays and the under-voltage release relays. The power supply phase failure relays in this circuit detect faults in the three phase A.-C. which goes to the plates of the power supply tubes. These relays are activated and their contacts closed under proper operating conditions. There is an under-voltage release relay for each power supply. During the starting sequence while initial clearing takes place, relays K33 are activated. These relays provide the high voltage required to pick up the under-voltage release relays. After the starting sequence is completed, the under-voltage release relays remain activated and their contacts are closed unless the voltage emitted by a D.-C. power supply drops below a specified level. During the initial clear period while the under-voltage release relays are being picked up, contact K19 (2) of relay K19 provides a circuit which shunts the under-voltage release relays and the power supplies phase failure relays. Thus, relay K28 is activated and contact K28 (1) is open at all times unless a fault is detected.

The starting sequence which takes place when the start button in the initiating unit is pushed is described chronologically in Table 2–1. In some cases, a contact is classified as both a pick up and hold contact for a circuit, since the contact must close for the circuit to operate and since the circuit continues to operate only so long as the contact remains closed. In other cases, the pick up and holding functions are performed by separate contacts.

When the stop button on the initiating unit is pushed, the ENIAC is completely turned off. Relay K9, then K10, K34, K11, K13, K15 and K19 are de-energized.

When only the A.-C. circuits are on, and the D.-C. start button is pushed, the following events take place: Relay K29 is deactivated, and through contact K12 (1) (closed provided that the A.-C. is on and there is no phase failure in the power for the ENIAC and power supply heaters) and K29 (1) (closed when K29 is deactivated), relay K13 is picked up. This turns the D.-C.

on and then initial clearing follows as indicated on Table 2–1 below.

TABLE 2-1.—CHRONOLOGICAL DESCRIPTION OF STARTING SEQUENCE

Activated Relay or Circuit Element	Pick Up contact (contact whose closing causes circuit to operate)	Hold contacts (Contacts which must remain closed for circuit to continue to operate)
K9—auxiliary start relay.	Start switch—closed when start button is pushed.	Stop switch—normally closed. K32 (1)—closed unless timer P has been activated for 5 minutes. K10 (1)—closes immediately after K9 is activated.
K10—main start relay and ENIAC heaters contactor.	K9 (1)	K9 (1). K10 (1).
K34—fans contactor	K9 (3)	K9 (3).
K11—power supply heaters contactor.	K34 (1)	K34 (1).
Amber start pilot and power supply heaters clock.	K9 (4)	K9 (4).
K12—one minute timer.	K11 (1)	K11 (1). Main and power supply heaters phase failure relays—closed unless a fault is detected.
K13	K12 (1)—closes after F has counted out 1 minute.	K12 (1). K29 (1)—closed unless L is activated.
K16—Main initial clear relay.	K13 (1)	K13 (1).
K14—10 sec. timer.		
K33—under voltage release pick-up relays.		K19 (4)—closed until K is activated.
K19—relay which terminates initial clear period.	K14 (1)—closes after timer has counted 10 seconds.	K19 (1). K13 (1). Initial clear switch—remains closed unless I.C. button is pushed.
Green ready pilot	K19 (3)	K19 (3).

When the D.-C. stop button is pushed, relay K29 is activated. Since contact K29 (1) then opens, relay K13 drops out and the D.-C. is disconnected. Contact K13 (1) also opens, causing relay K19 to drop out.

With regard to the matter of interrupting a computation, it might be pointed out that it is not necessary to push the stop button on the initiating unit or the D.-C. stop button for this purpose. Even though the power is turned on, a computation can be stopped in a number of different ways. If a program cable which delivers a program output pulse to a program tray is removed, the computation in progress ceases with the program whose program output pulse is eliminated in this way. If the card reader exhausts the cards in its magazine, the computation is terminated with the program just before the one in which reading would take place. A computation ceases, similarly, when the cards in the magazine of the card punch are exhausted.

2.1.2. *Initial Clearing*

When the ENIAC is turned on, it is a matter of chance as to which flip-flops in the various counters, both numerical and program ring, or which program flip-flop (in receivers, transceivers and common programming circuits) will come up in the abnormal state. It is obvious that a computation must start with the numerical and program rings in the clear position and with program flip-flops in the normal state in order that the correct answer may be obtained. Furthermore, if a flip-flop in a transceiver or a program control flip-flop such as the printer start flip-flop comes up in the abnormal state, not only is the associated program commenced, but also, upon the completion of the program, an output pulse is transmitted which, in turn, may stimulate another program control, etc. Thus, it is also necessary before starting a computation to

break program chains or sequences which are accidentally begun when the ENIAC is turned on. Furthermore, it is convenient to be able to stop a computation at a certain point (without turning the ENIAC power off), erase all data stored in accumulators and the master programmer, and then start afresh.

The initial clear circuits in the ENIAC provide for the contingencies mentioned above. The initial clear circuits consists of the initial clear push button K35 on the initiating unit (FIG. 24), relays K16 and K19 which were referred to in Section 2.1.1 and initial clear relays K17 and K18. When the ENIAC's power is turned on, initial clearing takes place automatically immediately after the D.-C. goes on (see Section 2.1.1). The initial clear push button is pushed when, with the power already on, it is desired to clear the accumulators and the master programmer. It is to be noted, that the *operation selector switch on the cycling unit must be set at continuous* for initial clearing to take place. Relay K16 is the main initial clear relay. When activated, this relay causes initial clearing to take place. Relay K19 terminates the initial clear period. Initial clear relay K18 is responsible for emitting the initial clear gate (ICG) which, in general, clears the counters used for either numerical or programming purposes. Initial clear relay K17 causes the master programmer clear gate (MPC) to be emitted. The MPC is used in the master programmer to break sequences (see the discussion in the latter part of this section).

When the start button on the initiating unit or the D.-C. start button is pushed, relay K19 is not activated so that relay K16 and the ten second timer K14 are picked up through contacts K13 (1) and K19 (4). At the end of 10 seconds, contact K14 (1) on the timer closes. Through K14 (1), relay K19 is picked up. From then on, relay K19 holds through contact K19 (1) and the initial clear switch which is normally closed.

When the power has been on and the initial clear button is pushed, relay K19 is de-energized so that K19 (4) closes. Since K13 (1) remains closed as long as the D.-C. is on, relay K16 and timer K14 are then picked up through K13 (1) and K19 (4).

When relay K16 picks up, contact K16 (1) closes, thus activating relay K17. Contact K17 (1) then closes and the MPC is emitted. As a result of the activation of relay K17, contact K17 (3), which is normally closed, opens. Now with K17 (3) closed, there is a circuit which allows a small amount of current to flow through the coil of relay K13 but not enough to pick this relay up, and very little passes through the large resistor to the condenser. While K17 (3) is open, however, the condenser is charged.

Ten seconds after relay K16 is activated, K19 is activated. Contact K19 (4) opens and K16 is, thus, deactivated. This causes contact K16 (1) to open and relay K17 to drop out. At this time, contact K17 (3) closes. This allows the condenser to discharge through the coil of relay K18. In this way, relay K18 is activated and contact K18 (1) is closed. With contact K18 (1) closed, the initial clear gate is emitted. Initial clear relay K18 is restored to the normal state with contact K18 (1) again open in about ½ a second when the condenser has discharged.

As can be seen from the discussion above, the 10 second period (when the green light is off and when timer K14 is operating) designated by the phrase initial clear period, is actually devoted to the master programmer clear signal. The initial clear gate comes on after the MPC goes off and lasts for about ½ a second. Both the MPC and ICG are carried to the other units of the ENIAC in the D.-C. voltage cable.

2.2. *Reader and Printer Program Controls on the Initiating Unit*

2.2.1. *Reader Program Controls*

Certain reader program controls are found on the initiating unit (FIGS. 24 and 25–A). These include the reader flip-flop K37 (FIG. 25–A) and program pulse input terminal (R*i*) K38, the reader interlock input terminal K40 and flip-flop K43, the reader finish flip-flop K42, the reader synchronizing flip-flop K47 and program pulse output terminal K39, and associated gates, buffers, and inverters. The reader start button K41 is also on the initiating unit.

The reader start flip-flop K37 is flipped into the abnormal state either when K38 receives a pulse or when, at the beginning of a computation (see Section 2.3), the reader start button K41 is pushed. When the start flip-flop is in the abnormal state, a start relay in the constant transmitter is activated so that the reader is stimulated to read a card and cause information read from the card to be stored in the constant transmitter. A little less than half way through the card reading cycle (see Chapter VIII), a reset signal from the reader resets the start flip-flop K37 so that, even though reading is not yet completed, the start flip-flop is capable of again being flipped into the abnormal state (by the reception of a pulse at K38) to remember that reading is to take place again.

When reading of one card is completed, the reader emits a finish signal which causes the reader finish flip-flop K42 to be flipped into the abnormal state. The interlock flip-flop K43 is flipped into the abnormal state when an interlock pulse arrives at K40 or, at the start of a computation, when the reader is stimulated to read by the reader start button K41. The reader interlock flip-flop K43 makes it possible to carry on a sequence of programs in parallel with reading and then to stimulate the next program sequence when both reading and the parallel sequence have been completed since no program output pulse is emitted from terminal K39 unless the interlock flip-flop is flipped into the abnormal state (see below). If a computation does not call for a sequence in parallel with reading, the operator can provide an interlock pulse by sending the pulse which goes to K38 and also to K40.

The coincidence of signals from the interlock (K43) and finish (K42) flip-flops cause gate K44 to emit a signal. The output of gate K44 gates a CPP through gate K46 which then sets the reader synchronizing flip-flop K47. The CPP gated through K43 by the normally negative output of the synchronizing flip-flop K–47 thus provides a reader program output pulse which is emitted from terminal (K39). The reason that the synchronizing flip-flop K47 and gate K43 are used after gate K46 is to ensure a program output pulse of the proper shape and in synchronism with other program pulses.

Neons correlated with the flip-flops mentioned above are shown in FIG. 23. Program controls for the reader in addition to those on the initiating unit are discussed in Chapter VIII.

2.2.2. *Printer Program Controls*

The printer program controls on the initiating unit include the printer start flip-flop K51 and program pulse input terminal K52, the printer finish flip-flop K53, the printer synchronizing flip-flop K54 and program pulse output terminal K56, and associated gates, buffers, and inverters. Neons correlated with the flip-flops appear in FIG. 23.

A program input pulse received at K52 flips the printer start flip-flop K51 into the abnormal state. This causes a start relay in the punch or other data recording device to be activated so that the recording device is set up for the data to be printed or otherwise recorded and so that a data recording cycle is initiated. About ¼ way through the data recording cycle, the data recording de-

vice emits a finish signal which resets the start flip-flop K51 and sets the printer finish flip-flop K53. The output of the finish flip-flop K53 in the abnormal state gates a CPP through gate K57. The output of K57 sets the printer synchronizing flip-flop K54 whose output gates a CPP through gate K58. The output of gate K58 is transmitted from K56 as a program output pulse.

2.3. *Initiating Pulse for a Computation: Reader Start Button and Initiating Pulse Button*

Once the starting sequence is completed (amber and green pilot lights are on) the ENIAC is ready to begin computing. To stimulate the computation to begin, however, a program pulse must be delivered to the input terminals of the program controls on which are set up the programs that begin in the first addition time of the computation. Alternate methods exist for stimulating the beginning of a computation.

If the first event of a computation consists of the reading of a card, the computation can be started by pushing the reader start button K41 on the initiating unit (see Section 2.2.1). When reading is completed, then, a program output pulse is emitted from terminal K39. This pulse can be used to stimulate the programs of the computation which immediately follow reading. As was noted in Section 2.2.1, pushing the reader start button also results in setting the reader interlock flip-flop so that no interlock pulse need be provided for a reading initiated by the reader start button.

The terminal marked R_s (K60) in FIG. 24 parallels the reader start switch and is used for remote control (see Section 2.2.1).

The second procedure for initiating a computation is to connect the terminal marked I_o (K61) in FIG. 24 to the same program line as the input terminals of the program controls used for the first programs of the computation. When the initiating pulse button K62 is pushed, the initiating pulse input flip-flop K63 (see FIG. 25–A) is set. Its output allows a CPP to pass through a gate K64 and set the synchronizing flip-flop K65. The output of the synchronizing flip-flop K65 gates a CPP through gate K67 which resets the input and synchronizing flip-flops K63 and K65 and causes a program pulse to be emitted from terminal I_o (K61). Neons correlated with the flip-flops mentioned above are shown in FIG. 23.

The two flip-flops operating as described above always provide a standard output program pulse. Gate K64 may open in such a way that only part of a CPP is passed. If it fails to operate flip-flop K65 no harm is done since flip-flop K63 is not reset and the next CPP is passed full strength by gate K64. Then the flip-flop K65 has one full addition time in which to set up so gate K67 is open and passes a standard program pulse. This pulse then resets the flip-flops and is transmitted.

The initiating pulse button K62 has a second important use in connection with testing ENIAC. One of the chief techniques for localizing errors in either the machine or the set-up of the machine is to operate the ENIAC in the one addition time mode or in the one pulse time mode. Here, the pulses for one addition time or 1 pulse time at a time respectively are given out in sequence every time the 1 pulse-1 addition time button on the cycling unit is pushed (see Chapter III). In this way, there is an opportunity to observe the numerical and programming neons. Frequently, it is more convenient to proceed through a portion of the computation with the ENIAC operating in its normal or continuous mode and then to switch to 1 addition time or 1 pulse time operation than it is to progress through the entire computation non-continuously. This may be arranged by disconnecting the program cable which delivers the pulse used to initiate the programs which are to be examined non-continuously. We call this point where the program cable is removed a break point. When the initiating pulse button is pushed, the computation begins and progresses to the break point. With the necessary switch made in the cycling unit (see Chapter III), computation in the non-continuous mode can be stimulated by delivering the initiating pulse from terminal I_o (K61) to the program line from which the program cable was removed. The reader will notice that after the initiating pulse button is pushed, two addition time cycles, one in which a CPP passes through gate K64 and one in which a CPP passes through gate K67, are required before the initiating pulse is delivered.

The emission of the initiating pulse may also be stimulated by remote control. The terminal marked I_s (K68) in FIG. 24 is used to parallel the initiating pulse switch with a switch which may be carried anywhere around the ENIAC room and which is connected to I_s via a program line which has no load box.

2.4. *Selective Clear Controls*

There are 6 selective clear program controls on the initiating unit. Each control consists of a transceiver with a program pulse input (C_i) and output (C_o) terminal (the location of these terminals on the panel is generally indicated by reference character K71) on the front panel. The outputs of the cathode followers of the six selective clear transceivers are connected in parallel to a line of the synchronizing trunk K72 (FIG. 29–B). When a selective clear receiver is stimulated, its flip-flop emits a signal called the selective clear gate (SCG); that is, whenever a program pulse enters one of the terminals C_i, the SCG is provided for one addition time and a program pulse is transmitted out of terminal C_o at the end of the addition time. One addition time later, the transceiver is reset by a CPP and a program output pulse is emitted from C_o. Neons associated with the selective clear program controls are shown in FIG. 23. For block diagram of a transceiver see FIG. 34.

The selective clear gate is delivered by the synchronizing trunk to the 20 accumulators. When the SCG is given out, and accumulator whose selective clear switch is set at SC clears in accordance with the setting of its significant figures switch (see Section 4.2.3). Notice that selective clearing lasts but one addition time and clears only the decade and PM counters of accumulators. The selective clear feature provides a convenient means of clearing the group of accumulators which store data for the printer (see Chapter IX) after printing takes place.

2.5. *Devices for Testing the ENIAC*

Located on the initiating unit (see FIG. 24) are the following devices for testing the ENIAC: D.-C. voltage meter K73 and associated voltage selector switches K74, D.C. voltage hum oscilloscope K75, and A.-C. voltage meter K76 and voltage selector switch K77.

The D.-C. voltage meter K73 together with the two D.-C. voltage selector switches K74 provide a means of examining any of the ENIAC's voltages. The D.-C. voltage chart K78 below the selector switches indicates which voltage is measured as a result of the combination of settings on the switches.

The A.-C. voltage meter K76 and switch K77 are used to measure the three phases of one of the two bus systems supplying 110 volt A.-C. to the filament transformers of the various units.

III. CYCLING UNIT

The cycling unit produces the pulses which are used to represent digits and to control the operation of units of the ENIAC. Also the carry-clear gate (CCG) is produced in the cycling unit. The pulses produced in the cycling unit control the timing of operations and enables the various units to operate in synchronism.

The following table gives a list of the pulses or gates

produced in the cycling unit. Also appearing in the table is the principal purpose of each pulse or gate.

TABLE 3–1

Pulse or gate	Abbreviation	Purpose
Central program pulse.	CPP	A program pulse used to control the activity of the various units of the ENIAC.
Tens pulses (off beat).	10P	Used to cycle the decades of an accumulator during the process of transmission of the number (or its complement) registered in the accumulator.
One pulse	1P	A coded system in the multiplier. Function tables and the constant transmitter makes use of combinations of these pulses to represent the digits zero to nine. Some of these pulses are used to represent the digits zero to nine.
Two pulses	2P	
Two-primed pulses.	2'P	
Four pulses	4P	
Nine pulses	9P	
One-primed pulse.	1'P	In the process of taking the complement this pulse is used to obtain the complement with respect to 10^n instead of 10^n-1.
Reset pulse	RP	This pulse is used to reset flip-flops in the accumulator decade units and to provide a carry-over pulse in the process of addition.
Carry-clear gate.	CCG	This gate controls the carry over process when adding in an accumulator and produces the clearing action when so desired.

The pulses and gates listed in the table above are produced in the cycling unit once each addition time. FIG. 2 shows the temporal order of these pulses and gates. These pulses and gates along with the selective clear gate from the initiating unit are distributed around to each unit of the ENIAC by the synchronizing trunk.

An addition time is normally 200 microseconds long. Each addition time is divided into twenty parts called pulse times, each ten microseconds long. All of the pulses except the 10P are produced at the beginning of pulse times or "on beat" and all have a duration of about two microseconds. The tens pulses (10P) are "off beat" since they pass through a 2.5 microsecond delay line and thus arrive at the beginning of the second quarter of a pulse time. The tens pulses, 10P, are used to cycle decades in the accumulators (see 4.3) during the process of transmitting the contents to an accumulator. These off-beat pulses are produced 2.5 microseconds late for timing reasons which will be explained in the chapter on the accumulator (see 4.3.1).

The pulses and gate above listed and shown in FIG. 2 are the only electrical impulses which pass from the cycling unit to the trunk lines and the arithmetical units of the ENIAC. There are however produced in the cycling unit certain impulses which, while similar in shape, potential and duration to the pulses so-named, do not pass out of the cycling unit, are used only within the unit as gates for effecting the production of the frame or cycle of pulses of FIG. 2, as will now be described.

The following description will show how normally a quartz crystal oscillator (FIGS. 29–A and B) emits 100 kc. sine waves which are converted into pulses for the ENIAC, spaced at a 10 mcs. interval by a pulse standardizer. The fundamental time unit for the ENIAC, a pulse time, is thus established as 10 microseconds. The output of the pulse standardizer goes to the so-called on beat circuit which contains another pulse standardizer and tubes for power amplification. The on beat circuit emits pulses (through one of its 3 outputs) to the off beat circuit. The off beat circuit shapes, amplifies and delays the pulses which it receives. One output of the off beat circuit through L18, delayed 1.25 mcs. after the on beat pulses, is taken to a 20 stage ring counter (neons correlated wtih the stages of the ring are shown in FIG. 27) which controls certain gate tubes and flip-flops. The off beat pulses from a second output of the off beat circuit, delayed 2.5 mcs. after the on beat pulses, are taken to a gate tube which is controlled by a flip-flop, the latter, in turn, controlled by the ring. Other gate tubes associated with the ring pass on beat pulses. The ring with its associated flip-flops and gate tubes is responsible for producing a pattern of pulses repeated every 20 pulse times (every addition time). The gate (CCG) and each of the 9 different kinds of pulses (see FIG. 2) emitted every addition time, are each carried on its respective one of the 11 leads of the synchronizing trunk (see Chapter II for the use of the 11th lead). The various units of the ENIAC are connected into the synchronizing trunk so that they can pick up the pulses needed for their operation.

The pulses generated by the cycling unit, or pulses from some external source, can be viewed on the screen of an oscilloscope built into the cycling unit.

This chapter will cover the following topics: sources of pulses and gates, Sec. 3.1; methods of operation of the cycling unit and ENIAC, Sec. 3.2; the cycling ring, Sec. 3.3; and the cycling unit oscilloscope, Sec. 3.4. Reference will be made to the following drawings:

Front Panel of the Cycling Unit	FIG. 27.
Front View of the Cycling Unit	FIG. 28.
Block Diagram of the Cycling Unit and Initiating Unit	FIGS. 29–A and B.
Cycling Unit Pulses and Gates	FIG. 2.
Timing of Pulses	FIG. 30.

3.1. *Pulses and Gates and Their Sources*

3.1.1. *The Pulses and Gates*

The nine different kinds of pulses and the gate emitted by the cycling unit every 200 ms. are shown in FIG. 2. The 10P are classified as off beat pulses; all other pulses as on beat. Each of the 10P, 9P, 2P, 2'P, 4P, the 1P, 1'P and CPP are roughly the same in shape and alike in duration (namely, 2 ms.). They differ from one another in the line of the synchronizing trunk over which they are emitted, and the purposes for which they are used in the ENIAC.

The 9P, the 1'P, the 1, 2, 2' and 4P are commonly used as digit pulses. An accumulator transmits the number stored in it or the complement of the number stored in it by gating appropriate numbers of the 9P over the various lines of the digit output. In the transmission of complements from an accumulator, the 1'P is gated and allowed to pass the lead which carries the extreme right hand significant figure being stored in the accumulator to make a tens instead of nines complement. The 1, 2, 2', and 4 pulses are used particularly where information stored in static form is converted into pulse form, e.g., in the high speed multiplier, the function table, the divider-square-rooter, and the constant transmitter. By suitable combinations of the 1, 2, 2', and 4 pulses any number between 1 and 9 can be formed. *The 10P are used only* in accumulators. They serve to cycle each counter around back to the position it starts from when the transmission of a number and/or its complement from an accumulator takes place (see Sec. 4.3.1).

The carry clear gate ("CCG" which lasts from pulse time 11 to 17) is used through cause the clearing of accumulators which, at the operator's option, may or may not take place after transmission of the content from an accumulator (see Sec. 4.2.3). The carry clear gate also allows a carry over pulse to pass from a decade counter to the decade counter immediately to the left if carry over takes place in the reception of a number by an accumulator (see Sec. 4.3.2). Carry over can take place in two ways: delayed or direct. In delayed carry over, the first *reset pulse* passed through a gate tube (which is controlled by a flip-flop that remembers that carry over is to take place) is gated by the carry clear gate so that it can reach the next decade with the effect of

a digit pulse. The second reset pulse resets this flip-flop. Direct carry over takes care of carry overs which result from carry over. In this latter case, the pulse which necessitates carry over (and not an original reset pulse, as above) is the one which the carry clear gate allows to pass to the next decade counter. The reset pulse is emitted twice, once during the emission of the carry clear gate for delayed carry over and once after the carry clear gate, to reset carry over flip-flops which may be set after delayed carry over takes place. The first reset pulse is also used to reset a flip-flop (the same one used for carryover in reception) which is set in the process of transmitting from an accumulator.

The principal uses of the central program pulse (emitted at pulse time 17) are the provision of the program pulses needed to stimulate program controls and for the resetting of the receivers and transceivers in these program controls.

3.1.2. *Sources of the Pulses and Gates*

A block diagram of the circuits of the cycling unit which are involved in generating the pulses and gates emitted by this unit appears in FIGS. 29–A and 29–B.

3.1.3. *The On-Beat Plug-in Unit*

The oscillator L1 emits 100 kc. sine waves which the pulse standardizer L2 converts into pulses spaced at 10 mcs. intervals.

In continuous operation (see Sec. 3.2) each pulse from the oscillator and pulse standardizer circuit is delivered to the on beat circuit L3. A special pulse standardizer in this circuit (tubes L4 and L5 and the 1 microsecond delay line L7) produces rectangular pulses 2 microsecond broad. The on beat circuit has 3 outputs. One of the outputs is brought to a terminal L8 labelled "On beat pulse output" (see FIG. 29–A). For every pulse received by the on beat circuit, a pulse in phase with the 9P is emitted from this terminal. These pulses are used in the test equipment of the ENIAC. Another output of the on beat circuit delivers pulses to line L6 for gates associated with various stages of the cycling unit ring and the third output delivers pulses to the off beat circuit L9.

3.1.4. *The Off-Beat Plug-in Unit*

The off beat circuit routes these pulses through a 2.5 microseconds delay line L11. This delay line is tapped at half its length, for the pulses which cycle the ring counter. The pulses delayed the full 2.5 microseconds, called the off beat pulses, are delivered to gate L12 (see FIG. 30 for a chronological comparison of the on beat and off beat pulses and the pulses which cycle the ring).

From a center tap on the 2.5 second delay line L11 pulses go through a pulse standardizer L10 and thence to step the ring counter L14. This pulse standardizer is similar to the usual pulse standardizer (used in accumulators) except that it has two driving tubes in parallel.

The setting of the zero stage of the ring having occurred by receipt of the 1.25 mcs. delayed off beat pulse, which is of two microseconds' duration, the next on-beat pulse will follow after an interval of 6.75 mcs. The first pulse conditions the first gate tube L15' so that receipt of the next on-beat pulse will transmit a pulse to the flip-flop 13 as stated. Similarly each of the succeeding stages of the ring will be set by the 1.25 delayed pulse, and this will result in the transmission from the respective gate of an on-beat pulse 6.75 microseconds later.

The end output of the delay line goes through another pulse standardizer L15 to the tens pulses gate L12. This pulse standardizer also has a one-microsecond delay line L20 to obtain square pulses of 2 microseconds length.

The pulses which step the ring arrive 1.25 microseconds after those that go to the pulse gates which are opened and closed by the stages of the ring. This means that the ring has 8.75 microseconds in which to step from one stage to the next, and for reliable operation the ring is designed to step to the next position in appreciably less time than this.

3.1.5. *Final Pulse Output of the Cycling Unit*

The off beat pulses pass through L12 to produce the 10P as long as gate L12 is held open by the 10P flip-flop L13 in the abnormal state. This flip-flop is flipped into the abnormal state until reset by a signal from gate L16, controlled by stage 10 of the ring. The 10P neon correlated with this flip-flop is shown in FIG. 21 at L17.

Stage 1 of the ring L14 controls gate L18. The on beat pulse passed through gate L18 gives rise to the 1P and the first of the 9P. Stage 2 of the ring controls gate L19. The on beat pulse passed through gate L19 gives rise to the first of the 2P and the second of the 9P, etc. In a somewhat similar way, the 1P, 2P, 2'P, and 4P, and the 1'P are generated respectively in the chronological order shown in FIG. 2, utilizing elements as illustrated in FIG. 29–B, as will be detailed later herein.

When the cycling unit ring is stepped to stage 11, gate L21 opens to pass an on beat pulse. This signal sets the carry clear gate flip-flop, L22 (see FIG. 27 for the associated neon in the abnormal state). This flip-flop remains in the abnormal state for the next 7 pulse times, being reset by an on beat pulse gated through gate L23 which is controlled by stage 18 of the ring. The signal from the carry clear gate flip-flop L22 in the abnormal state produces the CCG.

While the carry clear gate signal continues, an on beat pulse, gated through gate L24 (which is controlled by stage 13) produces an "RP" reset pulse of FIG. 2, and the second "RP" reset pulse is produced when the ring is in stage 19. Both of these are amplified and channelled in the same paths, as will later appear.

A signal from stage 17 of the ring gates an on beat pulse through gate L26 to produce a CPP.

All of the cycling unit pulses and gates shown in FIG. 2 are passed through cycling unit transmitters L27 for power amplification before transmission from the cycling unit to the several lines in the synchronizing trunk.

The ENIAC's oscillator circuit with its 100 kilocycle rate will ordinarily be located in the cycling unit. If for any reason it is desired to operate the ENIAC at some other rate, a different oscillator exteriorly located can be plugged in and used to supply pulses to the on beat circuit. When the oscillator switch L28 (see FIG. 27) is set at E (for "External"), and an external oscillator is plugged into the external oscillator input terminal at the right of this switch, the fundamental pulses for the cycling unit are derived from the external oscillator. When the cycling unit's built-in oscillator supplies the fundamental pulses, the oscillator switch is set at I (meaning "internal" oscillator). It is to be noted that the time constants for the ENIAC's circuits are designed for a frequency of 100 kc. and certain safety factors have been included on this basis. If a higher frequency is used, these safety factors will be lost so that the reliability of the ENIAC will be decreased.

3.2. *Method of Operation*

The cycling unit can be set up so that the ENIAC operated in one of 3 modes:

(1) Continuous operation at the fundamental frequency of the oscilllator used.

(2) One addition time operation in which the cycling unit supplies the pulses for only one addition time cycle at the oscillator rate with a wait of any length desired by the operator between addition times.

(3) One pulse time operation in which the cycling unit supplies the pulses of the addition time cycle one at a time with a wait of any length desired by the operator between pulses.

Continuous operation is the natural method of opera-

tion of the ENIAC. One addition time or one pulse time operation is used for testing and checking purposes. One addition time operation is particularly useful in checking a set-up that is put on the ENIAC. Before actually running through a complete computation continuously, the operator can cause the ENIAC to prorgess through one cycle of the computation, addition time by addition time. By observing the neon bulbs in the various units, he can then check to see that the units are operating properly and that switch settings and cable connections have been made correctly to carry out the contemplated set-up. To test whether or not a particular unit is functioning properly, 1 addition time, or, for finer discrimination, one pulse time operation can be used.

The cycling unit controls which are used for the various modes of operation are the operation selector switch **L29** and the 1 pulse time–1 addition time push button or "1P–1A" **L38** (see FIG. 28). When the operation selector switch **L29** is set at "Cont.," the cycling unit emits the pulses and gates continuously. When this switch is set at 1 add, the pulses and gates for 1 complete addition time cycle are given out every time the 1P–1A button is pushed. With the switch **L29** set at 1 pulse, the pulses or gates of the addition time cycle are given out in chronological sequence, one each time the 1P–1A button is pushed. It might be mentioned that all three modes of operation are possible whether the ENIAC's oscillator **L1** or an external oscillator is used to supply the fundamental pulses.

Continuous or non-continuous operation is accomplished by allowing all pulses or only certain pulses from the oscillator circuit to reach the on beat circuit **L3** (and through that the off beat circuit **L9**, and the ring **L14** with its associated gates). The continuous relay **L31**, the 1 addition time relay **L32**, gates **L33** and **L34** and the 1 pulse–1 addition time push button (see FIG. 29–A) are used for this purpose. It should be noted that gate **L34** is connected by line **L36** to the normally positive output of stage zero of the ring **L14**. Thus **L34** is closed when the ring is in abnormal state at stage zero and open at all other times.

In continuous operation, the requirements are that the circuit containing gates **L33** and **L34** shall pass all of the pulses from the oscillator and that accidentally pushing the 1 pulse–1 addition time push button shall have no effect. The requirements are met in the following way: with the operation switch set at continuous (as shown in FIG. 29) the continuous relay is activated so that its contacts 1 and 3 are closed and the 1 addition time relay **L33** is not activated so that its contact 6 is closed. Now with contact 1 closed, the cathode of tube **L37** floats and the tube is, therefore, inoperative. Since this tube is not conducting, its plate potential is relatively high and a positive voltage is applied to gate **L33**, so that one of the control grids of gate **L33** is sufficiently high for a positive signal on the other grid to cause it to conduct. The circuit through contact 3 delivers to the pulse standardizer **L2** and then to gate **L33** the oscillator pulses, which then pass through gate **L33**.

When the operation selector switch is set at 1P or 1A respectively, only the pulse which results from pushing the 1 pulse–1 addition push button **L38**, or only 20 oscillator pulses immediately following the pushing of the button, reach the on beat circuit. Let us, therefore, consider the circuit containing the 1 pulse–1 addition push button. The symbol designated **A69** (special pulse standardizer) in FIGS. 13 and 29–A indicates a flip-flop with but one stable state (a non-standard flip-flop for the ENIAC) as shown in FIG. 13. The normally positive output of this flip-flop is taken to tube **L37** and the normally negative output is used to reset the same flip-flop immediately after it is set. When the push button is pushed, twin tubes **A–76** (FIG. 13) go off and the flip-flop is set momentarily; otherwise, this flip-flop remains in the normal state. The function of this circuit in producing only a single standard pulse despite flutter or excessive duration of contact at the switch **L38**, has been explained at 1.2.12.

When the operation switch is set at 1P, neither the continuous nor the 1 addition time relay is activated, so that contacts 6, 4, and 2 are closed. The circuit through contact 2 connects the cathode of tube **L37** to —40 v. so that, with the flip-flop of **A69** in the normal state, tube **L37** is on. The negative output of this tube holds **L33** closed. Only when the push button is pushed is tube **L37** turned off so as to open gate **L33**. The positive pulse from tube **L37** also pases through the adjacent tube **L37'** and, through contacts 6 and 4, is delivered to the pulse standardizer **L2** and, finally, gate **L33**. This pulse transmitted from gate tube **L33**, is propagated through one stage of the cycling ring **L14** according to the stage of that ring last activated, and through respective channels as described in reference to the sources of pulses, earlier herein (see 3.1.5).

In 1 addition time operation, contacts 5, 4, and 2 are closed. The circuit through contact 2, as described above, causes gate **L33** to be opened momentarily when the 1 pulse–1 addition time button is pushed. The circuit through contacts 5 and 4 delivers the oscillator's pulses to the pulse standardizer and the gates **L34** and **L33**. The first oscillator pulse passes through gate **L33**. This pulse results, finally, in cycling the ring from stage zero to stage 1 so that the subsequent 19 pulses from the oscillator pass through gate **L34**. When the ring reaches stage zero again, **L34** is closed and **L33** does not open again unless the 1 pulse–1 addition button is pushed. In case the cycling unit has been running in the 1 pulse time mode and is switched into the one addition time mode in the midst of an addition time cycle, the pulses and gates for the remainder of the addition time are given out immediately (since gate **L34** is open), whether or not the 1 pulse–1 addition button is pushed.

Controls are provided which enable the operator to control the method of operation of the cycling unit when he is standing near some unit different from the cycling unit. The PA, 1A, and Cont. input terminals or sockets **L41**, **L42** and **L43** respectively on the panel front shown in FIG. 28 make this possible. One or more portable push buttons may be used in connection with these terminals by plugging them into respective program lines (with no load box) which are in turn connected temporarily by suitable short plug-in lines to respective terminals PA, 1A, and Cont. on the panel, as required.

A push button connected to terminal **L41** parallels the 1 pulse–1 addition time push button **L38** as in FIG. 29A. Portable push buttons connected to the "1A" or "Cont." terminals can be used only when the operation selector switch **L29** is set at "1P," since, with either of the settings, the mode of operation of the respective circuit, is locked so that it cannot be entered except by opening at the operation selector switch **L29**. Closing the portable button connected to terminal **L42** causes the 1 addition time relay **L32** to be activated; closing the portable button connected to the Cont. terminal **L43** causes the continuous relay **L31** to be activated.

3.3 *The Cycling Ring*

The cycling ring **L14** controls synchronization of all pulses in the ENIAC. The operation of the ring has been described in principle in Sections 1.2.5 and 1.3.3. The following description will show in detail the means for deriving all the time pulses of FIG. 2.

3.3.1. *The Tens Pulses (10P)*

When the ring is on stage 0, its associated gate **L16'** is open. Thus the first pulse of the addition time passes **L16'** and sets the flip-flop **L13**. This flip-flop must open gate **L12** inside of 2.5 microseconds in order to pass the first of the tens pulses arriving from **L15** in the off-beat pulse former. Thus, this is not a standard flip-flop; that is, the triggering tubes are omitted in order to improve

the time constant. Also, the output time constant is less than for a standard flip-flop.

The output of gate L16′ also goes on line L44 to trigger the scope L45 which is located on the cycling unit (see FIG. 28). This gives one vertical sweep each addition time on the scope.

The flip-flop L13 remains set until the ring reaches stage ten and the output of the gate L16 resets the flip-flop. Note that in order to not pass more than ten pulses the flip-flop must reset in less than 2.5 microseconds.

The output of L12 goes to a two stage amplifier L47 and thence to two transmitter plug-in units L27. A transmitter L27 consists of two stages with five tubes operating in parallel in each stage.

3.3.2. *The 1, 2, 2′, 4 and 9 Pulses*

The one pulse (1P).—When the ring is at stage one its associated gate L18 is opened to pass a one pulse. The pulse goes through an amplifier system generally indicated at L48 and L49 to a transmitter plug-in unit L27.

The two pulses (2P).—Stages two and three of the ring open their associated gates to pass pulses to form the two pulses. After being preamplified at L49, they are combined and further amplified at L48, and then fed to a transmitter plug-in unit L27.

The two-primed pulses (2′P).—Stages four and five open their associated gates which pass pulses to make up the two-primed pulses. As with the two pulses these are amplified and taken to a transmitter plug-in unit L27.

The four pulses (4P).—Stages six, seven, eight, and nine open their associated gates to pass pulses which make up the four pulses. These are amplified and taken to a transmitter plug-in unit L27.

The nine pulses (9P).—The one, two, two-primed, and four pulses are taken to buffers L51 and then combined to make up the nine pulses. Then they pass through a two stage (six tubes in parallel) amplifier L50 and then to four transmitter plug-in units.

3.3.3. *The One-Primed Pulse (1′P)*

Stage ten opens two gates L16 and L53. Gate L16 passes a pulse which resets the tens pulse flip-flop. Gate L53 passes the one-primed pulse through amplifiers L49 and then to three transmitter plug-in units L27.

3.3.4. *The Carry Clear Gate (CCG)*

Stage eleven of the ring opens gate L21. This gate passes a pulse which sets the flip-flop L22. The negative output of the flip-flop goes through amplifier tubes L54 to a transmitter plug-in unit L27. When this flip-flop is set this output takes a positive swing and the transmitter gives a positive gate on its output. Note that this amplifier system is direct coupled all the way through. The carry-clear flip-flop L22 is reset when the ring L14 reaches stage eighteen. The length of this carry-clear gate (70 microseconds) is about 1¾ times that needed for carry over in a twenty decade accumulator, that is, when the carry over takes place there may be a string of carry overs from the first decade down to the twentieth. This gives a seven to four safety factor which is somewhat less than the two to one which is attained in most parts of the ENIAC.

3.3.5. *The Reset Pulse (RP)*

Stages 12, 14, 15, and 16 of the ring do not operate any gates. Stage 13 opens gate L24 and passes a reset pulse. The output lead of gate L24 is joined with that of gate L25, the last gate in the ring series, associated with stage 19. Stage 19 opens gate L25 which also passes a reset pulse. Thus, in each addition time there are two reset pulses, one when the ring is at stage 13 and another when it is at stage 19. The outputs of the gates L24 and L25 go through amplifier system A57 to three transmitter plug-in units L27.

3.3.6. *The Central Program Pulse (CPP)*

Stage 17 opens gate L26 which passes the central program pulse (CPP). Since this pulse is used simultaneously more places by far than any other pulse in the ENIAC, it goes through the largest amplifier system. This pulse goes through tubes L58 for amplifying effect, then to a two stage (ten tubes in parallel) amplifier L59, and finally to nine transmitter plug-in units L27 which constitute a two stage amplifier with forty-five tubes in parallel in each stage.

3.4. *The Cycling Unit Oscilloscope*

An oscilloscope L45 whose screen is shown in FIGS. 27 and 28, is built into the cycling unit. The oscilloscope input switch L59 with its 12 positions makes it possible to view any of the groups of cycling unit pulses or gates, the selective clear gate, or any external signal brought to the cycling unit through terminal Ext. below the switch.

The brush of the switch L59 is connected to the vertical sweep circuit of the oscilloscope, whose base is controlled with a sweep and 10 microseconds, or a suitable fraction thereof, while the respective contacts at the switch are connected to respective 1 lines in the trays or trunks carrying the respective kinds of pulse shown in FIG. 2. Particular program pulses, or other signals including the subtract, and carry gate, in any part of a sequence may be brought to the "Ext." position indicated in FIG. 28, by a plug-in lead or "jumper" from the involved line of one of the program trays, or otherwise. These details are sufficiently understood and obvious without illustration.

The main purpose of the oscilloscope is to make possible vertification of the presence of the pulses and to provide a rough check on their amplitudes. When viewed on the screen, the images of the cycling unit pulses and gates on the screen should be approximately an inch high. Because of their reflection in the lines of the synchronizing trunk, the cycling unit pulses and gates seen on this oscilloscope screen do not have the symmetrical square shape shown on the chart below the screen.

IV. ACCUMULATOR

The complete accumulator of the ENIAC is capable of performing the following operations:

(1) Storing a ten digit number along with the proper indication of its sign.

(2) Receiving numbers (positve or negative) from other units of the ENIAC and adding them to numbers already stored, properly indicating the sign of the sum.

(3) Rounding off its contents to a previously determined number of places.

(4) Transmitting the number held, or its complement with respect to 10^{10}, without losing its contents (this makes it possible to add and/or subtract from the contents of one accumulator those of another).

(5) Clear its contents to zero (except for a possible round of five, see 4.2.3).

(6) Information stored in certain accumulators may be transmitted statically to certain other units.

The accumulator serves as a memory and arithmetic unit. Each accumulator can store and operate on a number having as many as 10 digits with its sign indication. Two accumulators can be interconnected by special plugging of their interconnector terminals so that they can store and operate on a signad number with as many as 20 digits. Programming memory is provided by the transceivers of the accumulator's 8 repeat program controls. Repeat switches included in the repeat program controls make it possible for an accumulator to remember that it

is to transmit a program output pulse 1 to 9 addition times after receiving a program input pulse. In addition to 8 repeat program controls, the accumulator has 4 non-repeat program controls which have receivers and can, therefore, receive but not transmit a program pulse.

Because an accumulator is capable of receiving a number or of transmitting the number and/or the complement of the number stored in it, it is capable of performing the operations of addition or subtraction. Repeat program controls on the ENIAC make it possible for the accumulator to receive or transmit repetitively from one to nine times when a given repeat program control is stimulated. Each accumulator has 5 digit input channels through any one of which it can receive a 10 digit signed number. Cable shifters plugged into these input terminals make it possible to receive the incoming number shifted to the right or left. Thus, the accumulator, through repeated addition, can carry out the multiplication of a number by a constant having one or more digits.

The ability to do addition and subtraction and the presence of transceiver units in the accumulator also make it possible for the ENIAC to compare the magnitudes of two numbers in accumulators and, on the basis of this discrimination, choose which of 2 alternative program courses is to be followed.

The accumulator can clear its contents to zero in all decades or can clear so that zero remains in all decades but one and a five remains in that one (clear to 5). The ability to clear to 5 in a given decade combined with the possibility of plugging a deleter into an accumulator's digit output terminal or terminals makes it possible to use the accumulator to round off numerical results.

The static outputs of various stages of the 10 decade counters and the binary PM counter of an accumulator can be connected to other units such as the high speed multiplier or printer so that these units can receive information about the number stored in a given accumulator statically (see Sec. 4.3.3).

An example of static outputs would be those derived from the plate potentials of the tubes in FIG. 5. For any given stage, the potential on the "A" (left in FIG. 5) side of the tube is normally low, and on the "B" side normally high; when the stage is energized—that is, when in the abnormal state—as A_0B_0, the plate potentials are reversed, the "A" side becoming high and the "B" side low. This condition exists as long as that stage is energized, and is therefore called a static condition, even though it may in some cases last for only $\frac{1}{100,000}$ second. During the time of such reversed plate potentials, these potentials may be used to provide an indication for energizing the neon indicating lamps (as is actually done), or may be used to provide a so-called "static" potential for any other purpose. This static potential should be distinguished from a digit pulse, whose duration is only two microseconds, and is therefore five times shorter in duration than even the briefest static voltage.

The registering of ten digit numbers is accomplished by the use of decade ring counters (see 1.2.5 and FIG. 36–B) and a PM (plus-minus) counter. The circuits which carry the various groups of pulses representing numbers and signs (including the decade plug-in units and the PM-Clear plug-in unit except for the clear tubes) will be called the numerical circuits. The accumulator contains common programming circuits which in each operation of the accumulator determine which of the above listed operations the unit performs. The accumulator contains a number of program control circuits (eight repeated program control circuits and four non-repeat program control circuits) which can be used at various times to cause the common programming circuits to make the accumulator perform one of the above operations.

Thus, usually each program control circuit will be used at most once in each sequence of computations whereas portions of the common programming circuits are used each time the accumulator performs an operation. No two program controls are used simultaneously. Actually, by making use of the master programmer it is possible to use one program control circuit several times in a given sequence of computations. The operation performed by the numerical circuits (controlled by the common programming circuits) is determined by the various switch settings of the particular program control circuit used.

When activated by an incoming program pulse (arriving via jumper connections from program trays to the accumulator front panel) the program control circuit provides certain gates to the common programming circuits which in turn supply certain gates or pulses to the numerical circuits and thus, cause the accumulator to perform a certain operation. At the end of the operation (which may last as many as nine addition times if a repeat program control circuit is used) the program control circuit gives out a program pulse which may be taken to other units of the ENIAC causing them to perform the next step in the sequence of computations.

The following topics regarding the accumulator will be discussed in this chapter: Sec. 4.1, program controls; Sec. 4.2, common programming circuits; Sec. 4.3, numerical circuits; Sec. 4.4, use of accumulators for fewer or more than 10 digit computations; and Sec. 4.5, problems illustrating the use of accumulators. References will be made principally to the following diagrams:

Accumulator Front View	FIG. 31.
Accumulator Front Panel	FIG. 32.
Accumulator Block Diagram	FIGS. 33–A to C.
Accumulator Cross-section	FIGS. 36–A to E.
Use of Dummy Programs	FIG. 37.

4.0. *General Summary of the Accumulator*

This description of an accumulator will be given principally in terms of the block diagram FIGS. 33–A, 33–B, 33–C, 31, 32–A and 32–B; but FIGS. 34, 35, 36–A, 36–B, 36–C, 36–D, 36–E, and FIGS. 2 to 14, will be pertinent as to details of the circuit elements, when required. Assembling FIGS. 33–A, 33–B, and 33–C, in the upper center and upper right of the assembly of figures there are eleven rectangles representing the ten decade plug-in units and the PM-clear unit (on the left). Just to the left of the PM-clear unit are seen the five decks of the significant figure switch. In the lower left hand corner are seen one receiver plug-in unit and two transceiver plug-in units. As indicated in the drawing there is one other receiver plug-in unit and six other transceivers making a total of four receivers located on two plug-in units and eight transceivers each located on a separated plug-in unit. Below the decade units are the α, β, γ, δ, and ϵ input gates of which only α and ϵ are shown in detail.

As indicated above, the circuits of an accumulator are divided into three groups for purposes of explanation. First, there are the program control circuits which comprise the circuits of the receiver and transceiver plug-in units, N4′ and N7, their associated switching circuits, and the repeater plug-in unit (FIG. 33–B). Second, the common programming circuits connect by means of interconnection plugs (see, for example, the terminals marked ST6, 7, and 8 on the left edge of FIG. 33–A to the program control circuits. Third and last, there are the numerical circuits which extend from the input plugs SV1, . . . , SV5 (bottom of FIG. 33–C) through the decades and PM unit to the output plugs SW1 and SW2 (at the top of FIGS. 33–A and 33–C). The common programming circuits directly control the numerical circuits by opening certain gates and in some cases introducing certain pulses into the numerical circuits. The following table summarizes the gates and pulses produced by the program control circuits and by the common programming circuits.

TABLE 4-1

Program Control Circuits				Common Programming Circuits	
Switch settings			Gates Provided at—	Gates Provided	Pulses Provided
Operation Switch	Clear Switch	Repeat Switch			
α	0	--------	SU1 (numerals encircled in figures.	Carry gate to tubes N14 and N15 in the decades and α input gates opened.	None.
β	C	--------	SU2	Carry gate as above and β input gates opened.	
A	0	1	SU10	Gates N17 and N17' opened	1' pulse added in first decade.
			SU6	Gates N18 and N19 opened	Tens pulses to cycle decades and Nines pulses for transmission over add output SW1.
AS	0	--------	SU7	Gates N21, N22, N23, and N24 opened.	Tens pulses to cycle decades, Nine pulses for transmission over add output and subtract output, and One-primed pulse for transmission over SW2.
S	0	--------	SU8	Gates N26, N27, and N28 opened.	Tens pulses to cycle decades, Nines pulses for transmission over subtract output, and One-primed pulse for transmission over SW2.
A	C	--------	SU6	Same as for A above	Same as for A above.
			SU9	Opens N29 passing CCG to clear tubes in the PM-Clear unit.	

Each accumulator has 12 program controls N1 (FIGS. 31 and 32). Four of these are non-repeat program controls; eight are repeat program controls. Each of these 12 program controls has an operation switch N2 for specifying the operation (receive, transmit, or neither) which the accumulator is to perform and a clear-correct switch N3. In addition, each non-repeat control has a receiver N4' (FIG. 33-B) with a program pulse input terminal N6; each repeat program control has a transceiver N7 with program pulse input (N8) and output (N9) terminals and a repeat switch N10. Neons associated with the 4 receivers and 8 transceivers are shown in FIG. 31 at N11.

The 12 program controls operate common programming circuits as instanced in Table 4-1 preceding (see also FIG. 33-B), the receive circuits, the transmit circuits, the clear circuits (including the significant figures switch N78 (FIGS. 32 through 33-A) and selective clear switch (N79), and a circuit which enables the accumulator to pick up the 1'P (see B on Table 4-1). The repeat switches of the 8 repeat program controls also operate in conjunction with the 9 stage repeater ring circuit N110. The repeater neons (see FIG. 31) are correlated with the stages of the repeater ring.

The programming circuits common to all 12 program controls operate the accumulator's numerical circuits (see FIG. 33-B). The accumulator's numerical circuits consist of 10 decade plug in units N31' and a PM-clear plug in unit N39 (FIGS. 33-A and C).

Each decade plug in unit includes a pulse standardizer N30 at its input, a decade (10 stage ring) counter N31, a decade flip-flop N32, a stage nine gate N33, reset pulse gate N34, carry over gates N14 and N15, A and S output gates (N35 and N36 respectively) and transmitters N37 and N38, and several inverter tubes specifically referred to later herein. Each decade counter stores 1 digit of a number and plays a part in the reception or transmission of one digit of the total of 10 digits that the accumulator can handle as explained in Sec. 1.3. The decade flip-flop N32 has 2 purposes: (1) In reception it remembers if carry over is to take place; (2) in transmission it controls the A and S output gates N35 and N36. Gates N33, N34, N14 and N15 participate in the carry over process. Gate N34, moreover, controls the resetting of the decade flip-flop. The decades are numbered from right to left, and decade 1 is the unit's decade, and the 10^9 decade is the tenth decade. There is a neon bulb associated with each stage of a decade counter and with the decade flip-flop (see FIGS. 31 and 36-B).

The PM-clear unit N39 contains a binary ring (PM) counter N41, A and S output gates N35 and N36' and transmitters (N40 and N43 for the plus and minus output, a pulse standardizer, and nine amplifier tubes 39' in multiple order, for the clear signal (which is delivered through a buffer 39''). There is also a special transmitter N46 for the 1'P used when the accumulator transmits subtractively. The PM counter has stage P for positive numbers, and stage M for negative numbers (which are treated as complements in the ENIAC). It should be noted that pulse input to the PM counter can come not only from the PM lead of a digit input terminal (over line N47 or N48), but also can result from carry over from the 10th decade. This latter fact makes possible the correct addition or subtraction of signed numbers as explained in Sec. 1.3. Neons correlated with the stages P and M counter are shown in FIG. 31 at the left of the digit neons. Their activation circuits appear in FIG. 4.

The negative of a number is represented in the ENIAC by the complement of the number with respect to 10^{10}. An accumulator stores the number $-2\ 345\ 098\ 765$ in the form $M+(10^{10}-2\ 345\ 098\ 765)$ or, $M+(7\ 654\ 901\ 235)$.

The decade counters and PM counter transmit their digit outputs through either or both of 2 terminals, the A (add) and S (subtract) output terminals N49 and N51, respectively (at the top of FIGS. 33-A and 33-C). The number stored in an accumulator is emitted over the A terminal; the complement, over the S terminal. The counters can receive their inputs from any one of 5 input terminals identified by the letters α, β, γ, δ, ϵ. The decade counters and the PM counter of an accumulator receive or transmit the information for all 10 digits and sign simultaneously (the transmisison of the pulses for each digit is, however, serial).

4.1. *Program Controls and the Significant Figures and Selective Clear Switches*

Suppose that a program pulse arrives at a non-repeat program input terminal (N6) (lower left corner of FIG. 33-B). This positive pulse will cause tube N52 to become conducting. The drop in plate voltage there will send a negative pulse into associated flip-flop N4 causing it to be set. The indicated polarity of the output of N4 will then be reversed and inverter N53 will go off (become nonconducting), causing the cathode follower N54 to go on (for circuit details see FIG. 35). The output of N54 comes from the cathode; therefore giving now a positive gate voltage on the output. This output goes to deck

3 of the operation switch. If the operation switch is set at α, β, γ, δ, or ε this positive gate voltage appears on the interconnection terminals labeled SU1 to 5 thereabove in FIG. 33–B. If the switch is set at A, AS, or S then the gate appears on SU6, 7, or 8 (lower left in FIG. 33–A). The fast output (cathode follower) is used there since these circuits must be set up before the 10 pulses arrive. The other (right hand) output of the receiver flip-flop N4 (which is positive after being set) opens the gate N56 (that is, allows a pulse on the first grid to cause the tube to conduct) and turns the buffer N57 on. This gives a negative voltage swing on the output which goes through the clear-correct switch N3 if closed, and deck 2 of the operation switch. If the switch is set at α to ε, this signal appears on terminal SU10 (FIG. 33–C) and will cause the correction to take place if SU10 is connected to ST10 thereadjacent. If set at O, A, AS, or S the signal-through the second deck turns the inverter N58 off and the buffer N59 on, giving a negative gate across SU9—ST9 and will cause the accumulator to clear. After the gate N56 in the receiver is opened, the CPP (Central Program Pulse) arriving at the end of the addition time resets the flip-flop N4. The time constants are such that gate N56 does not open in time to cause any conflict with the CPP which activates the receiver.

Now, suppose a program pulse arrives at a transceiver, say at input terminal N8. As in the receiver, this pulse-acting through a buffer N5, sets the flip-flop N61, and within 15 μs, the now negative output at the left of this flip-flop produces the positive gate from cathode follower N54' through deck 3 of the operation switch to the interconnection terminals SU1 to 5 or SU6, 7, or 8 with the alternate settings mentioned for the non-repeat circuit. This follows the practice that circuits are designed to operate in not more than half of the time which would suffice. Actually, the time constants for these circuits depend upon the setting of the program switches. The maximum time constant occurs on a circuit when two accumulators are interconnected to form a twenty digit accumulator and all program switches are set to activate that circuit. The other (right hand) output (which is now positive) of the flip-flop N61 turns the buffer tubes N62 on and opens the gate tube N63 (for circuit details see FIG. 36). If the clear switch N3 is setting on "C" (clear or closed), the negative gate output of tubes N62 goes through two decks of the operation switch and appears at SU9 and at SU10. The two tubes N58 and N59 are in the line from the receivers to raise the circuit to the D.-C. voltage level of outputs of the transceivers. The negative gate from the right hand buffer N62 in the transceiver will turn the inverter N64 off giving a positive swing to one of the grids of the gate tube N66. Later central program pulses (CPP) arriving at gate tube N66 will now be passed on into the repeater ring. They go through the pulse standardizer N67, and step the ring. If the repeat switch is set at 3 (as illustrated), then in the third addition time the ring N110 will have been stepped to stage three, giving a positive gate output through the repeat switch N10 to the gate tube N63 in the transceiver. Note, that one repeater ring is used by all the repeat program controls. The gate N63 causes the inverter N68 to go off, opening the gate N69 and turning the buffers N71 on. The negative output from the left one of the buffers N71 goes through the clear switch N3 and the operation switch giving a negative gate at SU 9. The output of the right buffer N71 turns the tube N73 off opening the gate N74 (this process of opening gate N74 takes about 100 microseconds). The CPP near the end of the third addition time passes this gate and turns the inverter N76 off (it over-rides the stepping pulse from N66 clearing the repeater ring back to stage one). The gate N69 being open, the central program pulse arrives here also at the end of the third addition time, resets the flip-flop N61 and feeds through the transmitter N77 giving a program output pulse at N9 which can be used to operate some other unit during the fourth addition time.

As stated earlier, each accumulator has 12 program controls: four non-repeat controls (consisting of receiver with program pulse input terminal, operation switch and clear-correct switch) and 8 repeat controls (consisting of transceiver with program pulse input and output terminals, operation switch, clear-correct switch, and repeat switch). In this section the possible settings and uses of program control switches will be described. The significant figures switch and selective clear switch which are more properly classified as part of an accumulator's common programming circuits are also described here. The switches are shown in FIG. 32. Neons correlated with the 12 program controls are shown in FIG. 31.

4.1.1. *The Operation Switch*

The operation switch N2 has 9 positions: α, β, γ, δ, ε, O, A, AS, S. If the operation switch of a stimulated program control is set at one of the settings α, β, γ, δ, or ε, the accumulator receives the pulses representing any number transmitted over the digit tray to which the corresponding digit input terminal SV1 to SV5 (bottom of FIG. 33–C) is connected. Obviously, if that input terminal is not connected to a digit tray or is connected to a tray not carrying pulses at the time the control is stimulated, the accumulator receives no pulses. This point will be referred to in Sec. 4.1.2, in connection with the clear-correct switch.

If the operation switch is set at A, S, or AS, the accumulator transmits its contents, the complement of its contents or both respectively when the control is stimulated.

The setting O of the operation switch top deck instructs the accumulator to neither receive nor transmit. This setting is useful on non-repeat or repeat control operation switches when it is desired to clear an accumulator without receiving or transmitting (see Sec. 4.1.2). When set on the operation switch of a repeat program control, the setting O provides a means of obtaining a program output pulse delayed from 1 to 9 addition times without, however, disturbing the contents of the accumulator. (See the discussion of dummy programs in Sec. 4.5.1.)

4.1.2. *The Clear-Correct Switch*

The clear-correct switch N3 can be set at either C ("clear," closed) or O (open). The accumulator's interpretation of the setting C depends on the setting of the associated operation switch.

If a program control's operation switch N2 is set at one of the transmit settings (A, S, or AS) or is set at O when a stimulating pulse reaches it, the accumulator clears, either to zero in all decades, or to zero in all decades except one in which it clears to 5. The setting of the significant figures switch N78 (see Sec. 4.1.4) determines whether clearing is to zero or 5 and, if to 5, in which decade the 5 appears.

With the operation switch set to a receive setting, α, β, γ, γ, or ε, the setting C of the clear-correct switch N3 gives the instruction "pick up the 1'P from the synchronizing trunk and put it in the first decade." If there are no digit pulses coming to the digit input terminal SV1 through SV5 when the control set up in this way is stimulated, the accumulator simply picks up the 1'P. If there are actually pulses coming to the digit input terminal, these are first received and then, when the cycling unit emits the 1'P, this pulse also is picked up and put into the first decade. A "receive-C" program in which digits are received and the 1'P is picked up is, however, not possible when the digits are being transmitted as a complement from another unit in such a way that the 1'P from the digit tray also arrives in units place. (See Sec. 4.3.1.)

There are at least three occasions when the "receive-C" setting of a program control proves useful. If a given

accumulator is being used to store the independent variable, the accumulator can be programmed to pick up the 1'P whenever it is desired to increase the value of the independent variable by one (see the illustrative problem of Chapter VIII). In some problem set-ups, an accumulator may receive from the S output terminal of the product, quotient, or two root accumulator, a complement with respect to 9 in all decades instead of a 10^{10} complement (see Chapters V and VI and Sec. 4.3.1). Also, an accumulator may receive a complement from a second accumulator shifted to the right en route so that the original 1'P needed to make a tens complement (see Sec. 4.3.1) is lost. The missing pulse, in either case, can be picked up through a "receive-C" program.

4.1.3. *Repeat Switch*

The repeat switch **N10** (found only on repeat program controls) can be set to any number between one and nine inclusive. The accumulator carries out whatever operation is set on the associated operation switch as many times as is specified by the setting of the repeat switch. Each repetition requires one addition time so that if the repeat switch of a control is set at r ($1 \leqslant r \leqslant 9$), r addition times must be allowed for the program set up on that control. The transceiver of a repeat program control emits a program output pulse at the end of r addition times.

It is to be noted that if the clear switch **N3** of a repeat program control is set at C in connection with an O or transmit setting of the operation switch, clearing of the accumulator takes place but once, at the end of the r^{th} addition time. The setting C in connection with a receive setting of the operation switch of a repeat program control causes the accumulator to pick up the 1'P in each of r addition times.

If the number a is stored in one accumulator and the number b is another accumulator, $a \pm rb$ (where $1 \leqslant r \leqslant 9$) may be formed in the first accumulator through the use of a repeat program control on each accumulator. The operation switch of the control on the first accumulator should be set at a receive setting and the repeat switch, at the value of r. The operation switch of the second accumulator's control should be set at A (if $a+rb$ is to be formed) or at S (if $a-rb$ is to be formed) and the correlated repeat switch, at $R \geqslant r$.

In a similar fashion, it is possible to form $a+b\Sigma r_i 10^{k-i}$. In this case where the coefficient of b has more than one digit, shifters (see Sec. 11.3) are used to effect multiplication by powers of 10. Notice that if the coefficient of b has p digits, p program controls will usually have to be used on the receiving accumulator but fewer than p may suffice on the transmitting accumulator. For example, $234b$ may be formed in an accumulator through the use of one program control (set-up to transmit additively 9 times) on the transmitting accumulator. Three program controls must be used on the receiving accumulator: one set up to receive, say on α, 4 times; another set up to receive on β, 3 times; a third set up to receive on γ, twice. A shifter which shifts numerical data 1 place to the left should be used at the β input terminal and one which shifts numbers two places to the left, at the γ input terminal of the receiving accumulator. As an example of the circumstances under which fewer than p program controls suffice on the transmitting accumulator, consider the case of forming $998b$. This can be done by programming the accumulator which stores b to transmit subtractively twice and then addtively once and by programming the receiving accumulator to receive twice thru an input terminal with a shifter and once thru an input terminal with a shifter that displaces data 3 places to the left (i.e., form $998b$ as 10^3b-2b).

4.1.4. *The Significant Figures Switch*

The significant figures switch **N78** is a part of the common programming circuits which function when the accumulator transmits subtractively or when the accumulator clears. The significant figures switch has eleven positions, 0, 1, . . . , 10. These numbers refer to the number of significant figures, counting the decades toward the right from the PM counter, to be retained in the accumulator.

If the significant figures switch on an accumulator is set at a number, s, for instance ($0 \leqslant s \leqslant 10$), when clearing takes place, decade $10-s$ (i.e., the $s+1^{st}$ decade from the left) clears to five and all other decades to zero. When a single accumulator is used, this means that the accumulator is cleared to zero in all decades if its significant figures switch is set at 10. If two accumulators (see Sec. 4.4.2) are interconnected to form a 20 decade accumulator, the setting 10 on the left hand accumulator causes it to clear to zero in all decades; the right hand accumulator then clears in accordance with the setting of its own significant figures switch. For example, if 11 significant figures are to be stored in the 11 left hand decades of a 20 decade accumulator, the significant figures switches of the left and right hand accumulators respectively are set at 10 and 1.

The setting of the significant figures switch also determines the decade place into which the 1'P is put when an accumulator transmits subtractively. With the significant figures switch of an accumulator set at s, the 1'P is transmitted over the lead for decade place $11-s$, i.e., the s^{th} decade place from the left. If the significant figures switch of an accumulator is set at 0, this means that the 1'P is not transmitted when subtractive transmission takes place. It is to be noted that the 1'P is picked up and put into units decade of an accumulator (which, in the case of 2 interconnected accumulators, means the 20th decade from the left) when a "receive-C" program control is stimulated regardless of the setting of the significant figures switch.

Notice, that as far as rounding off a number in an accumulator is concerned, the setting of the significant figures switch provides only for getting the correct s digits from the left. The significant figures switch setting has nothing to do with deleting the non-significant digits at the right. The operator provides for the deletion of non-significant figures by placing a deleter at the output terminal or terminals of the accumulator storing s significant figures (see Sec. 11.2). When printing of an s significant figure result is to take place from an accumulator and the non-significant figures at the right have not been deleted, deletion can be provided for in the set up of the card punch plug board.

4.1.5. *The Selective Clear Switch*

The selective clear switch **N79** (FIGS. 32, 33–A) has two positions, SC and O. When the selective clear signal is transmitted from the initiating unit (see Chapter II), all accumulators whose selective clear switches are set at SC clear; those accumulators whose selective clear switches are set at O do not clear.

4.2. *Common Programming Circuits*

4.2.1. *The Receive Circuits*

The receive circuits cause the accumulator to add to its present contents any ten digit signed number arriving through the input plugs **SV1** to **SV5**. This addition is accomplished by opening the proper set of receiving gates **N81** (FIG. 33–C), and by providing for the carry-over between the various decades.

Suppose that any activated program control has its operation switch **N2** set on α. This applies a positive gate to **SU1** (FIG. 33–B) through deck 3. The interconnector cable carries this to **ST1**, then it will cause tube **N82** to conduct and turn off the inverter **N83**. The positive gate from **N83** opens the gate tubes **N81** of the alpha group (FIG. 33–C), and any digit or PM pulses arriving at the plug **SV1** will be transmitted into the corresponding decade or the PM unit. Also, the positive gate from **ST1** will open the gate tube **N84** allowing the carry-clear gate (CCG) to be passed to the multiple in-

verters N86 which give out a greatly amplified positive pulse. The output from these inverters then opens the carry gates N14 and N15 in each decade. This carry-over will be explained in detail when the numerical circuits are taken up (see Sec. 4.3.1).

If the clear switch N3 is set on C (closed) and the operation switch on alpha, then a negative gate will be applied to inverter N87 turning it off and opening the gates N17 and N17'. This passes the 1' pulse through the interconnector terminals $ST_2$14 and 15 and by-pass 16 into the first decade of the accumulator. This provides for the correction of negative numbers where some of the last digits have been lost by the use of deleters, as will be explained later.

4.2.2. *The Transmit Circuits*

Suppose the operation switch of an activated program control is set at AS. Then a positive gate will be transmitted through deck 3 to SU7 and be transferred by the interconnector jumper to ST7 and the AS (add-subtract) lead. Then it will open the gate tubes N21, N22, N23, and N24. N21 will pass the cycling pulses (10P) to the inverter N88 and the cathode follower N89. The output of N89 operates the buffers N91 (one adjacent each decade), resulting in the decade being cycled from whatever stage they may register at, through all ten stages back to where they started. Gate tube N22 will pass the 9 pulses to the inverter N92 and the cathode follower N93. From there these pulses go to the gate tubes N36 in the decades and the PM unit N36'. Similarly, tube N23 will pass 9 pulses through N94 and N95 to the gates N35 of the decades and N35' of the PM unit. Tube N24 passes a 1' pulse through the transmitter N46 in the PM unit to the inter-connection terminals SU_1—ST_1–17. From there it goes to the significant figure switch and into one of the output terminals of the subtract output SW_2 (at the extreme right of FIG. 33–C).

If the operation switch is set at A then through deck 3, the cycling pulses (10P) after crossing terminals SU—ST6, are passed by gate N18 (FIG. 33–A), and the 9 pulses (9P) are supplied to the add gates N35 of the decades and the PM unit by the gate N19. If the operation switch is set at S, then through the 3*d* deck the cycling 10P pulses are passed by N26 and 9 pulses are sent to the subtract gates N36 of the decades and N36' the PM unit by gate N27; also, N28 provides the correction pulse (1'P). If the clear switch of the activated program control is set at C then at the end of the operation (one addition time in the case of receivers and one to nine addition times in the case of transceivers, depending upon the setting of the repeat switch), a negative gate voltage will appear at SU9 and from ST9 it will turn off the inverter N96 opening the gate N29. This passes a carry-clear gate (CCG) to the clear tubes (1 to 10 in the PM-Clear unit).

4.2.3. *The Clear Circuits*

For purposes of rounding off numbers the decades of an accumulator are provided with clear-to-five circuits. To the left of the PM unit in FIG. 33–A, is seen the significant figure switch N78. The setting of this switch determines which decade clears to 5. All other decades clear to zero. For example, to round off to three significant figures the seventh decade is cleared to five before the number to be rounded off is put in the accumulator.

Inspection of a decade plug-in unit in FIG. 36 (A and B) shows that clearing any stage in the ring is accomplished by a direct connection to the clear tubes 39' in the PM unit labeled "clear T," and a return circuit labeled "clear R" which returns to a suitable resistance (not shown). The block diagram shows that all stages except zero and five connect directly to the clear tubes and the resistance, whereas, stages zero and five connect to four decks of the significant figures switch (decks 1, 1A, 2, 2A). The significant figures switch effectively reverses the connections to the zero-five leads in the decade (set by switch N78) causing that decade to clear to five instead of zero.

If an accumulator is stimulated to transmit and clear, a signal from buffer N57 of receivers or buffer N71 (left tube) of transceivers is applied to gate N29 so that the carry clear gate (CCG) is passed to the PM-Clear unit. The clear signal from the PM tubes goes directly to the upper connections of stages 1, 2, 3, 4, 6, 7, 8, and 9 in all decades causing these stages to be flipped into the normal state. With the significant figures switch set at *s*, the signal from the clear tubes is routed through deck 2A to the upper lead of the zero stage in decade 10–S and through deck 1 to the upper connection to stage 5 in all decades except decade 10–S. Decks 1A and 2 of the significant figures switches are return circuits from the flip-flops. Thus, stage zero is left in the excited state in all decades except decade 10–S in which stage 5 is left in the excited state.

The clear signal arises by a carry-clear gate (CCG) being passed by tube N29 to the inverter N98 and thence to the buffer tube 39'' and amplifier tube group 39' in the PM unit. If the accumulator is being used with the multiplier or divider this clear gate may be introduced directly into the PM unit as illustrated. The gate tube N29 will be opened to pass a carry-clear gate in the following cases.

(*a*) If the ENIAC is to be initially cleared the initial clear gate (ICG) arrives through the buffer N99, which produces a gate pulse at gate tube 29 to open the latter.

(*b*) If the accumulator is set at N79 to selective clear and the selective clear gate (SCG) is provided at the initiating unit (see 2.4.), then the inverter N96 is turned off by the signal from the buffer N101, opening gate N29.

(*c*) Or, if the program control switch of an activated program circuit is set to O, A, AS, or S and the clear switch to C, then, at the end of the operation, a negative gate appears at ST9 which turns off the inverter N96 and opens the gate N29.

The ICG also clears the repeater ring N110 back to stage one by gating a CPP at N74.

4.2.4 *Interconnection Features (FIGS. 31, 32, 32–A and B, and 33)*

The outputs of the program control circuits appear at terminals SU located on the front panels. Just above these are the terminals ST. It is expected that the usual plan will be to operate as a ten digit accumulator. In this case a vertical jumper N–102 is plugged from the terminal SU1 to the one ST1 (FIGS. 32 and 32–A) and a load box N103 is placed in ST2. This effectively connects together the respective interconnector terminals SU and ST located next to each other on the block diagram FIG. 33. In case of twenty digit operation all the program controls must operate in parallel; this means that the load resistors for these circuits cannot be built in, since what is correct for separate operation would not be correct when they are operating in parallel. Thus, the load resistors are on a unit which is plugged into the front panel. Only one such unit is used with each accumulator or with each pair of accumulators when connected to form a twenty-digit accumulator.

If two accumulators are to be interconnected to form a twenty digit accumulator then the terminals SU2 and ST2 of the left hand accumulator are jumper-coupled respectively to SU1 and ST1 of the right hand one by horizontal jumpers N104; SU1 of the left hand is jumper-connected to ST1 of the left hand by vertical jumper N102, and a load box N103 is placed in ST2 of the right hand accumulator as shown in FIG. 32–B. This makes the carry-over from the tenth decade of the right hand accumulator go into the first decade of the left hand one and the 1' pulse (correction pulse) go into the first decade of the right hand accumulator. The "10" output of the significant figure switch of the left hand accumulator goes

to the input of the significant figure switch of the right hand accumulator. The "0" output of the right hand significant figure switch goes to the input of the units decade of the left hand accumulator.

A list of connections for ten and twenty digit operation are given in Tables 4–2 and 4–3. Note that the PM unit of the right hand accumulator is not used in twenty digit operation.

TABLE 4-2.—VERTICAL INTERCONNECTOR CABLE

[Just one used for either a 10 or 20 digit accumulator]

SU_1	ST_1	
1	1	These connections enable any program control circuit to cause the common programming circuits to make the accumulator receive on channels.
2	2	
3	3	
4	4	
5	5	
6	6	These connections enable any program control circuit to cause the common programming circuits to make the accumulator transmit on A, AS, or S.
7	7	
8	8	
9	9	This connection takes care of the clearing action.
10	10	This connection provides for the correction pulse.
11	11	
12	12	
13	13	This connection in the ST_1 end takes the carry of the 10th decade into the input of the PM unit.
14	14	
15	15	
16	16	This connection takes the correction pulse transmitted by the transmitter N46 in the PM-Clear unit to the input of the significant figure switch. Terminal 18 is a ground connection in each case.
17	17	
18	18	

Note that the load box plugs into terminal ST_2 and has jumpers which connect terminals 14 and 15 and 16 and 17. This takes the correction pulse into the units decade input (units decade of right hand accumulator in case of twenty-digit operation) and the 16 to 17 connection takes the "10" output of the significant switch to the units channel of the subtract output.

TABLE 4-3.—HORIZONTAL INTERCONNECTOR CABLE

SU_1	ST_1	
1	1	These connections cause any program control to cause the two accumulators to act in unison when receiving on α to ϵ.
2	2	
3	3	
4	4	
5	5	
6	6	These connections cause the accumulators to act in unison when transmitting on A, AS, or S.
7	7	
8	8	
9	9	This connection causes the clear circuits to act in unison.
10	10	This connection allows any program control to provide the correction pulse at terminal $ST_2$14 of either accumulator.
11	11	
12	12	
13	13	
14	14	
15	15	For upper cable this connection takes the output of the 10th decade of right hand accumulator to 1st decade input of the left hand accumulator.
16	16	This connection in upper cable takes "0" output of significant figure of right hand accumulator into the units channel of the subtract output of the left hand accumulator.
17	17	This connection takes "10" output of the significant figure switch of the left hand accumulator to the input of the significant figure switch of the right hand accumulator.
18	18	Terminal 18 is a ground connection in all cases. The connections 15, 16, and 17 serve no purpose in the lower interconnector cable (between terminals SU_1 and SU_2).

4.2.5. *Circuit for Admitting the 1'P to Units Decade*

A signal from the normally negative output of a transceiver's flip-flop, through a buffer **N57** or **N62** and then passing through the clear correct switch and one of the receive points on the operation switch reaches gates **N17** and **N17'** (FIG. 33–C, right) after passing through the inverter **N87**. These gates, when opened, allow the 1'P to pass through to the units decade of the accumulator.

4.2.6. *Repeater Ring Common to Repeat Program Controls*

The eight repeat program controls **N7** on an accumulator operate the 9 stage repeater ring circuit **N110** in common. A signal from the normally negative output of the flip-flop **N61** of such controls and then through buffer **N62** (right) opens gate **N66** so that a CPP can reach the repeater ring **N110** to cycle it one stage per addition time. When the ring reaches stage γ, the output signal from this stage, passing through a corresponding point y on the repeat switch, causes gate **N63** in the transceiver to emit a signal. The signal from **N63** opens gate **N69** which passes a CPP. The resulting pulse resets the transceiver's flip-flop and passes through the transmitter as a program output pulse. The signal from gate **N63** through N71 (right) also opens gate **N74** so that a CPP passing through it clears the repeater ring back to stage 1 at the same time as the transceiver is emitting a program output pulse.

4.2.7. *Tray Structure and Use*

Among the prime essentials of intercommunication between and among the units of the ENIAC are the digit and program trays.

As shown in FIGS. 31–C and 31–A, respectively, both the digit trays **N111** and the program trays **N112** are in the shape of shallow elongated rectangular open pans of sheet metal, eight feet long, 9 inches wide from front to back and 1.25 inches deep. The sides and ends are vertical walls of uniform height. When the trays are stacked on brackets at the front of the ENIAC, one on top of another, as shown in the elevations of panels of many of the units in the accompanying drawings, the wires therein are actually shielded on all sides. There are from one to nine digit trays stacked before the units of the machine according to maximum need at given locations, and only those needed for particular setups of the machine are utilized. The uppermost one may have a cover if desired. Each tray carries eleven parallel well spaced wires, separated electrically from each other by insulation and by vertical planiform sheet metal shields or partition walls **N113**, extending longitudinally in the trays, the top edges of which are at the same level as the tops of the sides and ends.

Gang receptacles **N114** are mounted in the front walls of both program and digit trays near their extreme ends, each having 12 sockets to receive twelve-blade gang plugs, **N115**, one at each end of jumper cables **N116** by which longitudinally aligned trays may have their wires mutually connected to form eleven series-connected lines or busses, and constituting trunk systems for program transmission or trunk systems for transmission of digit pulses or for transmitting the cycle of pulses from the cycling unit by which the operations of the whole system are synchronized, and which supply actual pulse origins when admitted to units by stimulated gates. One of the sockets in each receptacle and one blade of each plug serve to complete a ground lead.

The digit trays **N111** have additional similar receptacles **N117** at intervals corresponding to the width of the panels (which are two feet wide). From the contacts in these plugs taps **N118** are extended to respective wires in the tray, so that a jumper as last mentioned and of proper length may be plugged into the front of the tray where most convenient and into the appropriate receptacle (as $SV1_a$ of FIGS. 32 and 33–C) of the panel, by which signals from the bus lines of the tray are communicated to respective terminals of the unit constructed on the panel.

The program tray **N112** differs from the digit tray in that only 12-gang plugs are used to connect the digit tray to a panel unit, whereas the program tray must have provision for connecting any of its wires to an input of the panel unit. For this purpose, instead of duplicating the 12-gang receptacles, as in the digit tray, a corresponding number of groups of individual receptacles **N119** are set in the front wall of the tray, from which respective taps **N120** are extended to respective wires in the tray. The jumper **N121** in this instance may comprise either a single wire with appropriate plug on each end one of which is inserted in the proper socket **N119** of the tray and the other in a similar socket (as, 5_i, 5_o, -12_i, 12_o, etc., FIG. 32, and $SxSy$, FIG. 51) on the panel, or two wires may be used, with corresponding receptacles, one of which may be a ground connection.

The wires of at least one digit tray are connected respectively to the 10P, 1P, 2P, 2'P, 4P, 9P, 1'P, C.C.G., R.P., C.P.P. and S.C.G. output leads of the cycling unit, so that this and its series-connected trays become the "synchronizing trunk" named from time to time in this specification (see FIG. 29–B and Section III, 3.3, et seq.).

The right-hand ends of trays N111 and N112 (beyond the break in the drawing) are depicted without the conductors in order to better show the shielding and supporting members.

4.2.8. *Plug-In Unit Details*

Throughout the ENIAC the arithmetical units, the circuits are so laid out and their parts assembled that coordinated circuit groups of convenient size may be connected into the system by means of plugs N115 fixed on the chassis 123 having not more than twelve blades (one set at each end of the chassis) except in a very few cases. All of the blades may not be required in some cases, but the same kind of plug is then mounted on the chassis to serve as an anchor or retainer for the chassis, holding it in place on the brackets of the panel. This kind of a chassis may be seen in the plan and rear view illustration of the decade plug-in unit shown in FIGS. 31–F—31–G. Some of the plug-in unit chassis may be shorter than the decade plug-in unit, and for the mounting of such shorter units similar twelve-blade gang plugs are provided on each end, and matching receptacles with proper circuit leads are mounted in proper locations on the back of the panel. The chassis for all of these plug-in units are similar in being formed of sheet metal, and of rectangular pan-like form with vertical end walls and rear walls. They have approximately the same depth from bottom to top of the walls, and measure the same in most instances from the front wall to the back wall, but vary in length according to the number of tubes and complexity of the circuits required. The decade unit includes not only the ring-of-ten tubes N124, but also the associated pulse standardizer circuit, carry-over circuits, and transmitting circuits and tubes shown in part at N125. This decade unit has 28 tubes, some of which are twin tubes, such as 6SN7, the triodes of which operate either as independent valves, or in flip-flop relation, or otherwise, as required.

The plug-in units are supported on conventional brackets, without permanent fastenings, so that any may be manually removed for inspection, repair and testing, and replaced by inserting the gang plug blades in the corresponding sockets on the panel. The P-M plug-in unit, (not illustrated) is somewhat similar to the decade plug-in unit as to size of chassis, but requires only about 25 tubes.

It is a characteristic of all of these plug-in units that the gang plugs are located at the front sides of the chassis, at respective ends, and all of the tube sockets N125 are mounted in the rear vertical wall of the chassis on horizontal axes. This permit the numerous assembly of plug-in units to be assembled on the rear sides of the panels in close superposed relation, with all of the tubes of the whole machine exposed rearwardly in vertical zones in the panels spaced from the rear covers of the panels so that air may be drawn off at the upper ends of the panels, and admitted through openings are suitable locations in the back covers of the panel so as to impinge effectively on the tubes for regulating the operating temperatures. It also facilitates removal and replacement of tubes without disturbing circuits otherwise, the plug-in units remaining in their positions in most instances when such tube replacements are required.

There are no openings in the bottoms of the chassis, so that there is effective shielding of one plug-in unit from the one next adjacent thereabove or therebelow in a panel unit, as well as an approximately enclosing shield guarding against external disturbance.

4.3. *Numerical Circuits*

4.3.1. *General Description of a Decade Plug-In Unit (FIGS. 33–C and 36–A – 36–B)*

The pulse standardizer N30 (tubes N106, 107, 108 in FIG. 36–A) consists essentially of four triodes (N–106 being a double triode 6SN7. (See also FIG. 12 and detail description thereof.) The output of tube N107 goes both to tube N108 and the gate N33. The output of N108 goes directly to the decade ring. In the block diagram, FIGS. 33–A and C, the small number just outside the respective stages represents the digit corresponding to that stage. After clearing, the ring is setting at zero (for a detailed discussion of the operation of ring counter circuits, see 1.2.5).

Receiving numbers.—If five pulses arrive at the digit input they will pass through tube N106 (FIG. 36–A) of the pulse standardizer N30 (FIG. 33–C) and step the first ring N31 up to position five. Pulses will also go to the gate tube N33 but will have no effect since the second grid of that tube is negative, being connected to the now negative output of the ninth stage of the decade ring. Suppose that six more pulses arrive. Four of these will step the ring up to position nine. The fifth will step the ring from nine to zero and will pass through the gate N33 setting the decade flip-flop N32 and turning the inverter N109 off producing a positive pulse at gate N15. Since the incoming digits arrive before the carry gate (CCG) goes on (see FIG. 2) this fifth pulse does not pass gate N15. The sixth pulse steps the ring from zero to one. The carry clear gate comes on later in the addition time, opening gates N14 and N15. Since the flip-flop N32 has been set, the reset pulse RP (which arrives just after the carry clear gate comes on) is passed by gate tube N34 through the inverter N111 and through gate N14 to the digit input of the next decade to the left. This is called the delayed carry-over. The left decade having been standing with stage 0 in registering state, is thereby stepped to register at stage one. Thus, six plus five is now registered on these two decades as eleven.

Suppose that a decade registers nine, and a carry-over arrives from the next decade to the right. This carry-over pulse, besides stepping the left ring from nine to zero, also passes through gate N33 of the left decade, turning off the inverter N109. This transmits a positive pulse to gate N15 and since the carry gate is still on, there is a carry-over pulse formed by gate N15 which enters a third decade, next toward the left. This is called the direct carry-over. If all decades register nine, one may have a sequence of nineteen such carry-overs in the case of a twenty-digit accumulator so the carry gate has been made sufficiently long to provide for this possibility, and to attain the carry-overs of nineteen decades while the single CCG is effective.

Transmission of numbers.—The above description of a decade unit has been in terms of receiving numbers. Now consider an activated program with the program switch N2 set at AS, say. In this case the cycling pulses 10P are arriving at the digit input of each decade, there is no carry-over, since the carry gates N84, etc., are not open, and the nines pulses (9P) are arriving at the gates N35 and N36 in the decades. As indicated in the diagram, normally (after initially clearing) gate N36 is open. Suppose the decade registers the digit three. What happens during the twenty pulse times of an addition time is illustrated in the Table 4–4. Note, that the tens pulses arrive 2½ microseconds after the nines pulses; this gives the decade ring 7½ microseconds in which to step one stage and also 7½ microseconds for the flip-flop N32 to be set. If the operation switch is set at A instead of AS the only difference is that the 9 pulses do not appear at gate N36 and the 1'P is not provided. In case the switch is set at S the 1'P is provided at the significant figures switch 3*d* deck and the 9P appear only at gate N36. If the selective clear switch N79 is set to C then at pulse time 10 the carry-clear gate appears at gate tube N29 and the decades are cleared back to zero.

4.3.2. *General Description of a PM—Clear Plug-In Unit*

The PM-Clear unit contains a binary counter N41 to register the sign (P or M) of numbers. Since the binary counter is much simpler than the decade counter the pulse standardizer N44 therein may also be simpler. Thus, the tube A66 of FIG. 12 may be omitted and the output

taken from the plate lead of tube A60 to the binary ring N41. See Sections 1.2.11 and 1.2.12. Transmitters N43 and N40 transmit the sign indication over the add and subtract outputs respectively. Transmitter N46 forms a standard transmitter (see FIG. 14, Section 1.2.13) for the 1' pulse (used to give complements with respect to 10^n instead of 10^n-1, where n is the setting of the significant figures switch).

An odd number of pulses arriving at the PM binary counter will change its resulting position. An even number of pulses will leave it the same as it was to start with. If the number registered by the accumulator is positive and an activated program control has its operation switch set to AS, then nine pulses will pass gate N36'. If the registered number is minus, then nine pulses will be transmitted through gate N35' over the add output and none will go past gate N36'.

The transmission of sign indication is accomplished in a somewhat different manner. The S and A gates, N36' and N35' respectively, of the PM unit are controlled by stages P and M respectively of the PM counter. When a positive number is stored in an accumulator which is transmitting, a positive voltage from stage M holds gate N36' open so that the 9P are emitted over the PM lead of the subtract output terminal; no pulses are transmitted over the PM lead of the add output terminal since gate N35' is closed. If the sign of the stored number is M, gate N36' remains closed and N35' is opened so that no PM pulses are transmitted through the subtract output terminal, while 9 pulses are transmitted through the add output terminal.

TABLE 4-4.—A AND S TRANSMISSION

[Accumulator stores P 0 000 000 007—Significant figures switch is set at 10]

Pulse time	9P emitted over A leads PM 10 987 654 321	9P emitted over S leads PM 10 987 654 321	As result of receiving 10P acc. registers	Comment
0-17			7	Program input pulse is received.
18			7	
19			0 000 000 007	
1-0			P 1 111 111 118	
1		1 1 111 111 111	P 2 222 222 229	
2		1 1 111 111 111	P 3 333 333 330*	*Indicates that decade flip-flop is in abnormal state.
3	0 0 000 000 001	1 1 111 111 110	P 4 444 444 441*	
4	0 0 000 000 001	1 1 111 111 110	P 5 555 555 552*	
5	0 0 000 000 001	1 1 111 111 110	P 6 666 666 663*	
6	0 0 000 000 001	1 1 111 111 110	P 7 777 777 774*	
7	0 0 000 000 001	1 1 111 111 110	P 8 888 888 885*	
8	0 0 000 000 001	1 1 111 111 110	P 9 999 999 996*	
9	0 0 000 000 001	1 1 111 111 110	* *** *** *** P 0 000 000 007	
10		0 0 000 000 001		1'P is emitted over the lead for units decade because $s=10$.
11				
12				
13				Reset pulse resets all decade flip-flops.
14				
15				
16				
17	Program output pulse is transmitted if repeat control is used. Receiver (of non-repeat control) or transceiver (of non-repeat control) is reset.			

4.3.3 *Operation of the Numerical Circuits in Transmitting a Number and/or Its Complement*

When an accumulator is stimulated to transmit its contents and/or the complement of its contents, the 10P are routed simultaneously to each of the 10 decade ring counters of the accumulator. Each of the 10P cycles the counter one stage. Thus, if the stage corresponding to 7 is in the abnormal state before any of the 10P is received, after receiving one pulse, the stage corresponding to 8 is in the abnormal state, and stage 7 not. After receiving 10 pulses, the stage corresponding to 7 is in the abnormal state again (see Table 4-4).

Meanwhile the accumulator changes the 9P into digit pulses in the following way: Let d be the digit stored in a given decade counter before the reception of any of the 10P. Then as the 10P are received, $9-d$ of the 9P pass through gate N36 to be emitted over a lead of the subtract output terminal. That one of the 10P which cycles the decade counter from stage 9 to zero, also passes through gate N33 and sets the decade flip-flop. With the decade flip-flop in the abnormal state gate N36 is closed and N35 open so that the subsequent d pulses of the 9P group are passed over the corresponding decade place lead of the add output terminal. The first of the RP resets the decade flip-flop.

So far in this discussion mention has been made of transmitting through the subtract output terminal the complement of a number stored in an accumulator with respect to 9 999 999 999. Complements with respect to 10^{10} are provided by the accumulator's transmitting over the subtract output lead corresponding to decade s from the left (where s is the number of significant figures stored in the accumulator), the 1'P.

4.3.4 *Operation of the Numerical Circuits in Receiving a Number*

The digit pulse received through the 11 input gates (see Sec. 4.2.1) are routed simultaneously to the PM counter and the ten decade counters. Each pulse a decade counter receives cycles it one stage. The PM counter receivers zero sign pulses for a pulses for a positive number and 9 for a negative number. Each pulse received by the PM counter cycles it one stage so that the reception of an even number of pulses leaves the PM counter unchanged while the reception of an odd number of pulses has the effect of cycling the PM counter to the opposite stage.

If a given decade counter stores the digit d before reception and $p(9-d<p\leq 10)$ digit pulses are received, carry over takes place from that counter to the next one at the left (whether the PM or a decade counter). So called delayed carry over takes care of such carry-overs which result from incoming digit pulses. If a given counter, c, is in stage 9 and there is a carry over from the counter $c-1$, then, it is also necessary for carry over to take place from counter c to counter $c+1$. Carry overs which result from carry overs in this way are effected by a direct carry over process.

When a given counter is cycled to stage 9, a signal from this stage opens gate N33 so that the next pulse received by the decade (whether digit or carry pulse) not only cycles the counter back to stage zero but also passes through gate N33 and sets the decade flip-flop N32. In delayed carry over, the decade flip-flop continues to remember that a carry over must take place but no further action is taken while the digit pulses (the 9P and the 1'P) are being received. The signal from the normally negative output of the decade flip-flop opens gate N34 so that the reset pulse is passed (in pulse time 13 of the addition time cycle). This pulse resets the decade flip-flop and

also goes to gate N14. Now, in receive programs, the receive programming circuits allow the carry clear gate to reach and open gate N14, so that the pulse from gate N34 passes through to the next decade at the left.

The need for direct carry over arises after the first reset pulse is emitted by the cycling unit (since it is this reset pulse which gives rise to the need for direct carry over) so that carry over resulting from carry over must be treated differently. The carry pulse which passes through gate N33 goes to gate N15. Since the carry clear gate remains on for 7 pulse times, gate N15 is held open by the CCG from line N111 to pass this pulse to the next decade at the left. The carry clear gate, as a matter of fact remains on long enough for a carry pulse to proceed from units decade to the PM counter of 2 interconnected accumulators (with a safety factor). Notice, that even in direct carry over, the decade flip-flop is flipped into the abnormal state. The 2nd reset pulse which is emitted after the carry clear gate goes off, resets the flip-flop in the case (see FIG. 2).

A number may be received in an accumulator so that a digit appearing in the i decade of the transmitting unit is received in the i decade of the receiving unit by connecting the digit output terminal of the transmitting unit to some digit trunk by the standard cable for that purpose, and then connecting the same digit trunk to one of the 5 digit input terminals of the receiving accumulator by a standard cable. However, if it is desired to receive a number transmitted from decade i of the transmitting unit in decade $i+k$ of the receiving accumulator (where k may be either positive or negative), the number must be passed through a shifter en route from the transmitting to the receiving unit. It is usually most convenient to plug ordinary shifters into a digit input terminal of the receiving unit. A number may be shifted to the left either by an ordinary shifter plugged into a digit input terminal or by a special shifter plugged into a digit output terminal. A number may be shifted to the right only through an ordinary shifter plugged into a digit input terminal.

Table 4–5 illustrates the way in which an accumulator receives a number and also the delayed carry over process.

TABLE 4–5.—RECEPTION INVOLVING DELAYED CARRY OVER
[Accumulator stores M 9 832 104 707 and receives P 0 000 000 004]

Pulse Time	Accumulator Receives PM 10 987 654 321	Accumulator Stores After Receiving PM 10 987 654 321	Comment
0-17			Program input pulse received.
−18			
−19			
1-0	0 0 000 000 001	M 9 832 104 708	
1	0 0 000 000 001	M 9 832 104 709	
2	0 0 000 000 001	M 9 832 104 700*	*Decade flip-flop in abnormal state.
3	0 0 000 000 001	M 9 832 104 701*	
4			
5			
6			
7			
8			
9			
10			Carry-clear gate comes-in.
11			
12			
13	0 0 000 000 010	M 9 832 104 711	Reset pulse resets decade flip-flop and causes carry pulse.
14			
15			
16			
17			Program output pulse emitted if repeat control is used, and program control is reset.

4.3.5. *Static Communication Between an Accumulator and Another ENIAC Unit*

The high-speed multiplier receives its arguments and the printer data to be printed in static form from accumulators. The divider and square rooter also receives information about the signs of the arguments statically.

The term static is used to distinguish this kind of communication between an accumulator and another unit from the usual dynamic transmission in which an accumulator transmits d pulses for the digit d and the 0 or 9th pulses for sign P or M respectively.

A unit which receives the static outputs of an accumulator has an array of vacuum tubes corresponding to the flip-flops of the counters in an accumulator. For example, the ier selectors in the high-speed multiplier (see Sec. 5.3) which receive the multiplier from the multiplier accumulator statically consist of a 10 by 10 array of vacuum tubes. Each of the tubes in a column of the array corresponds to one of the flip-flops in a decade counter of an accumulator; each column in the array, to a decade counter in an accumulator. Two standard 55 conductor cables (carried in the static cable trough which runs along the tops of the ENIAC units) are used to deliver the static outputs of the accumulator which stores the multiplier to the ier selectors. The normally negative output of the flip-flop representing digit d in decade counter c is connected by one of the leads in these cables to the corresponding tube in the ier selectors. Thus, 100 of the 110 leads are used. An additional lead in one of the cables goes from the flip-flop for stage M in the accumulator's PM counter to a tube in the high-speed multiplier which represents sign M of the multiplier. In this way, when stage d of counter c is in the abnormal state (because that counter stores the number d) the tube in row d and column c of the ier selectors is turned on. The other tubes in column c of the ier selectors do not go on.

Similar connections are made to tubes in the printer from the counters of accumulators which store data for printing. In some cases data is printed from only 5 decades and the PM of an accumulator so that only 1 cable connects such an accumulator to corresponding tubes in the printer. The master programmer also has decade counters which are similar in some respects to the decade counters of an accumulator. These, too, can be connected statically to the printer.

In the case of the divider and square rooter only sign indication is communicated statically from the accumulators which store the numerator (or radicand) and denominator.

The length of time required for the information stored in an accumulator to be communicated in static form to another unit depends on the length of the leads from the accumulator to the unit. Approximately an addition

time is required to turn on the tubes in the high-speed multiplier and in the divider and square rooter because the accumulators statically connected to these units are near them. A somewhat longer time is required in the case of the printer.

4.4. *Use of Accumulators for Fewer Than or More Than Ten Digits*

4.4.1. *Use of an Accumulator To Store Two Numbers*

In some problems it may be desirable to put emphasis on the number of different numbers which can be stored in accumulators so that they will be readily available for computations rather than on the number of significant figures carried in the computation. While the accumulator has been designed to handle 10 digit numbers, it is possible to store in an accumulator two numbers with the same sign if their combined number of digits is 10 or fewer or with different signs if their combined number of digits is fewer than 10. In the first case the PM counter is used for the common sign. In the second case, one of the decade counters is used as a PM counter for the purpose of registering sign indication for one of the numbers with stage 0 representing sign P and stage 9, sign M.

When the numbers are transmitted to other units for computational purposes, they can be isolated from one another by the use of special deleters, adaptors, and/or shifters. It is to be noted, however, that if subtractive transmission takes place from an accumulator storing two numbers, only one of the numbers will be a correct tens complement since the other will lack the 1'P needed to make such as complement.

4.4.2. *Interconnection of Two Accumulators To Form a Twenty Decade Accumulator*

Another option available to the operator is whether an accumulator is to be used alone as a 10 decade accumulator with 12 program controls or as a 20 decade accumulator with controls for 24 programs. This option results from the fact that certain of the accumulator's circuits have been left open at the accumulator's interconnector terminals (indicated in FIGS. 33A through C by the symbol —□□—). The circuit so treated include the receive, transmit, clear, and pick up the 1'P circuits, and the input to units decade and the carry over input to the PM counter from decade 10. By special connections of the accumulator's interconnector terminals ST and SU, (I_{L_1}, I_{L_2}, I_{R_1}, and I_{R_2} in FIG. 32), these circuits are closed in one way (FIG. 32A) to make the accumulator function as a 10 decade accumulator and in a different way (FIG. 32B) to interconnect two accumulators so that they form a 20 decade accumulator.

If a single accumulator is used as a 10 decade accumulator, the following interconnections must be made:

(*a*) Vertical interconnector cable N102 must be plugged from interconnector terminal I_{L_1} to I_{L_2}.
(*b*) Load box N103 must be placed at interconnector terminal I_{R_1}.

If two accumulators are to be used as a 20 decade accumulator, the required interconnections are:

(*a*) Vertical interconnector cable N102 from I_{L_1} to I_{L_2}.
(*b*) Horizontal interconnector cables N104 from I_{R_1} to I'_{L_1} and from I_{R_2} to I'_{L_2}.
(*c*) Load box N103 at I'_{R_1}.

The significant figures switch of the left hand accumulator should be set to 10 and in the right hand accumulator to s' where $0 \leqslant s' \leqslant 10$ if $10+s'$ significant figures are desired. If fewer than 10 significant figures are desired, the left hand switch is set to this number and the right hand switch to 10.

For a given program only 1 program control is used. In reception, each accumulator receives its ten digits over one of its 5 digit input terminals. If the standard jumper cable for interconnecting accumulators is used, each accumulator receives its 10 digits through the digit input terminal on its front panel bearing the same designation (α–ϵ) as the setting of the operation switch used to program the reception. Each accumulator transmits its digit output through its own digit output terminals. In the transmission of complements the 1' pulse is emitted over the decade place lead of the last significant figure being retained. The 20 decade accumulator clears to zero in all decades except possibly one where clearing is to 5. Clearing is to zero in all decades if both s and s' are 10. In "receive-C" programs, the 1' pulse is put into the 20th decade from the left.

More than 2 accumulators should not be interconnected with one another as described above since the carry clear gate does not last long enough to provide safely for direct carry over across more than 20 decades; nor are the program control buffers designed to operate more than 2 accumulators.

4.5. *Illustrative Uses of Accumulators*

4.5.1. *Dummy Programs*

A dummy program is defined as one in which the operation and clear-correct switches are set at O and the repeat switch at r where $1 \leqslant r \leqslant 9$. Dummy programs are always set-up on repeat program controls. The dummy program has at least 3 important functions: (1) conversion of digit pulses into program pulses, (2) delay of a program pulse, and (3) isolation of programs from one another.

To terminate a computation at the desired point we make use of the fact that the complement of 9 in a decade place other than that of the extreme right hand significant figure is zero. Now, we stimulate repetition of the computing cycle each time by the program output pulse of a dummy program control whose program input pulse is derived from the digit pulse or pulses on the subtract output lead for decade 10 of accumulator 8. As long as the digit in the 10th decade is different from 9, this control receives and therefore, transmits a program output pulse which stimulates the iteration. When 9 appears in the 10th decade, this dummy program control receives and, therefore, emits no program output pulse so that the computation is terminated.

The question as to why the S digit output of the 10th decade is delivered to a program control which does nothing but transmit a program output pulse instead of being delivered to one of the controls used for computing may be raised at this point. The answer lies in the fact that the digit pulses do not begin to pour out of the S output terminal until pulse time 1 in the addition time cycle. This would mean that a computing program initiated by a digit pulse would start after at least one of the 10P and one of the 9P had been emitted by the cycling unit. Since these pulses play a vital role in computing programs, such programs must be initiated before the digit pulses are emitted. For this reason digit pulses may be used to initiate computing programs only under certain restricted conditions. Instead digit pulses should be converted into a true program pulse through the use of a dummy program and the computing program can than be initiated by the program pulse which results from the dummy program.

The above discussion regarding use (1) may be summarized as follows: To ensure that units receive all of the pulses needed for arithmetic operations, computational programs must usually be initiated by program pulses occurring at the time of the CPP. Where the stimulation of subsequent programs depends on digit pulses, the digit pulses should be converted into a program pulse by being brought to a dummy program control. The program output pulse from the dummy program control can then be used to stimulate computing programs.

The need for the second contribution (delay) of dummy programs becomes apparent in setting up a fairly compli-

cated problem in which a number of programs are carried out in parallel.

Suppose that at some point in a computation one program pulse is available to stimulate a multiplier program control and also to stimulate the transmission of the arguments for the multiplication program. Let us suppose further that the same multiplier program control is to be stimulated at some later time but that the arguments for the multiplication program, this time, are to be obtained in a different way. Obviously, the program pulse that stimulates transmission of the arguments must be isolated from the pulse that stimulates the multiplier program control for, otherwise, the units which transmit the arguments for the first multiplication cannot be suppressed from transmitting when the second multiplication program takes place.

The desired isolation can be provided for through the use of dummy programs in the manner suggested in FIGURE 37. The lines which carry program pulses have been labelled with program tray and line numbers for illustrative purposes.

4.5.2. *Magnitude Discrimination Programs*

As mentioned in the opening paragraphs of this chapter, the ENIAC is capable of discriminating between program sequences by examining the magnitude of some numerical result. In this section one possible method of carrying out such a magnitude discrimination program in an accumulator is discussed.

Let us assume that the critical quantity upon whose magnitude the choice of subsequent programs depends is x so that when $x<b$, program P_1 is to be stimulated and that when $x\geq b$, program P_2 is to be stimulated. The magnitude discrimination program is possible because 9 digit pulses are transmitted for sign indication M and none for sign indication P.

Let us form the quantity $x-b$ in some accumulator. Then, using a special adapter, connect the PM lead of the A output terminal of this accumulator to the program pulse input terminal of one dummy program control and the PM lead of the S output terminal to the program pulse input terminal of a second dummy program control as indicated on the schematic diagram of FIGURE 37-C.

Obviously when $x<b$, a positive number is emitted over the S terminal and a negative over the A terminal so that only dummy program control 1 is stimulated to emit a program pulse. Similarly, when $x>b$, the number emitted over the A terminal is positive and that over the S terminal, negative so that only dummy program control 2 is stimulated to emit a program pulse.

Even though both the number zero and its complement are represented in the ENIAC by P 0 000 000 000, the case $x=b$ (or $x-b=0$) can still be treated in the same way as $x>b$ (or $x-b=0$). For recall, when a positive number is transmitted from an accumulator, the A output gate of the PM counter remains closed and the S gate opens to allow the 9P to pass to the PM lead of the S output terminal. (Notice that when an accumulator which stores zero transmits subtractively to a second accumulator, this second accumulator receives, at first, M 9 999 999 999. Later, in the pulse time of the 1'P, the transmitting accumulator emits this pulse so that the receiving accumulator then stores P 0 000 000 000 after direct carry over proceeding from units decade to the PM counter has taken place.) These 9P received at the program pulse input terminal of dummy program control 2 cause the emission of a program output pulse to stimulate P_2.

In a problem in which accumulators are not urgently needed for storage or computational purposes, this set-up of a magnitude discrimination program is satisfactory. However, in general, this method has the disadvantage that no numerical programs other than one magnitude discrimination program can be carried out in an accumulator so set up, since both digit output terminals of the accumulator are completely associated with the magnitude discrimination program. The same magnitude discrimination can be effected without completely tying up either digit output terminal of an accumulator if the master programmer is used.

V. HIGH-SPEED MULTIPLIER

The high-speed multiplier finds the product of a signed multiplicand with as many as 10 digits by a signed multiplier of p digits ($p\leq 10$) in $p+4$ addition times. This high-speed is possible because products are obtained through the use of a multiplication table rather than by repeated addition, as was explained in Section 1.3.5 (Elementary Multiplication).

Not only does the high-speed multiplier find products, but it also has facilities for controlling certain programming features in accumulators associated with it: (1) It can instruct the argument accumulators to receive and clear or not clear at the end of the multiplication; (2) it can signal the final product accumulator to dispose of the product; (3) it delivers to associated accumulators programming signals used in the multiplication process.

The following topics will be discussed in this chapter: Sec. 5.1, program controls; Sec. 5.2, common programming circuits; Sec. 5.3, numerical circuits; Sec. 5.4, interrelation of high-speed multiplier and associated accumulators. Reference will be made to the following diagrams:

Front View	FIGS. 38.
Front Panels	FIGS. 39, 40 and 41.
Block Diagram	FIGS. 42-A, B, C and D.
Interconnection of High-Speed Multiplier with Associated Accumulators	FIGS. 43-A and B.

5.0. *General Summary*

It is assumed that the reader has familiarized himself with the operation of the elementary multiplier as described in Sec. 1.3.5.

The high-speed multiplier operates in conjunction with 4 or, possibly, 6 accumulators (see FIG. 43). Two accumulators, the ier (multiplier) and icand (multiplicand) accumulators, store the arguments. The accumulators used for this purpose have the static outputs of their counters connected to the multiplier. Also, the PM-clear unit is statically connected to the multiplier so that these accumulators can be cleared by a signal from the multiplier at the end of a multiplication program and so that the high-speed multiplier may take proper cognizance of the signs. If products having 8 or fewer significant figures are required, two accumulators are used for storing the products which the multiplier emits in pulse form through the digit output terminals on panel 3. These accumulators are referred to as the LHPP (left hand partial products) and RHPP (right hand partial products) accumulators. Where products of more than 8 significant figures are desired, a pair of interconnected accumulators may be used as the LHPP accumulator and another pair as the RHPP accumulator. The role of the LHPP and RHPP accumulators will be discussed in greater detail below. Either the LHPP or RHPP accumulator may be used as the final product (FP) accumulator.

The high-speed multiplier has 24 program controls (8 on each of its 3 panels, see FIGS. 38 through 41) on which can be set up 24 essentially different multiplication programs. In a problem in which there are more than 24 basic multiplications, each multipler control can be used on a number of different occasions with the aid of the master programmer or sequences of dummy programs.

Each program control consists of a transceiver P1 with program pulse input and output terminals (generally indicated at P2), multiplier (P3) and multiplicand (P4) accumulator receive switches, multiplier (P5) and multiplicand (P6) accumulator clear switches, a significant figures switch (P7), and a product disposal switch (P9). The argument accumulator receive switches (P3 and P4) enable the operator to specify the digit input

terminals through which the ier and icand accumulators shall receive their arguments for a given program. The significant figures switch (P7) setting determines into which decade place of the LHPP five round off pulses are transmitted for a given program. The setting of the places switch (P8) determines how many of the multiplier's digits are used for the program and, therefore, how long the multiplicaton takes (see below and Sec. 5.2). Instructions for the transmission of the product from the final product accumulator can be set up on the answer disposal switch (P9).

The 24 program controls operate the common programming circuit which include a 14 stage program ring (P11) with associated gates, inverters and buffers, the ier accumulator and icand accumulator receive circuits with program pulse output terminals $R\alpha$–$R\epsilon$ and $D\alpha$–$D\epsilon$ on front panel 1 (also shown in FIG. 42–B), argument accumulator clear circuits, the product disposal circuit with program pulse output terminals A, S, . . . , ASC on front panel 3 (FIG. 41), and the argument accumulator clear circuits.

The program ring P11 with its associated tubes clocks the progress of multiplication programs. Gates P12 and P13 which admit the 1'P and 4P are the round off gates. Gates P14 operate in conjunction with the places switch to terminate the program when the specified number of places of the ier have been used and, in conjunction with gate P16, to clear the ring to stage 13 at this time. The program ring P11, ultimately, also controls a circuit for correcting products if either or both of the arguments are negative (see discussion below), the *l* and *r* receiver circuits P17 which emit static signals to program the partial products accumulators to receive, the circuit P18 which emits the F pulse to stimulate the collection of the partial products in the final product accumulator, and the reset circuits (generally indicated at P19) for the program controls.

The outputs of stages 3 through 12, by means of the buffer tubes P21, control the high-speed multiplier's numerical circuits so that multiplication by each digit of the ier takes place successively.

The numerical circuits consists of the gates of the multiplier selector P22, the multiplication table P23, the coding gates P24 which pass the 1, 2, 2', and 4P, and the gates and the shifters of the multiplicand selector P26. The multiplication table stores the products of numbers between 1 and 9 by numbers between 0 and 9 by means of a resistance matrix as is explained below. The table actually consists of 2 tables, the tens and units tables, used for storing the tens and units digits of these products respectively. For example, the multiplication table remembers the product of 4×9 by storing 3 in the tens table and 6 in the units table, as was explained in connection with the elementary multiplier.

The ier selector tubes are set up by the static outputs of the ier accumulator counters. Each column in this array of tubes P22 is dedicated to 1 decade place of the ier; each row, to one of the digits between 0 and 9. When the program ring signals for multiplication by the ier digit in a particular decade place, the activated ier selector gate for that decade place emits a signal to the multiplication tables on one of the horizontal busses connecting the two.

Static signals for the products of all digits between 1 and 9 by the particular ier digit are emitted from the multiplication table and converted into pulse form at the coding gates P24. The products from the tens and units tables respectively then go to the left and right hand sets of gates of the multiplicand selector P26. These gates are set up by the static outputs of the icand accumulator so that only the products appropriate to the digits of the icand are allowed to pass.

These partial products then go to the left and right hand shifters P27. Each set of shifters consists of a 10 by 10 array of gates. The gates on each row are controlled by one stage of the program ring and the outputs of the gates are connected diagonally so that products are shifted successively one place to the right as multiplication by the ier digits progresses from left to right. The products are emitted from the 4 digit output terminals on panel 3 of the high-speed multiplier with those from the tens table being emitted by the terminals labelled "Left Hand Acc. I" and "Left Hand Acc. II" in FIG. 41 and those from the units table, by the terminals labelled "Right Hand Acc. I" and "Right Hand Acc. II." The terminals identified by II and I respectively take care of the digits for decade places 10^0–10^9 and 10^{10}–10^{19}.

Notice, that the high-speed multiplier transmits only the digits of the product but not the sign. For positive arguments, this results immediately in the correct signed product. If either or both of the arguments are negative, certain correction terms are needed to produce the correct signed products. From Table 5–1 in which the correction terms for the various cases are tabulated, it can be seen that whenever an argument is negative, the product obtained from the multiplication tables must be corrected by 10^{10} times the complement of the other argument. In the case where both arguments are negative, moreover, the sign of the product must be corrected. The programming circuits (see Sec. 5.2) provide for the last correction by causing the 1'P to be transmitted over the PM lead of the digit output terminal labelled "RH accumulator I." The programming circuits provide for the other corrections by causing the emission of program output pulses at the RS and/or DS output terminals P28 (FIG. 42–B). The operator must interconnect the multiplier with its associated accumulators so that these pulses stimulate the corrections to take place (see Sec. 5.4).

To summarize the discussion of the previous pages, multiplication of a 10 or fewer digit icand by a *p* digit ier required $p+4$ addition times. These addition times are used for the following purposes:

1. Reception of arguments.
2. Setting up of selector tubes and round off in LHPP accumulator.
3. } Obtaining the partial products (icand)×(1 digit of the ier) successively for the *p* digits of the ier.
. }
. }
o $p+2$. }
$p+3$. Correcting products in case either one or both of the arguments are negative.
$p+4$. Collecting the partial products so as to form the final product and clearing of the argument accumulators.

Tables 5–2 and 5–3 offer examples illustrating the operation of the high-speed multiplier. Although either the LHPP or RHPP accumulator can be used for forming the final product, we assume here, as in FIG. 43, that the RHPP accumulator is used for this purpose.

TABLE 5-1.—CORRECTION TERMS FOR NEGATIVE IER AND/OR ICAND

[R and D represent the absolute values of the ier and icand respectively]

	Case 1 Ier positive Icand negative	Case 2 Ier negative Icand positive	Case 3 Ier and Icand both negative
Ier	P+(R)	M+(10^{10}−R)	M+(10^{10}−R)
Icand	M+(10^{10}−D)	P+(D)	M+(10^{10}−D)
Product obtained from multiplication tables.	P+(10^{10}R−RD)	P+(10^{10}D−RD)	P+10^{20}+(RD−10^{10}R−10^{10}D) =M+(RD−10^{10}R−10^{10}D)
Correction term needed	M+10^{10}(10^{10}−R)	M+10^{10}(10^{10}−D)	M+P+10^{10}(R)+P+10^{10}(D)
Correct signed product	M+(10^{20}−RD)	M+(10^{20}−RD)	P+(RD)

5.1. *Program controls*

Each of the high-speed multiplier's 24 program controls consists of a transceiver with program pulse input and output terminals, argument accumulator receive switches and clear switches, a significant figures switch, a places switch, and a product disposal switch. Neons correlated with the transceivers are shown in FIG. 38.

accumulators are made and switches have been set up accordingly on the argument accumulators, the operator does not need to provide the argument accumulators with a separate program pulse to stimulate them to receive whenever a multiplication is to take place. The one program pulse which stimulates the performance of the multiplication also stimulates the reception of the arguments

TABLE 5-2.—MULTIPLICATION OF M 8 198 630 400 BY P 2 800 000 000

Description of program:
Multiply icand by 2 places of the ier
Round answer off to 8 places
Clear ier and icand accumulators after multiplication
Transmit product from final product accumulator

Add. Time	Ier accumulator stores PM 10 987 654 321	Icand accumulator stores PM 10 987 654 321	LHPP Accumulator (I)		RHPP and FP Accumulator (I)	
			Receives PM 10 987 654 321	Stores after receiving PM 10 987 654 321	Receives PM 10 987 654 321	Stores after receiving PM 10 987 654 321
1	P 2 800 000 000	M 8 198 630 400	M 8 198 630 400			
2			0 0 000 000 050	P 0 000 000 050		
3			1 011 100 000	P 11 011 100 050	0 628 626 080	P 0 628 626 080
4			0 607 642 030	P 1 618 742 080	0 048 248 402	P 0 676 874 482
5			M 7 200 000 000	M 8 818 742 080		
6	Program output pulse and product disposal signal are omitted				M 8 818 742 080	M 9 495 616 562
7	Product is transmitted from product accumulator					

TABLE 5-3.—MULTIPLICATION OF M 8 198 630 400 BY M 2 800 000 000

Description of Program:
Multiply icand by 3 places of ier
Do not round answer off
Clear ier and icand accumulators
Retain product in final product accumulator

Add. Time	Ier accumulator stores PM 10 987 654 321	Icand accumulator stores PM 10 987 654 321	LHPP Accumulator (I)		RHPP and FP Accumulator (I)	
			Receives PM 10 987 654 321	Stores after receiving PM 10 987 654 321	Receives PM 10 987 654 321	Stores after receiving PM 10 987 654 321
1	M 2 800 000 000	M 8 198 630 400				
2			1 011 100 000	P 1 011 100 000	0 628 626 080	P 0 628 626 080
3			0 607 642 030	P 1 618 742 030	0 048 248 402	P 0 676 874 482
4			0 000 000 000	P 1 618 742 030	0 000 000 000	P 0 676 874 482
5					1'P 0 000 000 000	M 0 676 874 482
6			1' 7 200 000 000	P 8 818 742 030	P 1 801 369 600	M 2 478 244 082
7	Program output pulse is transmitted				P 8 818 742 030	P 1 296 986 121

5.1.1. *The Multiplier and Multiplicand Accumulator Receive Switches*

Each of the argument accumulator receive switches **P3** and **P4** has the positions α, β, γ, δ, ϵ, and 0. Associated with the points α–ϵ on the switch for the ier accumulators are the program pulse output terminals R_α–R_ϵ (FIGS. 39 and 42–B) and, for the icand accumulator, D_α–D_ϵ. If one of these switches is set at a receive point, a program pulse received on a program input terminal is retransmitted through the corresponding terminal R_ϵ–R_ϵ or $D_{\alpha-\epsilon}$ when the program control of which the switch is a part is stimulated. The operator sets up program controls on argument accumulators so that a pulse transmitted in this way will cause reception to take place as specified.

The program pulse arriving at **P2** through terminal 1*i*, for example, turns the buffer **P41** on, giving a negative pulse through the switch, turning inverter **P43** (ϵ) off (with the switch setting at as illustrated). This causes the buffer **P42** (ϵ) to conduct and the transmitter **P44** (ϵ) gives a program pulse out of terminal R_ϵ located on the front of panel 2 (FIG. 39).

The argument accumulator receive switches **P3** and **P4** have been provided in order to simplify the programming of multiplications. Once the connections between some or all of the terminals R_α–R_ϵ, D_α–D_ϵ and the argument provided that they can both be received during the first addition time of the multiplication. If, for example, both the ier and icand are received directly from the constant transmitter, the argument accumulators cannot both receive their arguments in the same addition time because the constant transmitter transmits but one number in an addition time.

If an argument accumulator receive switch is set at O, no pulse to stimulate reception of the corresponding argument is transmitted. The setting O is used for multiplication programs in which the argument is held over from the previous program (see Sec. 5.1.2) or in programs in which it is desirable to stimulate the argument accumulator independently to receive its argument.

5.1.2. *Multiplier and Multiplicand Accumulator Clear Switches (P5 and P6)*

Clear circuits in the high-speed multiplier are connected to the PM-clear units of the ier and icand accumulators. If an argument accumulator clear switch is set at C, the high-speed multiplier's clear circuits emit a clear signal towards the end of addition time $p+4$ which causes the corresponding argument accumulator to clear. In programs for which a clear switch is set at 0, no clear signal is transmitted to the corresponding accumulator.

Depending upon the setting of these switches the following four possibilities arises:

	Ier Clear Switch	Icand Clear Switch	Result
(1)	0	0	Neither multiplier or multiplicand accumulators clear.
(2)	C	0	An activated program causes inverter P76 (3) to go off opening the gate P70 (4). This gate passes the CCG to the inverter P77 (2) which turns the associated buffer P78 (2) on, the output of which goes directly to the clear tubes 2 to 10 in the PM unit of the multiplier accumulator.
(3)	0	C	In this case P76 (1) goes off opening the gate P70 (1). The CCG turns off the inverter P77 (1) which in turn causes the buffer P78 (1) to conduct, the output of which goes directly to the clear tubes of the multiplicand accumulator.
(4)	C	C	Here the inverter P76 (2) goes off opening the gates P70 (2) and (3). As above, the clear gate is passed into the two sets of clear tubes in the respective PM units.

5.1.3. *The Significant Figures Switch (P7)*

The setting of the significant figures switch determines to which decade place of the LHPP accumulator **5** pulses for round off are transmitted. If this switch is at $2 \leqslant S \leqslant 9$, the five round off pulses are sent to decade $10-s$ of LHPP accumulator I. For $s=10$, the round off pulses are sent to decade 10 of LHPP accumulator II. (Unless 2 pairs of interconnected accumulators are used to receive the partial products, the round off pulses emitted for $s=10$ are lost.) No round off pulses are emitted in a program for which the significant figures switch is set at "off."

The significant figures switch provides greater flexibility in the round off options for the 24 programs than would be possible if the only round off control available were the significant figures switch on the final product accumulator. If, however, the round off requirements on all multiplication programs are the same, the significant figures switches of the multiplier program controls can be set at off and the significant figures switch on the final product accumulator can be set appropriately.

Notice that the setting of the significant figures switch of a multiplier program control does not cause the final product accumulator to emit the 1'P (needed for a complement with respect to 10^{10}) when the product is disposed of subtractively. Whether or not this pulse is put in, and the decade in which it is put, depend on the setting of the significant figures switch on the final product accumulator (see Sec. 4.1.4). If a product is disposed of subtractively in such a way that the 1'P is not transmitted by the final product accumulator, the 1'P can be put in at the receiving accumulator (see Sec. 4.1.2).

5.1.4. *Places Switches (P8)*

This switch determines how many digits of the multiplier are used in the multiplication. Since the time required for a multiplication is $n+3$ where n is the number of digits in the multiplier the time required for a problem can be materially shortened if fewer than ten digits of the multiplier can be used. With the place switch setting at 8 (as illustrated) the multiplier ring will step to stage 10 using eight digits of the multiplier. The inverters **P87** (8) and **P89** (10) being off, the gate **P14** (10) will turn the inverter **P88** off and in the next addition time a CPP will pass gate **P16** and through the inverters **P91** will clear the ring to stage 13.

If the places switch of a program control is set at p (where $2 \leqslant p \leqslant 10$), the high-speed multiplier multiplies the entire icand by the p left hand digits of the ier whenever this program control is used. Such a program lasts $p+4$ addition times and a program output pulse is emitted by the transceiver $p+4$ addition times after the reception of the program input pulse.

5.1.5. *Product Disposal Switch (P9)*

The points A, AS, . . . , ASC on the product disposal switch together with the program pulse output terminals A, S, . . . , ASC at the left of panel 3 of the high-speed multiplier make it possible for this unit to direct the transmission of the product from the final product accumulator.

Suppose that the product is finally collected in accumulators 13 and 14. The setting of the product switch determines what the pair of accumulators (operating as a twenty digit accumulator) do with the numbers. Suppose the disposal switch is setting on SC (as illustrated). The program which started the multiplication set the flip-flop (**P56** in transceiver **P1**) and so opened the gate **P30** in the transceiver. At the end of the multiplication the reset signal arrives on line **P78**, passes gate **P30** and turns off the inverter **P63**. This turns on the buffer **P72** giving a negative gate through the disposal switch turning off inverter **P71** (SC) opening gate **P61** (SC). At the beginning of the next addition time a CPP is passed through the transmitter **P79** (SC) to the terminal SC on front panel number three (FIG. 41). Generally, the operator will connect this output to the input of a program control circuit on accumulators 13 or 14, say, and the corresponding accumulator program switch will be set to S and the clear switch to C. If needed, the other outputs A, S, AS, AC, and ASC, can be connected to the inputs of program control circuits on accumulators 13 and 14 (or 11 and 12 if the product is collected here) and the corresponding switches set accordingly.

At the end of addition time $p+4$ when the high-speed multiplier program control emits a program output pulse, a pulse is also emitted from the terminal A, S, . . . , or ASC corresponding to the point at which the product disposal switch is set. The product disposal program pulse output terminals which are used should be connected to program pulse input terminals on the final product accumulator (see FIG. 43). If a product disposal switch of a given program control is set at 0, the high-speed multiplier does not emit a product disposal pulse when this program control is used.

The program switches on the final product accumulator may, but need not necessarily, be set so as to correspond to the labeling of the product disposal terminal from which the stimulating pulse comes. For example, if in a given program it is convenient to dispose of some product subtractively twice, and then clear and, moreover, no multiplication program requires ASC disposal, then the ASC output terminal can be connected to a repeat program control on the final product accumulator set up for subtractive transmission repeated 2 times with clearing. Notice that with such a set-up the point ASC on the product disposal switch no longer has the meaning transmit A and S simultaneously and clear but, rather, the meaning established by the set up of the program control on the final product accumulator.

In a course like the previously described one care must be exercised to prevent conflicting programs. Since during the first two addition times of a multiplication program, the RHPP accumulator has a completely non-active role, product disposal lasting 2 addition times is possible (with the RHPP accumulator used as the FP accumulator) even though a new multiplication program is initiated when the product disposal signal is emitted. If the product is disposed of repetitively r times (where $r>2$), the next multiplication program must be initiated no sooner than $r-2$ addition times following the product disposal signal. It might also be mentioned at this point that repetitive reception of an argument cannot be accomplished through the use of the terminals R_a–R_e or D_a–D_e since the arguments must be received no later than the end of addition time 1 of a program in order to allow sufficient time for the selectors to set up.

5.2. *Common Programming Circuits*

5.2.1. *Argument Accumulator Receive Circuits*

A program input pulse delivered to a program control is routed immediately through buffers (P39 and P41 on program control 1, for example) to the argument receive switches for that control. Each receive point on these switches connects to one of 5 output circuits consisting of buffer **P42**, inverter **P43**, standard transmitter **P44**, and program pulse output terminal **P46** (R_a–R_e or D_a–D_e on front panel 1). The program output pulse transmitted in this way is taken to a program control on the argument accumulator to stimulate reception of the argument (see Sec. 5.4).

step the ring until it arrives at stage one. When it reaches stage one P83 closes shutting off the CPP.

This method of initial clearing by stepping the ring to stage one is used here since, as described below, the regular clearing circuits operate in conjunction with the places switch to clear the ring to stage 13 in the process of terminating the multiplication.

The program ring is in stage 1 when a program input pulse is received by some program control at the end of, let us say, addition time zero. During addition time 1, the argument accumulators receive their arguments (see Sec. 5.2.1) and, at the end of addition time 1, the ring cycles to stage 2.

TABLE 5-4.—CHRONOLOGICAL OPERATION OF HIGH SPEED MULTIPLIER'S PROGRAMMING CIRCUITS

[*Note.*—It is assumed here that ten-decade accumulators are used for the partial products]

Add. Time for 2 digit multiplier	Stage of Ring Counter	Event	
		In High Speed Multiplier's programming circuits	In associated accumulators
End of Add. time: 0	1	(1) Program input pulse is received and re-transmitted to ier and/or ieand accumulators.	(1) See addition time 1.*
1	1	(1) Ring cycles to stage 2 at CPP time.	*Ier and ieand accumulators receive arguments.
2	2	(1) 1P passed by P31 sets l and r receivers. (2) 1′P gated through P12 and 4P through P13 are delivered to round-off gates. (3) Ring cycles to stage 3.	(1) LHPP and RHPP accumulators' "receive on" circuits are activated. (2) LHPP accumulator receives five roundoff pulses.
3	3	(1) Signal from stage 3 opens ier selector 10th place gates so that multiplier tables are entered with first from the left ier digit. (2) Signal from stage 3 opens shifter gates P40. (3) Ring cycles to stage 4.	(1 and 2) LHPP accumulator receives tens digits of "ieand×first ier digit" in decade places 10 through 1. RHPP accumulator receives units digits of "ieand×first ier digit" in decade places 9 through 1.
4	4	(1) Signal from stage 4 opens ier selector gates and shifter gates. (2) Signal from P14 (4) gates a 1′P through P32. (3) Signal from P14 (4) gates CPP through P33 to initiate RS and DS corrections if R and/or D are negative. (4) Signal from P14 (4) gates CPP through P34 to provide reset signal for l and r receivers. (5) Signal from P14 (4) allows CPP to pass through P16 to clear ring to stage 13.	(1) LHPP accumulator receives tens digits of second P.P. in decade places 9 through 1. RHPP accumulator receives units digits of second P.P. in decade places 8 through 1. (2) PM counter of RHPP accumulator receives 1′P if both ier and ieand are negative. (3) See addition time 5.** (4) LHPP and RHPP accumulators' "receive on" circuits cease to be activated.
5	13	(1) Signal from stage 13 allows CPP to pass through P36 and P35 to the reset flip-flops for program controls 1–8 and 17–24. (2) Signal from stage 13 gates a CPP through P38 so that F pulse is emitted. (3) Ring cycles to stage 14.	**RS and/or DS corrections are made (see addition time 4). (2) See addition time 6.***
6	14	(1) Signal from stage 14 goes to reset gates of program controls 9–16 to reset these controls. All other program controls are reset by signals from reset flip-flops. (2) Ieand and ier accumulator clear signals are emitted. (3) Program output pulse and product disposal signal are emitted. (4) Ring cycles to stage 1.	***LHPP and RHPP are combined. (2) Argument accumulators clear.
7	1		Product is transmitted from final product accumulator.

5.2.2. *Program Ring and Associated Circuits*

When a high-speed multiplier program control is stimulated, the signal derived ultimately from the normally negative output of the flip-flop holds gate **P47** open so that a CPP is admitted to cycle the program ring **P11** one stage per addition time. The effect of signals from various stages of the ring on the round off, partial product receiver, complement correction, final product collection (F pulse), and program control reset circuits are discussed in this section. Mention is also made of the effect of signals from the ring on the numerical circuits which are discussed in greater detail in Sec. 5.3. Table 5–4 summarized the chronological operation of the programming circuits for the case of a 2 place multiplier.

Whenever a program control circuit is activated the inverter **P81** goes off opening the gate P47. This gate then passes central program pulses through the pulse standardizer **P82** to step the ring. Whenever the ring is not at stage one the gate P83 is open. This passes central program pulses to the inverter P84 and thence to the gate **P86**. If the initial clear gate is on, the CPP pass P86 and

The timing is important here:

Pulse time	17 18 19 0	2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
	CPP steps ring to second stage	1 P sets receivers to cause partial prods. to be received	4 P start	1′ P arrives

Thus, in one addition time the ring steps to the second stage, the product accumulators are set to receive, and the five pulses for the roundoff are put into the proper decade. The CPP that steps the ring could not be used to operate the receivers because of the time it takes for P31 to open.

A signal from stage 2 opens gate P31. The 1P passed through this gate sets the l and r receivers early in addition time 2. These receivers are not reset until the end of addition time $p+2$ (see discussion below). As long as these receivers are set, a static signal is delivered to the

l and *r* terminals on front panel 3. These signals, brought to interconnector terminals on the left and right hand partial products accumulators (see Sec. 5.4.1.2), stimulate the reception, through the α input terminal, of the round off pulses (see discussion immediately following), the partial products emitted during the succeeding *p* addition times, and the 1'P to correct the sign of the product when both the ier and icand are negative. Since the *l* and *r* signals are brought directly into the "receive on α" programming circuits of the product accumulators, no program controls need be set up to program the reception of the partial products.

The signal from stage 2 of the ring also opens gates **P12** and **P13** so that the 1'P and 4P are passed. These five pulses, used for round off of the product, are delivered to the gates P48. Each of these gates is connected to a point on the significant figures switches as indicated in FIG. 42–B. The normally positive output of the activated program control's flip-flop through inverter **P49**, buffer **P51**, and point *s* on the significant figures switch, opens one of these gates so that the round off pulses are emitted over the lead for decade place 10—*s* of the left hand partial products digit output terminal I or over the lead for decade place 10 of the left hand partial products digit output terminal II.

The output from stage 2 also goes to gate **P31** which gates a 1 pulse. This 1 pulse turns the inverter **P21** off and thence sets the two receivers. The outputs of these two receivers come to front of panel three. (See FIG. 41.) From there these gate signals will be taken by special interconnecting jumpers to interconnector terminals ST_1**1** on accumulators **11** and **12** and accumulators **13** and **14**. Inspection of the accumulator block diagram (FIG. 33) shows that this will cause the product accumulators to receive the partial products over the input digit terminals α. This is an example of a receiver located in one unit operating the governing circuits of another unit.

In addition time 3, a signal from stage 3 through **P52** and inverter **P53** is applied to the ier selector gates for the 10th decade place and through inverter **P54**, to the shifter gates **P40** (Left-hand and Right-hand). In this way, multiplication by the first digit of the ier takes place with the products being emitted on the leads for decades 10–1 of the digit output terminal LHPP accumulator I and on the leads for decades 9–1 of the digit output terminal RHPP accumulator I, and for decade 10 of RHPP accumulator II. Similarly, in addition times 4, 5, . . . , $p+2$, the ring causes multiplication by successive digits of the ier and the emission of the products shifted over one place to the right each time.

When the ring steps to stage three and **P52** goes on and inverter **P53** off the gates are opened for the tenth digit of the multiplier (gates 0–9 in tenth place). Depending upon the value of the tenth digit of the multiplier one of the lines through the multiplication tables will carry a negative gate (which will turn off certain pulse gates in multiplication table **P23**). At the same time inverter **P54** will go off causing the bottom row of gates in the two shifters **P49** to open. Thus, the tens partial product will feed into accumulator **11** and the units partial product into decades 1 to 9 of accumulator 13 and decade 10 of accumulator 14. Notice that the units product is already shifted one place to the right. Thus, when the right and left hand products are collected at the end of the multiplication no extra shifting will have to be done.

As the ring steps from 3 toward stage 12 the gates for successive digits of the multiplier are opened and the gates on corresponding levels in the shifters are opened.

If the place switch is setting on 8 (as shown) the inverter **P87** (10) is off opening associated gates **P14** (10). When the ring reaches stage 10 the inverter **P89** (10) goes off causing the gate **P14** (10) to go on and the inverter **P88** to go off. This opens the gate **P16** and at the end (pulse time 17) of the addition time under consideration a CPP turns the inverters **P91** off clearing the ring to stage 13 (this clear signal overrides the stepping signal which would normally step the ring to stage 11). The output of **P88** also gates a CPP at the end of the addition time at **P34** which turns the inverter **P92** off causing the receiver flip-flops to reset. This causes the product accumulators to stop receiving the partial products. The output of **P88** also opens the gates **P33** and **P32**. The CPP gated by **P33** ultimately gives a program pulse out DS if the multiplier is negative and out RS if the multiplicand is negative. If both multiplier and multiplicand are negative **P32** gates a 1' pulse which finally goes into the PM channel to accumulator 13.

When the ring steps to stage **13** the inverter **P93** goes off and gates **P35**, **P36** and **P38** are opened. At the 14th addition time **P36** gates a CPP which sets a flip-flop causing programs 1 to 8 to reset. At the same time **P35** likewise causes programs 17 to 24 to be reset. **P38** gates a CPP during the 14th addition time which will generally be used to collect the right and left hand products. This pulse is transmitted to terminal F on the front panel. From there it will be jumped by the operator to a program tray and then used to program transmission of the left hand partial product, say, and the reception of this left hand product by accumulators 13 and **14**.

Stage 14 of the ring causes programs 9 to 16 to be reset. The ring is located on panel two of the multiplier, so the gates **P30** in transceivers 9 to 16 can be operated directly by the output of the ring. Since transceivers 1 to 8 are on panel one a special flip-flop **P66** set by a CPP during the 13th addition time (passed by gate **P36** which is opened by stage 13 of the ring) provides the reset signal. Similarly, another flip-flop **P67** resets programs 17 to 24.

From stage 14 the ring steps back to stage **1** and stops. At this time the transceiver gives an output program pulse.

The places gates number **P14** emit a signal on the coincidence of a signal from the normally negative output of the flip-flop **P56** and buffer **P37** (right) passing through point *p* on the places switch and a signal from stage $p+2$ of the ring. The signal emitted by one of these gates terminates the multiplications by successive ier digits, causes complement correction to take place, and resets the *l* and *r* receivers.

The phase of the multiplication program in which the tables are used is terminated as follows: A CPP passed through gate **P16** at the end of addition time $p+2$ clears the ring to stage 13. At the same time, a CPP passed through gate **P34** resets the *l* and *r* receivers.

During addition time $p+2$, the signal from one of the places gates allows a 1'P to pass through gate **P32** and a CPP, through gate **P33**. A static output signal from stage M of the ier accumulator's PM counter holds gate **P58** open so that this gate passes the output of gate **P33** to the DS output terminal on panel 3. Similarly, if the icand is negative, the output of gate **P33** passes through gate **P59** to the RS terminal. The gates **P32**, **P61** and **P62** are so arranged in series that the 1'P is allowed to reach the PM lead of terminal RHPP accumulator I only if both the ier and icand are negative. This latter pulse is received in the right hand partial product accumulator because the *r* receiver is not reset until the end of addition time $p+2$ after this pulse has been emitted. With the associated accumulators set up as shown in FIG. 43, the pulses transmitted from terminals RS and DS stimulate the carrying out of the complement corrections (shown on Table 5–3) during addition time $p+3$.

At the end of addition time $p+3$, a CPP passes through gate **P38** which is held open by a signal from stage 13 of the ring. This pulse, transmitted through terminal F (on panel 3) is used to stimulate the collection of the partial products into the final product (see FIG. 43 and Sec. 5.4).

At the end of addition time $p+4$, the activated program control is reset and a program output pulse is transmitted. This resetting is accomplished in one way for program controls (9–16) on panel 2 and in a slightly dif-

ferent way for program controls 1–8 and 17–24 on the first and third panels (see FIGS. 39, 40 and 41).

The signal from stage 14, early in addition time $p+4$ is brought directly to gate P30 of transceivers on the second panel. This gate, controlled by the normally negative output of the flip-flop, then emits a signal which passes through inverter P63 and opens gate P64. The CPP passed through gate P64 at the end of addition time $p+4$ resets the flip-flop and is transmitted as a program output pulse.

Gate P30 of a transceiver on the first or third panel also gets a reset signal early in addition time $p+4$. This signal, however, is derived from one of the reset flip-flops (P66 on panel 1 or P67 on panel 3). A signal from stage 13 opens gates P36 and P35 to allow a CPP to pass and, thus, set the reset flip-flops on panels 1 and 3 respectively. The normally negative output of these flip-flops is then brought to gate P30 in the associated transceivers. Neons correlated with the reset flip-flops are shown in FIG. 38.

5.2.3. *Argument Accumulator Clear Circuits*

The reset signal, whether from stage 14 or from the reset flip-flops (see discussion immediately above), causes gate P30 of the stimulated transceiver to emit a signal early in addition time $p+4$. This signal, through inverter P63 and buffer P68, passes through the ier and/or icand accumulator clear switches to one or two of the argument accumulator clear gates P70. The argument accumulator clear gates are so connected to points on the clear switches that gate P70 (4) is opened if only the ier accumulator is to be cleared, gates P70 (2) and P70 (3) if both argument accumulators are to be cleared, and gate P70 (1) if only the icand accumulator is to be cleared. Towards the end of addition time $p+4$, the carry clear gate (CCG) passes through the opened clear gate (or gates) to the PM-clear unit of the accumulator (or accumulators) to cause the clearing of the argument accumulators as specified by the settings of the argument accumulator clear switches.

5.2.4. *Product Disposal Circuits*

There are 6 product disposal circuits A, S, . . . , ASC each consisting of a program pulse output terminal on panel 3, a transmitter, a gate P64, a buffer P71. Each of these circuits is connected to the corresponding point A, AS, . . . , ASC on the product disposal switch.

The signal emitted by gate P30 of the stimulated program control when the reset signal arrives, passes through inverter P63, buffer P72 and the product disposal switch to the buffer of the appropriate product disposal circuit. Thus, the gate in such a circuit is held open to pass a CPP at the end of addition time $p+4$. This pulse, emitted from one of terminals A, S, . . . , ASC at the end of addition time $p+4$, is used by the operator to stimulate disposal of the product (see Secs. 5.1.5 and 5.4) which takes place during addition time $p+5$.

5.3. *Numerical Circuits*

The numerical circuits of the high-speed multiplier consist of the ier selector P22, the tens and units multiplication tables P23, the coding gates P24, the left and right hand icand selector gates P26, the left and right hand shifters P27, and the four digit output terminals P73, P74, P76, and P77 (LH partial products accumulators I and II and RH product accumulators I and II, respectively, on panel 3).

The ier selectors P22 consists of a 10 by 10 array of gates. The ier selector gate in row i (i=0 to 9 from bottom to top) and column j (j=10 to 1 from left to right) receives, as one input, the static output of stage i in decade counter j of the ier accumulator and, as its second input, a signal from stage $13-j$ of the multiplier ring. The output signal from a gate in row i activates row i of the multiplication tables.

In the tens table of P23 there are eight groups of vertical conductors corresponding to icand digits 2 to 9 and in the units table, 9 groups of vertical conductors corresponding to icand digits 1 to 9. The basic products are remembered by means of a pattern of connections between the horizontal conductors (from the ier selectors) and the vertical conductors (to the coding gates P24). Each of the vertical conductors is labelled so as to indicate the pulses (1, 2, 2′, or 4) which are brought to the coding gate to which it is connected. No conductor is needed for icand equal to one in the tens table since the tens digit of any one digit ier by icand equal to one is zero.

Now, a signal from a gate in row i of the selectors is delivered through the connections between row i of the tables and the vertical conductors to the coding gates. Since the output of the ier selector gate is negative the signals from the multiplication tables have an inhibitory effect on the coding gates to which they are delivered. Notice that for ier equal to zero, all coding gates are turned off. The 1, 2, 2′, or 4P are allowed to pass through only the coding gates which receive no signal from the multiplication tables.

Suppose, for example, that the digit in the tenth decade place of the ier is 2. Then during addition time 3, the tube numbered 2 in the 10th place of P22 emits a signal. The ensuing action is exactly as described in Sec. 1.3.5.

SELECTION OF PRODUCTS BY ICAND SELECTORS WHEN ICAND M 8 198 630 400 IS MULTIPLIED BY FIRST DIGIT OF IER P 2 800 000 000

Decade Place	Left Hand Icand Selector Gate	Pulses Passed	Right Hand Icand Selector Gate	Pulses Passed
10	8	1	8	6
9		0	1	2
8	9	1	9	8
7	8	1	8	6
6	6	1	6	2
5	3	0	3	6
4		0		0
3	4	0	4	8
2		0		0
1		0		0

For example, when the icand N 8 198 630 400 is multiplied by the first digit of the ier P 2 800 000 000 (see the illustrative problem of Table 5–2), the product pulses passed by icand selector gates are shown in Table 5–5. Table 5–6 shows the timing of a multiplication operation.

TABLE 5-6.—OPERATION OF MULTIPLIER

Addition and pulse time	Description
0.17	Program pulse arrives at transceiver. This pulse passes buffers (P39 and P41) and depending upon the setting of the multiplier and multiplicand receive switches may be transmitted again. Gates P47, P14 (12) and P48 (10) (assuming the places switch is at 10 and that the significant figure switch is at 10) are opened.
1.17	A CPP passes P47 to step the program ring to stage 2. Gates P12 and P13 are opened, as is gate P31.
2.1	One pulse passes gate P31 to set the l and r receivers.
2.6 to 2.10	Four pulses and a one primed pulse pass gates P12 and P13 to give five pulses out channel 10 of SV3.
2.17	The program ring steps to stage 3. The output of stage three causes the multiplication of the multiplicand by the first digit of the multiplier to take place.
3.17	The program ring steps to stage 4 and multiplication by the second digit takes place.
4.17	The program ring steps to stage five, and so forth.
11.17	The program ring steps to stage 12, opening gate P16, P34, P33 and P32. Multiplication by the tenth digit of the multiplier takes place.
12.10	1′P passes P32 and (if both multiplier and multiplicand are negative) will be transmitted into the PM unit of accumulator 12.
12.17	A CPP passes P16 cleaning the ring to stage 13 opening gates P36, P35, and P38. A CPP passes P34 to reset the l and r receivers. A CPP passes gate P33 and may pass P58 and/or P59 to cause the complement corrections.
13.17	The program ring steps to stage 14. CPP pass gates P36 and P35 to set the flip-flops P66 and P67. A CPP passes gate P38 to be transmitted to program the product collection (this pulse appears at terminal F).
14.10	The CCG may pass one or two of the gates P70 (1), (2), (3) or (4) to cause the multiplicand and/or the multiplier accumulator to clear.

Notice that the pulses for the partial products are emitted from inverter tubes instead of standard transmitters. For this reason, the digit output terminals on panel 3 must be connected to input terminals on the partial products accumulators by means of digit trays or cables to which no other units are connected in parallel. No load boxes are used on these digit trays (see Sec. 5.4).

5.4. *Interrelation of the High-Speed Multiplier and Its Associated Accumulators*

5.4.1. *Interconnections for Numerical and Programming Data*

The 10 decade counters of the ier accumulator (9) are connected statically to the ier selector gates through cable **P73'**. Similarly, the decade counters of the icand accumulator (10) are connected to both sets of icand selector gates by cable **P74'**; the *n*th place of the icand going to the *n*th place of both the left-hand and the right-hand selectors. Stage M of the ier accumulator is statically connected to gates **P58** and **P61** and stage M of the icand accumulator, to gates **P59** and **P62** of the complement correction circuit (see Sec. 5.2.2). Fifty leads in each of 4 55-conductor cables are used for the static outputs of the 20 decade counters involved. An additional lead in each of 2 of the cables carries minus sign data. These cables are brought from accumulators 9 and 10 to the selector gates in the high speed multiplier by way of the static cable trough which runs along the top of the ENIAC panels.

Only accumulators **9** and **10** which are next to the high-speed multiplier can be used as the ier and icand accumulators since only one addition time, the 2nd, is allowed (with a safety factor included) for the set-up of the arguments in the selectors. If longer static leads were used to deliver the arguments to the selectors, more time than has been provided would be needed to set up the arguments. As a matter of fact not even the ier and icand accumulators can be interchanged since the time constants have been measured on the basis that the further accumulator (9) is connected to the ier selectors on panel 1 and the nearer accumulator (10), to the icand selectors on panel 2 of the high-speed multiplier.

The outputs of gates **P70** in the clear circuits (see Sec. 5.2.3) are also connected to the PM clear units of the argument accumulators.

All the other connections between the multiplier and its associated accumulators are numerical and programming purposes are made through digit or program trays or cables. These are shown in FIG. 43, which indicates the external connections between the panels.

5.4.1.1. *Programming Connections for "Receive Argument" Instructions*

The terminals R_a–R_ϵ are connected to program pulse input terminals on the ier accumulator as indicated at **P98**. The program switches associated with these terminals are set up appropriately. Similarly terminals D_a–D_ϵ are connected to program pulse input terminals on the icand accumulator as indicated at **P99**. Although FIG. 43 shows all of the R_a–R_ϵ and D_a–D_ϵ terminals connected, it is, of course, necessary to make connections only for the terminals which are used.

5.4.1.2. *Connections for Partial Product Reception*

The signals emitted through the *l* and *r* terminals on panel 3 of the high-speed multiplier during addition times 2 through $p+2$ are delivered to the "receive on α" programming circuits of the partial products accumulators by means of cables **P46** and **P97** running from the *l* and *r* terminals to interconnector terminals on the LHPP and RHPP accumulators respectively. The digit output terminals on panel 3 of the high-speed multiplier are connected to the α input terminals of the partial products accumulators as indicated at **P101** and **P102**. If products with 8 or fewer significant figures are required, the dotted digit connections may be omitted.

To repeat the statement made in Sec. 5.2.2, no other units can be connected in parallel to the trays used to carry the partial products and no load box should be used on these trays.

5.4.1.3. *Connections for Complement Correction*

The S output terminals of the ier and icand accumulators are connected to the input terminals of LHPP Accumulator I and RHPP Accumulator by lines **P103** and **P104** respectively for the purpose of delivering to these accumulators the correction terms required if either or both of the arguments are negative (see Table 5–1). With these digit connections, the following program connections must be made:

(1) From terminal RS on panel 3 to a control on the ier accumulator set up for subtractive transmission and to a control on the LHPP accumulator set up for reception on β (line **P106**).

(2) From terminal DS on panel 3 to a control on the icand accumulator set up for subtractive transmission and to a control on the RHPP accumulator set up for reception on β (line **P107**).

A second method of making the complement correction connections is possible. The S output terminals of the ier and icand accumulators may be connected to the β input terminals of RHPP accumulator I and LHPP accumulator I respectively. In this case the program connections are as follows:

(1) From terminal RS to the ier accumulator and to the RHPP accumulator.

(2) From terminal DS to the icand accumulator and to the LHPP accumulator.

5.4.1.4. *Connections for Final Product Collection*

FIG. 43 shows the partial product accumulators set-up so that the RHPP accumulator also serves as the final product accumulator. The A output terminal of the LHPP accumulator is connected to the β input terminal of the RHPP accumulator by line **P104** and the F terminal on panel 3 is connected to a control on the RHPP set up for reception on β and on the RHPP for additive transmission, by line **P108**. Since the RHPP accumulator is free for two addition times at the beginning of multiplication programs and the LHPP accumulator is free for only one addition time (see Sec. 5.1.5), there is a slight advantage in using the RHPP accumulator as the final product accumulator if repetitive disposal of the product is contemplated. Otherwise, by suitable digit tray and programming connections, the LHPP accumulator can just as well be made to serve as the final product accumulator. Notice that it is not necessary to use a shifter at the β input terminal of the FP accumulator in collecting the partial products in one accumulator because the high-speeed multiplier's shifters align the partial products so that they can be combined properly.

5.4.1.5. *Programming Connections for Product Disposal Instructions*

FIG. 43 shows several of the A, S, . . . , ASC terminals on panel 3 connected to program controls on the final product accumulator which are set-up for transmission. As mentioned earlier in Sec. 5.1.5, the meanings taken on the points A, S, . . . , ASC on the product disposal switch depend entirely on the set up of the program controls on the final product accumulator to which the terminals A, S, . . . , ASC are connected.

5.4.2. *Position of Decimal Point in Product Accumulator*

The position of the decimal point of the product can easily be deduced from the description of the way in which the shifters route the partial products (see Sec. 5.3). If *r*, *d*, and *f* respectively represent the number of decade places that the decimal points of the ier, icand, and final product are removed from the PM place in their respective accumulators (*r*, *d*, and *f* are positive

or negative according as they are counted toward the right or left of the PM counter), then

$$f=r+d$$

This formula is illustrated in the table below:

ier	r	icand	d	product	f
P 1. 000 000 000	1	P 1. 000 000 000	1	P 0 1.00 000 000	2
P 0 03.0 000 000	3	P.4 000 000 000	0	P 0 01.2 000 000	3
P 0 03.0 000 000	3	10^{-2}(P.4 000 000 000)	−2	P 0. 012 000 000	1

VI. DIVIDER AND SQUARE-ROOTER

The divider and square-rooter performs the operations of dividing and square-rooting ten and twenty digit numbers. To carry out these operations with ten and twenty digit numbers it makes use of four and seven accumulators, respectively. Thus, the divider and square-rooter unit itself is essentially a programming circuit which controls the operation of the associated accumulators.

The process of division is that of repeated subtraction. Thus, the numerator is in one accumulator and the denominator in another. The denominator is subtracted until an overdraft occurs. At this time the numerator is shifted (by transmitting to a shift accumulator and transmitting back with a shifter in the digit line). Note that the overdraft was not corrected as in some methods of division used on computing machines. Instead, signs are changed and the denominator is alternately subtracted and added between the shifts. The quotient is built up by the divider sending +1 or −1 into the proper decade of the quotient accumulator for each subtraction.

The process of square rooting is likewise accomplished by repeated subtractions (the quantity subtracted being increased by two each time in the proper decade). The number to be square rooted is placed in the numerator accumulator and the numbers to be subtracted are built up in the denominator accumulator. When an overdraft occurs the number in the numerator accumulator is shifted (similar to the shift in dividing) and certain corrections are made to the number in the denominator accumulator and the subtraction process is repeated. As the process continues twice the square root is built up in the denominator accumulator.

The time required to complete the above operations depends on the number of places required in the answer and the digits in each place of the answer. If it is assumed that the average digit of the answer is 5 and if p designates the number of places in the answer, approximately $13p$ addition times are consumed in division or square rooting.

The first section of this chapter contains a general summary of the divider and square rooter. Sections 6.1, 6.2, and 6.3 respectively cover the program controls, common programming circuits, and numerical circuits of this unit. Information pertinent to the interrelation of accumulators associated with the divider and square rooter appears in Section 6.4. Examples of division and square rooting are given in Section 6.5. The following diagrams will be referred to in this chapter:

Front View of the Divider and Square Rooter__ FIG. 44
Divider and Square Rooter Front Panel_____ FIG. 45
Divider and Square Rooter Block Diagram____ FIG. 46
Interconnection of Divider and Square Rooter with its Associated Accumulators_____ FIG. 47

6.0. *General Summary*

It is assumed that the reader is familiar with FIGS. 18 and 19 and with their associated descriptions.

The divider and square rooter carries out a division or square rooting by operating as a central programming agent for a group of associated accumulators (see Section 6.4). In division the associated accumulators are the numerator (dividend) accumulator, the denominator (divisor) accumulator, shift accumulator, and quotient accumulator; in square rooting the associated accumulators are the numerator (radicand) accumulator, the shift accumulator, and the denominator (twice the root) accumulator. The divider controls these accumulators in the sense that at various periods of the operation cycle, it transmits to these accumulators program signals appropriate to the period of the computation and the quantities involved in the computation and in the sense that it provides the answer accumulator with the numerical data from which the answer is ultimately formed.

The operation cycle, whether for division or square rooting, divides itself rather clearly into 4 periods: period I in which the stage is set for the following periods, period II during which the operation itself proceeds, period III, the round off period, and period IV, the interlock and clear period. When a divider and square rooter program control is stimulated, the events which occur in the four periods mentioned above, depend, to some extent, on the way in which the program control is set up.

In addition to a transceiver with program pulse input and output terminals, each of the 8 program controls contains an interlock pulse input terminal and 8 program switches (see FIG. 45).

These switches and their purposes are as follows:

(*a*) *Numerator receive switch.*—During the first addition time of the division this switch may be used to cause the numerator accumulator to receive either α or β.

(*b*) *Denominator receive switch.*—During the first addition time of the division this switch may be used to cause denominator accumulator to receive on α or β.

(*c*) *Numerator clear switch.*—At the end of the division or root process this switch may be used to cause the numerator accumulator to clear.

(*d*) *Denominator clear switch.*—At the end of the process this may be used to cause the denominator accumulator to clear.

(*e*) *Interlock switch.*—This switch decides whether or not the interlock feature is used. Suppose this switch is setting on N1. At the end of the division or root process the various flip-flops and rings in the divider square-rooter are cleared and an output program pulse is transmitted. If this switch is on 1 then this clearing process and output pulse does not occur until both a signal is received on one of the interlock inputs (upper left corner of FIG. 46), and the division or root process is completed.

(*f*) *Answer disposal switch.*—This switch is connected to four receivers and thus gives four possible ways of disposing of the answer (that is, four ways it could be transmitted).

(*g*) *Round-off switch.*—This switch decides whether the answer to the division or the square rooting process be rounded off.

(*h*) *Division-square root and place switch.*—This switch determines whether the process is division or square rooting and how many places are used. There is a choice of 4, 7, 8, 9, or 10 places.

The remaining program control circuits include:

(1) *The common programming circuits.*—In the divider-square rooter (as in other units) the common programming circuits comprise all of the circuits except the program controls (described above) and the numerical circuits (described just below).

(2) *Numerical circuits.*—The numerical circuits of the divider-square rooter comprise the place ring and its associated gates (lower right hand corner of FIG. 46), the pulse gates (just above and to the right of the place ring), and the "1," "—1," "2," and "—2" receivers which open these gates.

During period I of a division, the divider and square rooter emits signals which stimulate the argument accumulators to receive the arguments in accordance with option 1 above and sets up certain of its common programming circuits (see Section 6.2) in accordance with option 3.

Period II, for division, includes combinations of a basic division sequence and a shift sequence. When the numerator and denominator have like signs, the denominator is subtracted from the numerator and the quotient is increased by one unit in a particular decade place; when the signs of the arguments are unlike, the denominator is added to the numerator and the quotient is decreased by one unit in a particular decade place. When the remainder from the numerator after an addition or subtraction of the denominator shows an overdraft (i.e., a change in sign from the one which the remainder carried before the addition or subtraction), the basic division sequence is interrupted. Then the remainder is transmitted from the numerator accumulator to the shift accumulator where it is received shifted over one place to the left. Next the numerator accumulator again receives the numerator from the shift accumulator. The basic division sequence is repeated with the quotient respectively increased or decreased by one unit after every time a subtraction or addition of the denominator takes place. After a shift sequence, however, the unit is added to or subtracted from a decade place of the quotient one further to the right than before the shift sequence.

Square roots in the ENIAC are obtained by a method which makes use of the fact that

$$\sum_{i=1}^{a}(2i-1)=a^2$$

and which is analogous to a method often used to find square roots on electric or manual desk computing machines.

Period I for square-rooting not only covers the reception of the numerator (or radicand) and the set-up of certain circuits in the divider and square rooter, but also provides for the reception of one pulse in the 10^8 decade of the denominator (twice the root) accumulator.

In the basic square-rooting sequence of period II, odd numbers successively increasing (and accumulated in the denominator accumulator) are subtracted from the radicand until an overdraft occurs. Then odd numbers successively decreasing are added to the radicand. The ENIAC finds by this procedure twice the square root (formed in the denominator accumulator) since the answer is increased or decreased by two units after each addition or subtraction takes place. Period II, in square rooting as in division, includes a shift sequence which takes place whenever the remainder of the radicand indicates a change of sign. The square root shift sequence provides for transmission of the radicand to the shift accumulator to shift it one place to the left and the return of the shifted radicand to the numerator or radicand accumulator. The shift sequence, furthermore, provides for the subtraction or addition respectively of one unit first in the decade place in which twice the root was previously increased or decreased by two units in the basic square root sequence and then in a decade place one further to the right. After a shift sequence the basic square root sequence is repeated until overdraft occurs.

Period II is terminated and period III initiated when an overdraft occurs and when the divider and square rooter has found the number of places (counting toward the right from the PM decade) of the answer specified by the setting of the divider-square root and places switch of the answer. In division, period III includes the shifting of the numerator one place to the left as in the shift sequence of period II. Then, if round-off is specified by the setting of the program control, the denominator is subtracted from or added to the numerator (if the numerator's remainder and the denominator have like or unlike signs respectively) five times.

TABLE 6-1.—DIVISION—ILLUSTRATIVE PROBLEM

[Problem: Divide P 0 2090070 000 by P 0 230 000 000. Round answer off to 4 places. No interlock]

Period	Add. Time	Quotient Accumulator		Numerator Accumulator		Denominator Accumulator	Shift Accumulator	
		Receives	Stores after Receiving	Receives	Stores after Receiving	Receives during period 1 and stores thereafter	Receives	Stores after Receiving
I	1			P 0 209 070 000	P 0 209 070 000	P 0 230 000 000		
	2							
	3							
II	4			M 9 770 000 000	M 9 979 070 000			
	5	P 0 100 000 000	P 0 100 000 000					
	6						M 9 790 700 000	M 9 790 700 000
Shift	7			M 9 790 700 000	M 9 790 700 000			
	8			P 0 230 000 000	P 0 020 700 000			
	9	M 9 900 000 000	P 0 090 000 000					
	10						P 0 207 000 000	P 0 207 000 000
Shift	11			P 0 207 000 000	P 0 207 000 000			
	12			M 9 770 000 000	M 9 977 000 000			
	13	P 0 001 000 000	P 0 091 000 000					
III	14						M 9 770 000 000	M 9 770 000 000
	15			M 9 770 000 000	M 9 770 000 000			
	16			P 0 230 000 000	P 0 000 000 000			
	17			P 0 230 000 000	P 0 230 000 000			
	18			P 0 230 000 000	P 0 460 000 000			
	19			P 0 230 000 000	P 0 690 000 000			
	20			P 0 230 000 000	P 0 920 000 000			
	21							
	22	P 0 000 000 000	P 0 091 000 000					
IV	23							
	24		Program output pulse and answer disposal signal is transmitted					
	25		Answer is transmitted from quotient accumulator					

TABLE 6-2.—SQUARE ROOT—ILLUSTRATIVE PROBLEM

[Problem: Find $\sqrt{P\ 0\ 081\ 360\ 400}$. Round answer off to 4 places. No interlock]

Period	Add. Time	Numerator (Radicand) Accumulator		Denominator (Two Root) Accumulator		Shift Accumulator	
		Receives	Stores after receiving	Receives	Stores after receiving	Receives	Stores after receiving
I	1	P 0 081 360 400	P 0 081 360 400				
	2						
	3						
	4			P 0 100 000 000	P 0 100 000 000		
II	5	M 9 900 000 000	M 9 981 360 400				
	6			P 0 200 000 000	P 0 300 000 000		
	7			M 9 900 000 000	P 0 200 000 000	M 9 813 604 000	M 9 813 604 000
Shift	8	M 9 813 604 000	M 9 813 604 000	M 9 900 000 000	P 0 100 000 000		
	9	P 0 100 000 000	P 0 003 604 000				
	10			M 9 980 000 000	P 0 170 000 000		
Shift	11			P 0 010 000 000	P 0 180 000 000	P 0 036 040 000	P 0 036 040 000
	12	P 0 036 040 000	P 0 036 040 000	P 0 001 000 000	P 0 181 000 000		
	13	M 9 819 000 000	M 9 855 040 000				
	14			P 0 002 000 000	P 0 183 000 000		
III	15			M 9 999 000 000	P 0 182 000 000	M 8 550 400 000	M 8 550 400 000
	16	M 8 550 400 000	M 8 550 400 000				
	17	P 0 182 000 000	M 8 732 400 000				
	18	P 0 182 000 000	M 8 914 400 000				
	19	P 0 182 000 000	M 9 096 400 000				
	20	P 0 182 000 000	M 9 278 400 000				
	21	P 0 182 000 000	M 9 460 400 000				
	22						
	23			M 9 998 000 000	P 0 180 000 000		
IV	24						
	25	Programs output pulse and answer disposal signal is transmitted					
	26	Answer is transmitted from denominator accumulator					

If overdraft does not result from these subtractions or additions, the quotient is respectively increased or decreased by one unit in the last place from the left required by the setting of the places switch. Period III of square rooting is similar to that for division except for two details. In square rooting this period covers the shifting of the radicand's remainder and the addition or subtraction of one unit in the decade place of twice the root which, in the previous basic square root sequence, was decreased or increased by two units. Also, in square-rooting as in division, if round-off is specified, the contents of the denominator accumulator are then subtracted from or added to the contents of the numerator accumulator. If no overdraft results, twice the root is increased or decreased by two units.

Period IV is identical in both division and square rooting. In this period, ring counters (see below) in the divider and square rooter are cleared and certain flip-flops are reset so as to ready the divider and square rooter for the next program. A program output pulse is transmitted either to indicate the completion of the operation or the reception of an interlock input pulse as well at the completion of the operation. The divider-square rooter signals for the disposal of the answer in accordance with the setting of the answer disposal switch at the end of period IV and the numerator and denominator accumulators clear or do not clear in accordance with the settings of the numerator and denominator accumulator clear switches. Tables 6–1 and 6–2 show numerical examples.

The events described above are motivated by the divider and square rooter's common programming circuits. The answer which is accumulated in the quotient accumulator in division or in the denominator accumulator in square rooting is supplied by the numerical circuits of the divider and square rooter.

The common programming circuits of the divider-square rooter which are operated by the program controls may be divided roughly into 3 circuits which are concerned solely with programming within the divider-square rooter (internal programming circuits); circuits which program the associated accumulators as well as other circuits within the divider (internal-external programming circuits); and circuits concerned solely with programming the accumulators associated with the divider and square rooter (external programming circuits).

The internal programming circuits (see FIG. 46) include the program ring circuit, the overdraft circuit, the sign indication circuit, the divide flip-flop, and the interlock and clear circuit, all indicated by appropriate legends in FIG. 46.

Program Ring Circuit (FIG. 46–A)

The program ring circuit contains a flip-flop called the pulse source flip-flop which controls the emission of certain specialized pulses used only in the divider and square rooter. Which pulses are emitted depends on whether division or square rooting is the operation and also on the period of the computation. The 9 stage program ring directs the progress of the computation by providing gates for particular signals suitable to the phase of the computation at various times. The cycling of the program ring is controlled by the program ring flip-flop and by certain of the special pulses whose emission in turn, is controlled by the pulse source flip-flop.

Overdraft Circuit (FIG. 46–B)

The overdraft circuit has for its purpose the sensing of overdrafts. It consists of a binary ring counter (called the numerator ring) for registering the sign of the numerator. This ring is cycled only during period I and just after the numerator is shifted to the shift accumulator in periods II and III. In addition to the numerator ring, the overdraft circuit has four gates each of which is connected to a stage of the numerator ring and statically to the PM counter of the numerator accumulator. As long as the remainder from the numerator remains the same as it was before an addition or subtraction of the denominator, this circuits emits an NO (no overdraft) signal. When the numerator's remainder changes sign an O (overdraft) signal is emitted.

Sign Indication Circuit (FIG. 46–C)

The sign indication circuit compares the signs of the numerator and denominator emitting a like sign signal when numerator and denominator have the same sign and an unlike sign signal when the signs of the numerator and denominator differ. The denominator flip-flop in this circuit is set only if the denominator is negative. The denominator flip-flop feeds to each of four gates which have for their second input static leads from the PM counter of the numerator accumulator.

Divide-Root Flip-Flop (FIG. 46–C)

The divide flip-flop is used to remember whether the operation being performed is division or square rooting. This flip-flop affects programming only during the round off period at which time its intervention results in the emission of the instructions which distinguish period III for division from period III for square rooting.

Interlock and Clear Circuit (FIG. 46–A)

The interlock and clear circuit which consists of the interlock flip-flop, the interlock coincidence flip-flop, the clear flip-flop and the various gates operated by these flip-flops, during period IV, emits signals which clear the divider and square rooter's rings and reset certain of its flip-flops.

The circuits which are both internal and external programming circuits are those containing the receivers which, when set, motivate the accumulators associated with the divider and square rooter to perform certain suboperations involved in division and square rooting and which also stimulate other programming circuits within the divider and square rooter to function (see Section 6.2). The receivers included in this category are those controlling the N_γ, D_A, D_S, Q_α, D_γ, D'_γ, S_α and N_{AC} and S_{AC} and N'_γ circuits. Signals from these receivers are delivered to the associated accumulators by means of special cables leading from the quotient accumulator and shift accumulator program terminal, the denominator and square root accumulator program terminal, and the numerator accumulator interconnector terminal (see FIG. 45) to interconnector terminals on accumulators corresponding to the names of the terminals on the divider and square rooter.

The N_γ circuit (FIG. 46–B) stimulates the reception, via the numerator accumulator's γ input channel, of the denominator or the complement of the denominator when either of these quantities is transmitted from the denominator accumulator as a result of the setting of the D_A or D_S receivers during the basic division or square rooting sequence of period II or in round off during period III.

The Q_α circuit (FIG. 46–B) controls the reception, via the quotient accumulator's α channel, of the units which are used to form the quotient and which are transmitted by the divider and square rooter whenever the basic division sequence of period II takes place or at the end of period III in round off programs if no overdraft results from the addition or subtraction of five times the denominator from the numerator.

The D_γ circuit (FIG. 46–B) controls the reception by the denominator accumulator via its γ channel of the +2 or −2 units transmitted by the divider and square rooter every time the basic square rooting sequence of period II occurs or in period III if no overdraft occurs after the addition or subtraction of 5 times twice the square root in period III of round off programs. Another receiver, the D'_γ receiver also controls reception via the denominator accumulator's γ channel of numerical data which ultimately forms twice the square root. This receiver, however, is used to program the reception of the single unit (+ or −) transmitted first in a given decade place and then in a decade place one further to the right during the square rooting shift sequence of period II and to program the reception of a single unit just once at the beginning of period III for square rooting.

The $S\alpha$, N_{AC}, S_{AC}, and $N'\gamma$ circuits (FIG. 46–E) control events which occur during the shift sequence of period II and at the beginning of period III for either division or square rooting. The first two circuits stimulate the transmission (with clearing) of the contents of the numerator accumulator to the shift accumulator which receives this data through its α channel. A shifter which shifts numerical data one place to the left is placed at the α input terminal to accomplish the shifting of the numerator, as was explained in connection with FIGS. 18 and 19. The numerator is then cleared out of the shift accumulator and returned to the numerator accumulator via the numerator accumulator's γ input channel as a result of the setting of the S_{AC} and N'_γ circuits.

The circuits which are used solely for external programming are the numerator and denominator accumulator clear circuits and the N_α, N_β, D_α, D_β, receivers and answer disposal receivers 1, 2, 3, and 4. Signals from the external programming circuits are delivered to the associated accumulators in exactly the same way as are the signals from the circuits which are both internal and external programming circuits.

The N_α and N_β circuits (FIG. 46–A) correspond respectively to the points α and β on the numerator accumulator receives switches and are used to stimulate the reception of the numerator (or radicand) by the numerator accumulator at the beginning of a program. The D_α and D_β receivers have a similar function. Whether these receivers actually stimulate reception through the α or β input channels or through some other channels depends, of course, on the manner in which the interconnector plugs of the cables leading from the divider and square rooter to the numerator and denominator accumulators are wired. The plugs stimulate reception in accordance with the labelling on the numerator accumulator and denominator accumulator receive switches.

The instructions given to the quotient or denominator accumulator as a result of the setting of one of the four answer disposal receivers depend on the wiring of the interconnector plugs used to deliver the divider and square rooter's programming instructions to the answer accumulators.

The answer is built up in the quotient accumulator (in division) or in the denominator accumulator (in square rooting) out of numerical data produced by the numerical circuits of the divider and square rooter. These circuits, which are discussed in greater detail below, include the +1, −1, +2, −2 receivers, gates controlled by the above mentioned receivers which pass the 1, 2, 2', 4, 9, or 1' pulses, the 10 stage place ring, and 10 pairs of digit output gates with each pair controlled by a stage of the place ring.

The answer is formed one unit (in division) or two units (in square rooting) at a time in a particular decade place from the digit pulses passed through the 1, 2, 2', 4, 9, and 1' pulse gates and routed into appropriate decade places by the 10 pairs of gates controlled by the places ring. Sign indication M belonging to any component of the answer is derived from the 9P delivered to the PM lead of the answer output terminal on the divider and square rooter front panel.

6.1. *Program Controls*

There are eight standard transceivers to receive the incoming program pulses. As in the case of the multiplier the incoming program pulse is immediately retransmitted to cause the numerator and denominator accumulators to receive their numbers without the loss of time. This retransmission takes place through buffers located on a separate plug-in unit (there are two such plug-in units altogether). Two such buffers, R2, are illustrated in the lower left corner of FIG. 46.

The divider and square rooter has 8 program controls each consisting of a transceiver with program pulse input and output terminals on the divider and square rooter front panel (see FIG. 45), an interlock pulse input terminal R1, a numerator accumulator and a denominator accumulator receive switch, a numerator accumulator and denominator accumulator clear switch, a divide-square root and places switch, a round off switch, an answer dis-

posal switch, and an interlock switch, all as shown in FIG. 45.

6.1.1. *The Numerator Accumulator and Denominator Accumulator Receive Switches*

The buffers R2, described above, feed two switches (for each control circuit) located on the front panel, namely, the numerator and denominator receive switches, R3 and R4 respectively. Each of these switches has three settings, α, β and 0. The four outputs of these two switches go through inverters R6 (FIG. 46–A) to four receivers R7 (located on two plug-in units). The outputs of these receivers come to output sockets SV1, SV2, $SU_3$1, and $SU_3$2 located on the front panel. The outputs may be connected directly to the common programming circuits of the respective accumulators by use of a special inter-connector cable.

The numerator accumulator and denominator accumulator receive switches of the divider and square rooter have the same purpose as the multiplier accumulator and multiplicand accumulator receive switches of the high-speed multiplier. These two sets of switches on the divider-square rooter enable the operator to control the stimulation of the reception of the arguments entering into a divider and square rooter program centrally at the divider and square rooter instead of locally at the associated accumulators. The instructions specified by the setting of the receive switches on the divider and square rooter, however, are transmitted statically to the numerator and denominator accumulators via cables leading from the denominator-square root receiver output terminal and the numerator receiver output terminal on the divider and square rooter's front panel to interconnector terminals respectively on the numerator accumulator and denominator accumulator. It is to be noted that in the case of the high-speed multiplier, the instructions set-up on the receive switches are transmitted in pulse form from pulse output terminals on front panel 1 of the high-speed multiplier to program pulse input terminals on the ier and icand accumulators. In the case of the high-speed multiplier it is necessary to set-up ier and icand accumulator program controls corresponding to the R_e–R_ϵ and D_e–D_ϵ terminals on the high-speed multiplier. In the case of the divider and square rooter it is not necessary to set up program controls on the numerator and denominator accumulators since the receive instructions are delivered directly into the common programming circuits of these accumulators.

The numerator accumulator and denominator accumulator receive switches differ also from the high-speed multiplier's receive switches in that the former offer the operator only two options as to the accumulator input channel through which reception is to take place. The cables used to connect the numerator receiver output terminal and the denominator and square root receiver output terminal to the numerator and denominator accumulator interconnector terminals have been so wired that if either or both of the numerator or denominator accumulator's receive switches be set to α or β, the corresponding accumulator receives its argument through the α or β input channel respectively.

If it is not desired to stimulate the reception of an argument on any given program or if it is desired to control the reception of either or both arguments for a given program locally at the appropriate accumulator (by delivering a program input pulse to a suitably set up program control on the accumulator either before or simultaneously with the program input pulse that stimulates the divider and square rooter program control), then one or both receive switches can be set to O (off).

When the receive switch of a given program control is set to a setting different from O, the divider and square rooter emits the receive instructions at the same time as the program control's transceiver is set by the program input pulse so that the accumulator correlated with the receive switch receives its argument during the 20 pulse times immediately following the reception of a program input pulse by the divider and square rooter.

6.1.2. *The Numerator Accumulator and Denominator Accumulator Clear Switches*

The output of buffer R8 (in the transceiver, FIG. 46–D) goes to the numerator and denominator clear switches R9 and R11. This buffer goes on only at the end of the division or rooting process (and possibly after an interlock signal) when clearing is taking place. The output of the switches R9 and R11 (three outputs: numerator, denominator, or both) goes to inverters R12 and thence to gates R13, FIG. 46–A. These gates pass the carry clear gate (CCG) through the inverters R14 and buffers R16. This signal goes directly to the clear tubes in the PM-Clear units of the corresponding accumulators. The following table illustrates what happens with the various settings of these switches:

TABLE 6-3

Num. Clear Switch	Denom. Clear Switch	Effect (as tube R8 in transceiver goes on)
O	O	None.
C	O	R12 (3) goes off and associate gate R13 passes a CCG through the inverter R14 (N) and buffer R16 (N) to the clear tubes in the numerator accumulator.
O	C	R12 (1) goes off and associated gate R13 passes a CCG through R14 (D) and R16 (D) to the clear tubes of the denominator accumulator.
C	C	R12 (2) goes off and the associated two gates R13 pass CCG's through both inverters R14 and buffers R16.

If a clear switch is set to C, the clear circuits in the divider and square rooter emit a clear signal during the last addition time of a program just before the transmission of a program output pulse. This signal is delivered by means of static leads (see FIG. 47) from the divider and square rooter to the PM-Clear Unit of the accumulator corresponding to the receive switch set at C in the addition time at the end of which the divider and square rooter emits a program output pulse.

Since the denominator accumulator is used as the answer accumulator in square rooting programs and since answer disposal takes place in the addition time following the transmission of a program output pulse, it is obvious that the answer would be lost before it could be transmitted to another unit if the denominator accumulator clear switch were set at C for square rooting programs. The answer disposal switch together with a suitable adaptor plugged into the denominator square root accumulator program terminal provide a correct method for clearing the denominator accumulator without loss of the answer in square rooting programs.

6.1.3. *The Divide-Square Root and Places Switch*

The divide-square root and places switch R19 provides a means of choosing which of the divider and square rooter's operations is to be performed on a given program and of specifying the number of places in the answer (counting from the front of the unit) to be found. The five left hand positions of this switch (FIG. 46–D) specify division to 4, 7, 8, 9, or 10 places and the five right hand positions, square rooting to 4, 7, 8, 9, or 10 places. The number of places chosen by the operator for a given program will depend on the accuracy requirements of the computation and on the alignment of the arguments in the argument accumulators.

Of the two decks of this switch one (the one on the right in FIG. 46–D) determines whether the process is to

be division or square rooting. This deck takes the output of buffer R17 in the transceiver to the round-off switch R18. The other deck R19 determines how many places the answer is to contain. This switch handles two jobs. This means that the number of places used in a division or a square rooting is restricted to 4, 7, 8, 9, or 10. See Section 6.4 for a discussion of the relationship between the location of the decimal point in the argument and answer accumulators.

The setting of the divide-square root and places switch like the setting of the significant figures switch of the high-speed multiplier, has no effect on the putting in of the 1'P pulse when the answer is disposed of subtractively from the answer accumulator. Which decade the 1'P is put into in subtractive disposal depends on the setting of the significant figures switch on the answer accumulator. If programs with different round off requirements are performed, it may be necessary to supply the 1'P at the accumulators which receive complements from the answer accumulator.

6.1.4. *The Round-Off Switch*

The round-off switch R18 is a double-pole, double-throw switch which determines whether the answer is to be rounded off or not. One pole of the switch operates in case of division and the other in case of square rooting and works in conjunction with one deck of the root-divide and place switch. The four terminals connect to four inverters (the four triodes R21) which in turn connect to the gates R22. These gates provide the division pulse (DP), the square root pulse (SRP), and the round-off pulse (ROP).

The round off switch R18 offers the operator a choice between obtaining an answer rounded off (RO) or not rounded off (NRO) to the number of places specified by the setting of the divide-square root and places switch. In general, division or square rooting programs in which 10 or fewer answer places are required will either be performed with round off or else round off will be taken care of in an accumulator after the divider has found more answer places than are required. To obtain answers with 11–19 places (see Sections 6.2 and 6.4), two programs are necessary. The first one, in which the first 10 left hand digits are found, should be performed without round off. The result of the second program should be rounded off whether as part of the second divider program or in an accumulator after the divider program.

It should be noted that under certain circumstances, twice the square root obtained through a round off program may be in error by 2 units in the last place found. For example, the divider and square rooter produces the answer P0002 when $2\sqrt{0}$ is found to four places in a round off program. The reason for this slight inaccuracy becomes apparent when it is remembered that round off of square roots as carried out by the divider is only approximate. Let R represent the remainder from the radicand and let $p+2x$ be the number stored in the denominator accumulator at the end of addition time III—2 where $2x$ is the extreme right hand digit of the answer found (so that, at this time p is the answer less $2x$). Assume that k answer places have been found and, for simplicity, let us say that the decimal point in the numerator and denominator accumulator occurs k places from the left. If k is odd (so that R, the remainder from the radicand before round off, is greater than or equal to zero) the decision to change or not change the answer by 2 units in the last place depends on whether $R-5p-10x$ does not or does show an overdraft. If round off were carried out exactly, the quantity

$$R-5p-10x-2.5$$

would be examined instead. Thus, the rounded off answer is inaccurate when $R-5p-10x\geqslant 0$ and when $R-5p-10x-2.5<0$. It can easily be seen, then, that the rounded off answer obtained in square rooting programs is correct except when

$$0\leqslant(5p+10x)-|R|<2.5$$ for an even number of places

or

$$0\leqslant|R|-(5p+10x)<2.5$$ for an odd number of places

6.1.5. *The Answer Disposal Switch*

This switch has five positions, four of these go respectively to four receivers and the fifth is an "off" position. At the end of the division or square rooting process (and after the interlock signal has arrived if the interlock switch is at "I" the buffer R23 (in the transceiver) goes on. This may (depending upon the setting of the switch) cause one of the inverters R24 to go off opening one of the gates C or D 46 or 47. The CPP passed by one of these gates will turn the corresponding inverter R26 off activating the corresponding receiver. The outputs of this receiver go directly (provided the operator connects them) to the common programming circuits of the quotient accumulator or to the denominator accumulator depending on the interconnector cable used. The timing of the operation of these circuits is explained in Sections 6.4.1. and 6.4.2.

The answer disposal switch on the divider and square rooter is comparable to the product disposal switch on the high-speed multiplier in that the former enables the operator to provide for the stimulation of the disposal of the answer from the answer accumulator without the necessity of delivering a program input pulse to the answer accumulator specifically for this purpose. The answer disposal switch on the divider and square rooter, however, offers the operator only 4 optional methods of disposal in contrast with the 6 options of the product disposal switch on the high-speed multiplier.

The answer disposal signals emitted by the divider and square rooter, moreover, are static signals which are delivered to the quotient and/or denominator accumulator by means of cables connecting the quotient accumulator and shift accumulator program terminal and/or the denominator-square root program terminal to interconnector terminals on the quotient and/or denominator accumulator. Points 1 and 2 of the answer disposal switch refer to the disposal of the quotient and points 3 and 4 to the disposal twice the root. The exact meaning conveyed by their settings, however, depends on the wiring of the adaptors and interconnector cables used to carry instructions from the program terminals on the divider and square rooter to interconnector terminals on the associated accumulators (see Section 6.4.2) since the instruction signals are brought directly into the accumulators' common programming circuits. In the high-speed multiplier, on the other hand, the instructions specified by the settings A, S, AS, AC, SC or ASC of the product disposal switch, depend on the setup of the product accumulator program controls which receive product disposal pulses from the A, S, AS, AC, SC, or ASC pulse output terminals on panel 3 of the high-speed multiplier.

6.1.6. *The Interlock Switch*

The setting of this switch (R27 in FIG. 46–D) determines whether the interlock feature is used or not. If this switch is setting at "NI" the buffer R28 (in the transceiver) causes the inverter R29 (NI) to go off and the gate R31 to open, FIG. 46–A. The CPP's passed here turn the inverter R32 off. The gate R33 is opened at the end of the division as square rooting process and the CPP's from R32 are passed to provide the clearing action.

If the interlock switch is setting at "I" R29 (I) is turned off and R34 is open. In order for a CPP to get through to gate R33 the flip-flop R35 must be set opening

gate R37. This flip-flop is set only when a signal arrives over one of the interlock inputs turning on one of the buffers R38. (This pulse may arrive during the division or root process or even before it starts.)

Thus, if the switch is set on "I" the clearing signals and the output program pulse are not provided until: (1) the division or square rooting process is completed and the control ring steps down to stage seven, and (2) a program signal has arrived over one of the interlock input terminals and set the flip-flop R35. Note that the interlock flip-flop R35 is not reset unless the program control being used is set to "I." This means that a number of divisions or square roots may be done and then the interlock feature be used at the end even though the interlock pulse arrived during one of the earlier divisions.

The setting of the interlock switch determines the conditions for the occurrence of the final addition time of a divider and square rooter program (i.e., the addition time when a program output pulse, answer disposal signal, signal for clearing the argument accumulator's and signals for clearing certain circuits within the divider and square rooter are emitted). If the interlock switch is set at no interlock (NI), the final additional time occurs during the second addition time following the completion of the actual numerical operations involved in a division of square rooting (i.e., during the second addition time of period IV). If the interlock switch is set at I (interlock), not only must period III be completed, but also the divider and square rooter must have received an interlock input pulse before the divider and square rooter program can be considered completed. In the interlock case, the final addition time takes place during the second addition time following whichever of the 2 events hereinafter listed occurs later in the cycle of operations: (1) completion of period III; (2) the reception by the divider and square rooter of an interlock input pulse (see Table 6–11).

The interlock feature of the divider and square rooter is desirable when a division or square rooting program occurs simultaneously with another sequence of programs and is to be followed by a second sequence using either the same units as are used by the sequence in parallel with the division or square rooting or using results obtained from the parallel sequence and results of the division and square rooting. By using the final program output pulse of the sequence in parallel with the division or square rooting as an interlock input pulse and then using the divider and square rooter's program output pulse as the initial program input pulse for the sequence which is to follow the division, the operator insures the completion of all of the programs of the parallel sequence before the commencement of the second sequence.

Had the interlock feature been omitted from the design of the divider and square rooter, the operator, under the same circumstances as those described in the previous paragraph, would have faced two equally disagreeable alternatives: (1) never to schedule a parallel sequence lasting between the minimum time to maximum time for completing a division or square rooting; (2) to compute the maximum number of addition times required to complete the division or square rooting program and then to use the final program output pulse of the sequence in parallel with the division or square rooting to produce eventually (after a delay consistent with the maximum division or square rooting time) an initial program input pulse for the second sequence.

6.2. *The Common Programming Circuits*

The common programming circuits, which constitute most of the divider, will be divided into sections as indicated below. This subdivision is a logical one, that is division is with respect to the purpose of the particular circuit and not with respect to physical location. To a considerable extent this division is indicated on the block diagram (FIG. 46) by the spacing between circuits. The subdivisions are:

(*a*) *The pulse source circuit.*—This circuit centers around the pulse source flip-flop R39 located on FIG. 46–E. The circuit extends up to and including the gates R22 on 46–B.

(*b*) *The program ring circuit.*—The program ring is located on the upper portion of the block diagram, FIG. 46–A. This circuit includes the program ring flip-flop R41 and the associated gates, FIG. 46–D.

(*c*) *The sign indication circuit.*—This circuit (FIG. 46–C) includes the denominator flip-flop, the numerator ring, and the sign indicating matrix (just below).

(*d*) *The over-draft circuit.*—This circuit determines when the numerator changes sign, that is, when there has been an overdraft. This circuit is located at the top center of the block diagram, FIG. 46–B.

(*e*) *The add-subtract circuit.*—This circuit programs the trial additions or subtractions and is located directly under the numerator ring and the sign indication circuit. Its left hand part, FIG. 46–B, consists of the N_α receiver and the D_γ and Q_α receivers. The right hand part, FIG. 46–C, consists of the D_S and D_A receivers and the associated gates, inverters, and buffers.

(*f*) *The round-off circuit.*—The round-off circuit is located practically in the midst of the add-subtract circuits. It consists of the round-off flip-flop and the associated gates and inverters. It includes the gates R43.

(*g*) *The root correction circuit.*—This circuit is essentially the receiver D and the root reset lines.

(*h*) *The shift circuit.*—The shift circuit is below the overdraft circuit and to the right of the pulse source circuit. At the time of overdraft it causes the number in the numerator accumulator to be transmitted to the shift accumulator and then to be transmitted back again. A shifter is used on the input (α) to the numerator accumulator so that the number is shifted one place to the left when it comes back from the shift accumulator. The shift circuits comprise the S_α, N_A, S_A, and N_α receivers and their associated gates and inverters.

(*i*) *The clear and interlock circuits.*—The clear circuits are located in the upper left hand corner of FIG. 46–A to the left of the program ring. These circuits determine when the division or rooting process has finished and (depending upon the setting of the interlock switch of an activated program control) perhaps when some other sequence of computations is finished (as indicated by the output program pulse of that sequence arriving over one of the interlock inputs). Since a division or root process is of unknown length this allows the operator to carry on other computations simultaneously and then to follow with another sequence of computations only when both the division or root process and the other sequence are completed.

6.2.1. *The Pulse Source Circuits*

The pulse source flip-flop is normally in a state which causes gates R44 and R46 to be open. The flip-flop is in this position except for period III. Thus, during periods I, II, and IV central program pulses pass gate R44, go through the inverter R47 and the cathode followers R48 and R49. This produces a general pulse (GP) which does the following things

(1) Goes to gates R22 (1) and R22 (2) to produce a division pulse (DP), FIG. 46–B,

(2) Goes to gates R22 (5) and R22 (6) to produce a square root pulse (SRP), FIG. 46–B,

(3) Goes to gate R51 to clear the program ring, FIG. 46–D,

(4) Goes to gate R52 to set the program ring flip-flop,

(5) Goes to gate R53 to produce a "P" pulse which causes an add-subtract cycle to take place, FIG. 46–E,
(6) Goes to gate R54 to cause a shift cycle to take place,
(7) Goes to gate R55 to produce a root reset pulse,
(8) Goes to gate R56 to produce a "P" pulse which starts another add-subtract cycle after a shift cycle is completed, and
(9) Goes to gate R57 (FIG. 46–B) to step the numerator ring and set the denominator flip-flop in case of negative signs.

The gate R46 passes the one-primed pulse and during a shift cycle this pulse passes gate R58 to step the quotient place ring. Using the 1'P here allows extra time for the quotient ring to step and set up its array of gates.

During period III the flip-flop R39 is set. This opens the gate R59 and the central program pulses pass the inverter R61 and the cathode follower R62 to produce a third period pulse (IIIP). This third period pulse does the following things:

(1) Goes through the buffer R63 and the inverter R64 to give a root reset pulse, FIG. 46–F,
(2) Goes to the gates R22 (3) and R22 (4) to produce a round-off pulse (ROP), FIG. 46–B,
(3) Goes through the buffer R66, inverter R67 and the buffer R68 to the pulse standardizer of the program ring, FIG. 46–A.

The pulse source flip-flop R39 is set during a shift sequence by a pulse passing gate R69. This gate will be opened by the inverter R71 going off, and this is caused by a coincidence between the setting of the place switch and the position of the quotient place ring as detected by one of the gates R72. This flip-flop is reset either by the program ring reaching stage seven and opening gate R73 to pass a CPP or by a Cl' pulse arriving at the buffer R74 from the clear circuits. The Cl' pulse resets this flip-flop when initially clearing whereas the CPP passing R73 indicates the division or rooting is completed and by resetting R39 prevents the program ring from stepping until another program control is activated.

Before a program input pulse is received by a transceiver to stimulate a given program control, but immediately after initial clearing or the completion of a previous program, the status of certain important components of the divider and square rooter's common programming circuits may be summarized as follows:

In the program ring circuit, the pulse source flip-flop and the program ring flip-flop are in the so-called normal state. The program ring (whose stages are designated by A, B, 1, 2, . . . , 7) is in stage A. The observer viewing the divider and square rooter from the front (see FIG. 44) observes that the pulse source and program ring flip-flop neons are lit as is program ring neon A.

The numerator ring of the overdraft circuit is in stage P (the corresponding neon is lit) and the denominator flip-flop of the sign indication circuit is in the normal state (with the denominator flip-flop neon lit). If the previously completed program was a square rooting program, the divide flip-flop is in the normal state and the divide flip-flop neon is off. Otherwise this flip-flop is in the abnormal state and its corresponding neon is on. The interlock, interlock coincidence, and clear flip-flops are in the normal state (and their corresponding neons are off). The receivers of the internal and external-internal programming circuits are all in the normal state and the neons corresponding to them are off.

In the numerical circuits, the place ring is in stage 1 (and the place ring neon numbered 9 in FIG. 44 is on). The +2, −2, +1, and −1 receivers are in the normal state (and their corresponding neons are off).

6.2.2. *The Program Ring Circuit*

As soon as a program control of the divider and square rooter is stimulated, period I is initiated. The characteristics of period I as evidenced in the divider and square rooter's program ring circuit are given in the following paragraphs.

The pulse source flip-flop, FIG. 46–E, remains in the normal state so that a 1'P is gated through R46 to produce a $1'P_1$ and a CPP is gated through R44 to produce a GP pulse every addition time. If the program control's divide-square root and places switch is set at a divide setting and the round-off switch at round-off or no round-off, then GP is gated through R22 (2) or R22 (1) respectively to produce a divide pulse (DP); if the divide-square root and places switch is set at a square root setting and the round off switch at RO or NRO, GP is gated through R22 (5) or R22 (6) respectively to produce a square root pulse (SRP).

During period I, also, the program ring flip-flop, FIG. 46–D, remains in the normal state so that DP or SRP is gated through R76 or R77 respectively, FIG. 46–A, to cycle the program ring 1 stage per addition time.

In the third addition time of period I, the program ring is in stage 1. A signal from this stage gates a GP through gates R51 and through R52 clearing the program ring back to stage A and flipping the program ring into the abnormal state at the end of addition time 3. This marks the termination of period I for division; period I for square rooting lasts one addition time longer. (See Table 6–5 and Table 6–8.)

During period II the pulse source flip-flop remains in the normal state so that GP, $1'P_1$ and either DP or SRP continue to be emitted at the end of every addition time. Since the program ring flip-flop is in the abnormal state (and gates R76 and R77 are closed) neither DP nor SRP can cycle the program ring. The program ring, therefore, continues to register stage A throughout this period.

Period II is terminated and period III initiated when an S pulse (this is a pulse produced by the divider or square rooter when a shift sequence is about to begin—see below) is gated through R69 as a result of the coincidence of a signal from the stage of the place ring corresponding to the places setting of the divide-square root and places switch and a signal from this same switch. The pulse produced in this way is designated in FIG. 46 by the symbol SS. The SS pulse flips the pulse source flip-flop into the abnormal state.

During period III, then, $1'P_1$ and GP (and therefore either DP or SRP) cease to be emitted. Instead, a CPP is gated through R59 at the end of every addition time to produce a pulse designated by IIIP. IIIP cycles the program ring 1 stage per addition time during period III. Also, if the round-off switch has been set at RO, IIIP is gated through R22 (4) or R22 (3) (when the divider-square root and places switch is set respectively at a square-rooting or division point) to produce a round off pulse (ROP) at the end of every addition time in period III. Notice that ROP is emitted only if round off is to take place.

Period III is terminated when the program ring has been cycled through its 9 stages. Period IV is initiated when a CPP is gated through R98 to produce an F pulse and through R73 to produce an F' pulse. The F' pulse resets the pulse source flip-flop into the normal state so that in period IV (as in periods I and II) $1'P_1$, GP and SRP or DP are emitted.

The positions of the program ring at all times is listed in the division and square rooting times tables. The following table gives the effect of each position of the program ring.

TABLE 6-1

Position of program ring	Period I: Division	Period I: Square rooting
A		
B	Gate R 57 is opened to pass a general pulse (GP) through the inverter R79 to the gates R81 and R82 to set the numerator binary ring and the denominator flip-flop in case of negative signs.	Same as for division.
1	(1) Opens gates R51 and R52 to clear program ring and to set the program ring flip-flop. This causes the ring to clear to zero and remain there until period III.	(1) Same as for division.
	(2) Opens gate R83 which passes a division pulse (giving a P pulse) starting the first add or subtract cycle (IIA).	(2) Opens gates R84 and R86. These pass square rooting pulses (SRP) which cause +1 to be placed in the denominator accumulator to start the square root process.

Period III

(Operation is same in division or square rooting)

A	
B	Opens gate R87 to pass a round-off pulse (ROP) giving a P pulse which starts the add or subtract process. Gate R57 is opened but with no effect since general pulses (GP) are not produced in this period.
1	No effect since GP, DP, or SRP pulses are not produced this period.
2	
3	
4	
5	Opens gate R88 to pass an ROP giving a reset pulse which terminates the add or subtract process started above.
6	Opens gate R89 passing an ROP through the inverter R91 to gate R92. In case of no overdraft R92 passes this pulse through the inverter R93 into the round-off circuits. Opens R73 resetting the pulse source flip-flop.
7	Opens R98 which passes a CPP to the clear circuits.

6.2.3. *The Interlock and Clear Circuits*

These circuits consist of three flip-flops and associated gates and inverters. One flip-flop **R35** remembers whether the interlock signal has arrived or not (the interlock signal is the output program pulse for the last operation of the sequence of computations which goes on simultaneously with the root or division process). Another flip-flop **R94** remembers the fact that the division or root process is finished. These two flip-flops open gates **R37** and **R33** which pass a central program pulse serially setting the flip-flop **R96**. The interlock flip-flop **R35** may be by-passed in case the interlock switch is set at "NI." In this case the CPP passes gate **R31** instead of gate **R37**. The pulse passed by **R33** resets the flip-flop **R94**.

The output of flip-flop **R96** opens gate **R97** in the activated transceiver and gate **R98**. A CPP passes gate **R98** and the inverter **R99** to provide the *Cl'* pulse. Thus, CL' is a positive pulse. In some places a negative pulse is needed for the clearing action so the *Cl'* pulse goes through a buffer **R101** to produce the *Cl* pulse—a negative pulse.

The *Cl'* pulse does the following:

(1) May pass gate **R34** (depending upon the position of the corresponding interlock switch) to reset the interlock flip-flop **R35**.

(2) Turns on the buffer **R102** causing the program ring to clear back to stage A.

(3) Turns on the buffer **R74** resetting the flip-flop **R39**.

(4) Turns on the buffer **R103** producing a root reset pulse which resets the D'γ receiver **R104** and the +1 and −1 receivers.

The *Cl* pulse does the following:

(1) Resets the flip-flop **R96**.

(2) Resets the denominator flip-flop **R106**.

(3) Turns off the inverter **R107'** causing the numerator binary to be cleared.

To summarize, the F pulse sets the interlock coincidence flip-flop **R94**. Then the next CPP gated through **R37** if the interlock switch is set at I and the interlock flip-flop has been set as a result of the reception of an interlock input pulse is gated through **R33** (controlled by the interlock coincidence flip-flop). It is to be noted that the interlock flip-flop is insensitive to which of the 8 interlock input terminals has been pulsed. An interlock input pulse received at any of the interlock input terminals sets this flip-flop regardless of which program control on the divider and square rooter has been stimulated. This flip-flop is also insensitive, in some respects, to the time of reception of the interlock input pulse. An interlock input pulse received any time after the completion of one divider and square rooter program (and this may even be before the stimulation of the next divider and square rooter program) serves to flip the interlock flip-flop for the next divider and square rooter program. The signal gated through **R33** resets the interlock coincidence flip-flop and sets the clear flip-flop. The setting of the clear flip-flop results in the emission of a reset signal for the transceiver and the emission of the CL and CL' pulses. The CL and CL' pulses are responsible for clearing the program ring circuit, the place ring, the numerator ring, and the denominator flip-flop prior to the commencement of a divider and square rooter program (see Section 6.2.1).

6.2.4. *The Overdraft and Sign Indication Circuits*

The overdraft and sign indication circuits receive the information upon which they operate (in the case of the overdraft circuit, the sign of the contents of the numerator accumulator and in the case of the sign indication circuit, the sign of the denominator) by means of static leads from the numerator and denominator accumulators' PM counters. The N^- and N^+ lines carry sign signals if the contents of the numerator accumulator are respectively negative or positive. The D^- line delivers signal indication circuits only if the denominator is negative.

The overdraft circuit is a matrix of gates similar to that in the sign indication circuit. This matrix is fed by the output of the numerator ring and by the static outputs of the PM ring in the numerator accumulator. The setting of the numerator ring is fixed during the process of addition or subtraction (in both division and square rooting) and its setting depends upon the original sign of the numerator and the number of shifts which have occurred. When the PM sign of the numerator changes indicating an overdraft the static leads to the overdraft circuit change their potential causing a different gate to conduct.

As explained in the next section the add-subtract cycle takes two addition times. Thus, there is a full addition time after each trial addition or subtraction for the PM static lines from the numerator accumulator and the overdraft circuits to set up.

Thus, the sign indication circuits remember the sign of the denominator by the denominator flip-flop (remains unchanged throughout the whole process) and the sign of the numerator (by the numerator binary ring) (changes after each overdraft); and the overdraft circuit detects a change in sign of the numerator (or radicand in case of square rooting).

After the program ring has reached stage B (in period I), allowing the numerator ring to be stepped if necessary, gate **R107** (3) will be conducting if the numerator is positive or else **R107** (2) in case the numerator is negative. Then gate **R109** is closed and gate **R111** is open. Gate **R111** being open leads to the production of a pulse P which causes the add-subtract cycle to take place. When an overdraft occurs **R107** (1) or **R107** (4) is conducting, causing gate **R111** to close and **R109** to open. This leads to a shift sequence, that is the numerator is sent to

the shift accumulator and then transmitted back through a shifter which moves it one place to the left.

The overdraft circuit consists of the numerator (binary) ring R112 whose stages represent sign P and sign M respectively and the 4 gates R107. Each of the 4 gates receives one input from the numerator ring and the other from either the N^+ or N^- line. The gates R107 may be thought of as (M, N^-), (M, N^+), (P, N^-), and (P, N^+) gates where the first symbol in a parenthesis designates the stage of the numerator ring and the second the numerator sign line to which the gate is connected.

The numerator ring R112 clears to stage P at the end of a program and, in the midst of a program, can be cycled only during period I or at specific times in periods II and III. In period I, when the program ring is in stage B, a GP is gated through R57, the resulting signal is gated through R81 to cycle the numerator ring from stage P to M only if the numerator is negative. During period II and III, the numerator ring can be cycled only when R80 opens to pass a CPP. Gate R80, however, is open only when the S_α receiver is set and this receiver is set only after an overdraft has occurred.

Thus, the 4 gates receive information about the current sign indication of the contents of the numerator accumulator over the static leads from the numerator accumulator's PM circuit. The numerator ring, on the other hand, registers the sign of the contents of the numerator accumulator before the denominator is either subtracted from or added to the contents of the numerator accumulator. The 4 gates in the overdraft circuit compare the current with the past sign of the contents of the numerator accumulator. The coincidence of signals to gate R107 (2) (M, N^-) or R107 (3) (P, N^+) leads to the emission of an NO signal. Similarly gate R107 (1) or R107 (4) emits an O signal upon the coincidence of signals on both inputs.

As long as an NO signal is emitted the basic operation sequence of period II is performed. When an O signal is emitted, the basic operation sequence is interrupted either by a shift sequence or by the initiation of period III. The O and NO signals produce these results by inhibitory actions since no inverters intervene between the gates of the overdraft circuit and the gates to which O and NO are delivered. When NO is emitted, gate R109 is closed and gate R111 passes a signal which gates a GP through R53. The resulting pulse is designated by P. The P pulse is produced in other ways when the sensing of overdraft is irrelevent or unnecessary. At the end of period I in division, a signal from stage 1 of the program ring gates DP through R83 to produce a P pulse. Also, after shifting of the numerator accumulator's contents in period II, a signal from the N′ receiver gates a GP through R36 to produce a P pulse. In period III, the P pulse is produced when a signal from stage B of the program ring gates an ROP through R87. The P pulse, in period II, initiates the basic operation sequence; and in period III, initiates the 5 substractions or additions of the denominator to the contents of the numerator accumulator by setting the N_γ receiver and either the D_S or D_A receiver. In period III, moreover, when NO is emitted, gate R92 passes a signal (emitted when a signal from stage 6 of the program ring opens gate R89 so that an ROP can pass) which activates the correction of the answer in accordance with the state of the divide flip-flop. When the O signal is emitted, gates R111 and R92 are closed and gate R109 passes a signal from the D_γ or Q_α receiver which, in turn, gates a CP through R54 to produce an S pulse. The S pulse motivates the shift sequence of period II or, when gated through R69 to produce an SS pulse initiates period III.

The sign indication circuit is quite similar to the overdraft circuit in its components and functioning. This circuit consists of 4 gates R108, the denominator flip-flop R106. Each gate is connected to one of the 2 output leads from the denominator flip-flop and to either the P or M stage of the numerator ring. The denominator flip-flop is in the normal state when a program commences and can be flipped into the abnormal state to remember the fact that the denominator is negative at only one specific time in the course of a divider and square rooter program. This one specific time is addition time 2 of period I when gate R57, held open by a signal from stage B of the program ring, passes a GP which can then pass through gate R82 to flip the denominator flip-flop if the contents of the denominator accumulator are negative. Once flipped, the denominator flip-flop remains in the abnormal state until reset by CL in period IV.

If the denominator is positive (and therefore the denominator flip-flop is in the normal state) and the contents of the numerator accumulator before a subtraction or addition of the denominator are positive or negative. (So that the numerator ring registers P or M respectively), then gates R108 (4) or R108 (2) respectively emits a like sign or unlike signal. Similarly, gates R108 (1) and R108 (3) emit a like or unlike sign signal respectively.

Note that the arrangement of the gate tubes in this circuit is not the usual plan followed elsewhere in the ENIAC. Usually, there is an inverter between two gates. If the first gate tube begins to conduct it causes the inverter to go off. The resulting positive signal causes the second gate tube to conduct (assuming the other control grid is sufficiently positive). Here in the sign indication circuit (the same is true in the overdraft circuit, see Section 6.2.4) there is no inverter between the gate tubes. The plates of R108 (4) and R108 (1) are connected to one control grid of the gate tubes R113, R43 (1) and R43 (2). Thus, if gate R108 (4) or R108 (1) is conducting, the grids of the three gates are held below cut-off and none of them can conduct. On the other hand, if neither of these gates is conducting then their plate potential is relatively high and the gates R113, R43 (1), and R43 (2) will conduct if a relatively positive signal is applied to their other control grids.

The like sign signal closes gate R113 so that gate R114 passes a P pulse (see Section 6.2.4) which sets the D_S receiver. The unlike sign signal closes gate R114 so that gate R113 passes a P pulse which sets the D_A receiver. The coincidence of like or unlike sign signal and a signal from the round off flip-flop also determines which receivers of the internal-external progarmming circuits and of the numerical circuits are set in period III.

Note that the denominator flip-flop is changed only at the beginning of the process, that is, it does not change its state during the process of division or square rooting. On the other hand, the numerator ring is stepped at the start for negative numerators and, in any case, is stepped during each shift sequence. At the end of the process the clear pulse (*Cl*) arrives from the clearing circuits and resets the flip-flop and clears the numerator binary ring.

6.2.5. *The External-Internal Programming Circuits*

A program input pulse delivered to a program pulse input terminal of the divider and square rooter immediately passes through the numerator and denominator accumulator switches (R3 and R4) whence it sets the N_α or N_β and D_α or D_β receivers R7. Thus, during addition time 1 of period I, the numerator and denominator accumulators receive their arguments if this reception is controlled by the divider and square rooter. The arguments may of course, be received prior to this if their reception is controlled locally at the accumulators. At the end of addition time 1, a CPP resets these receivers and they do not function again in any subsequent period of the program.

The N_γ and D_A or D_S receivers (in the Add-Subtract circuit) function during period II and, if round off is specified, during period III. The P pulse (see Section 6.2.4) sets the N_γ (R116) receiver at the same time that it sets the D_A or D_S receivers R117 (depending on whether the unlike or like sign signal is being emitted). During period II, GP resets these receivers one addition time after they have been set. In period III of round off programs,

the N_γ and D_A or D_S receivers remain set throughout addition times 3, 4, 5, 6, and 7. At the end of addition time 7 an ROP gated through **R88** by a signal from stage 5 of the program ring resets these receivers. Thus, the denominator is subtracted from or added to the contents of the numerator accumulator 5 times in round off programs.

During period II, when DP or SRP is being emitted, the setting of the N_γ receiver leads, one addition time later, to the setting of the Q_α side of receiver **R118** in the presence of a division pulse (DP) or the D_γ side of receiver **R118** in the presence of a square root pulse (SRP). Simultaneous with the setting of the Q_α receiver, DP sets the +1 side of receiver **R150** if the D_S side of receiver **R117** was previously set or the −1 side of receiver **R150** if the D_A side of receiver **R117** was previously set. Similarly, in square rooting programs, the +2, or −2 side of receiver **R151** is set at the same time as the D_γ receiver is.

During period III of round off programs, the setting of the D_γ or D_α receiver does not result from the setting of the N_γ receiver, but, instead, takes place if a ROP is gated through **R92** because NO is emitted. The ROP is then routed to set either the D_γ or Q_α receiver by means of gates controlled by the round off flip-flop. This same ROP and other gates controlled by the round off flip-flop effects the setting of the +2 or −1 receiver (if the D_S receiver was set during addition times 3–7) or the −2 or −1 receiver (if the D_A receiver was previously set).

During period II, the emission of an O signal leads to the emission of an S pulse (see Section 6.2.4). The S pulse sets the S_α and N_{AC} receivers. A CPP gated through **R119** as a result of the setting of the S_α receiver causes the setting of the S_{AC} and N'_γ receiver **R121**. Thus, in either division or square rooting, the shifting of the contents of the numerator accumulator one place to the left is provided for.

The S pulse also sets the D'_γ receiver **R104** and, gated through **R122** or **R123** by a signal from the +2 or −2 sides of receiver **R151** respectively, sets the −1 or +1 receiver. The D'_γ receiver and the +1 or −1 receiver remain set for 2 addition times in period II for square rooting. They are reset when a CPP is gated through **R124** after the NO state of affairs is restored in the overdraft circuit. Since the D'_γ and +1 or −1 receivers remain set for 2 addition times and, since the place ring is not cycled until the second addition time (see Section 6.3), the correction of twice the root as described in Section 6.0 (a change of one unit first in one decade place and then in a decade place one further to the right) takes place: It is to be noted that in period II for division, the D'_γ receiver is set but that there is nothing for the denominator accumulator to receive at the time since neither the +1 nor the −1 receiver is set in division. DP resets the D'_γ receiver in the division case one addition time after its setting.

At the beginning of period III, also, the S pulse sets the S_α and N_{AC} receivers and one addition time later the S_{AC} and N'_γ receivers are set. In period III, the D'_γ receiver is set and either the +1 or the −1 receiver is also set in the case of a square rooting program. It is to be noted, however, that IIIP resets the D'_γ receiver and the +1 or −1 receiver one addition time after their setting in period III so that twice the square root is corrected by only one unit in the last answer place.

When the clear flip-flop **R96** is set (see Section 6.2.3), gate **R97** in the transceiver emits a signal which has 3 effects: (1) passing through the answer disposal switch, it sets the answer disposal receiver (1, 2, 9, 11) specified by the setting of switch **R126**; (2) passing through the numerator and denominator accumulator clear switches **R3** and **R4**, it allows the carry clear gate to pass through gate **R13** (1) (if only the denominator accumulator is to be cleared), through gates **R13** (2) and **R13** (3) (if both the numerator and denominator accumulators are to be cleared), or through gate **R13** (4) (if only the numerator accumulator is to be cleared); (3) it gates a CPP through **R127** to provide the transceiver's reset signal and a program output pulse.

Thus clearing of the numerator and/or denominator accumulators takes place a little prior to the emission of a program output pulse and answer disposal signal.

6.2.6. *The Divide Flip-Flop*

The divide root flip-flop **R142** is set or reset during period I of divider and square rooter programs. In division programs DP flips this flip-flop into the abnormal state (and turns on the corresponding neon); in square rooting programs, SRP resets this flip-flop if it was previously flipped into the abnormal state in a division program.

The effects of this flip-flop on the divider and square rooter's common programming circuits become apparent in addition time 8 of period III for round off programs when an ROP is gated through **R89** by a signal from stage 6 of the program ring. If the signal from gate **R89** is gated through **R92** as a result of the emission of the NO signal, then, in the division case, this signal is gated through **R128** to set the Q_α receiver and through gate **R129**. The signal from gate **R129** is gated through **R43** (4) to set the +1 receiver or through gate **R43** (1) to set the −1 receiver when the like or unlike sign signal respectively is emitted. Similarly, in the square rooting case, the D_γ receiver is set by a signal gated through **R131** and either the +2 or −2 receiver on the coincidence of a signal from gate **R132** and either the like or unlike sign signal respectively.

6.2.7. *Chronological Description of the Common Programming Circuits*

Tables 6–5, 6–6 and 6–7 summarize the operation of the common programming circuits during periods I, II, and III respectively of a division program. The corresponding summaries for the square rooting case are found in Tables 6–8, 6–9, and 6–10. Table 6–11 summarizes the events of period IV for both square rooting and division.

Below the title, each table carries a statement indicating the number of addition times required to complete the events of the period. In some cases, the events which occur in the last addition time of the period are listed in the comment column beside the events of the next to the last addition time instead of on a separate line (e.g., the events of addition time 4, period I, for square rooting in Table 6–8). This is done when the event described occurs, not in the common programming circuits of the divider and square rooter, but rather in an associated accumulator.

The overlapping of periods is also indicated on the tables. For example, addition time 3 of period I for division overlaps with addition time *d* of period II for the first basic division sequence. Thereafter, addition time *d* overlaps with the second addition time of the basic division sequence or with the second addition time of the shift sequence.

It is recommended that Tables 6–5 through 6–11 be compared, at this time, with the illustrative problems in Tables 6–1 and 6–2.

From the tables, it appears immediately that the exact number of addition time required to complete any given division program (provided that the divider and square rooter need not mark time waiting for an interlock input pulse) is $14+2(p-2)+2$ (number of additions or subtractions of the denominator) and that the number of addition times for any given square rooting program is $15+2(p-2)+2$ (number of additions or subtractions of the contents of the denominator accumulator) where p is the number of places specified by the setting of the divide-square root. Since overdraft can never occur in division by zero, division by zero consumes an infinite number of addition times. If denominator equal to zero is a computational possibility, the operator should precede division programs by discrimination programs with the purpose of avoiding such divisions.

TABLE 6-5.—DIVISION—INITIAL SEQUENCE—PERIOD I

[Requires three addition times: 1-3]

Add. Time (and Prog. Ring stage)	Signal	Effect	Comment
0 (A)	(1) Program input pulse	(1) (a) Sets transceiver in the divider. (b) Sets N_α or N_β and/or D_α or D_β receivers	(1) (a) (b) The numerator and/or denominator are then received by the numerator and/or denominator accumulator respectively in add. time 1.
1 (A)	(1) CPP	(1) Gated through R44 by a signal from the pulse source flip-flop (in the normal state) produces a GP pulse.	(1) This effect occurs in every subsequent add. time of a division program except during period III.
	(2) GP	(2) Gated through R22 (1) or (2) produces a DP pulse.	(2) This effect occurs in every subsequent add. time of a division program except during period III.
	(3) DP	(3) (a) Gated through R76 by a signal from the program ring flip-flop, cycles the program ring to stage B. (b) Sets the divide flip-flop if this flip-flop is in the normal state.	(3) (a) (b) This turns on the divide flip-flop neon.
2 (B)	(1) GP gated through R57 by a signal from stage B of the program ring.	(1) Is then gated through gate R81 by the N- signal so that the numerator binary ring is cycled to stage M in the event that the numerator is negative.	
	(2) D- signal	(2) Is gated through R82 by the output of gate R57. Output of gate R82 sets the denominator flip-flop in the event that the denominator is negative.	(2) This turns off the denominator flip-flop neon.
	(3) DP	(3) Cycles the program ring to stage 1	
3 (1)	(1) DP	(1) (a) Gated through R83 by a signal from stage 1 of the program ring produces a P pulse.	
	(2) P	(2) (a) Sets the N_γ receiver. (b) Gated through R114 when the like sign signal closes R113 sets the D_B receiver or gated through R113 when the unlike sign closes R114 and sets the D_A receiver.	(2) (a and b) Then during add. time 4, the numerator accumulator receives either the complement of the denominator or the denominator. At the end of add. time 4, GP resets these receivers. The setting of these receivers is the event described (in the table for period II) as occurring in add. time d=3+2n for n=0.
	(3) GP	(3) (a) Gated through R51 by a signal from stage 1, clears the program ring to stage A. (b) Gated through R52 flips the program ring flip-flop.	(3) (a) (b) The program ring flip-flop neon is turned off at this time.

TABLE 6-6.—DIVISION PERIOD II—BASIC DIVISION SEQUENCE

[Requires two add. times: $d+1$ and $d+2$]

Add. Time (and Prog. Ring Stage)	Signal	Effect	Comment
	For n=0, this add. time is counted as part of period I. For n>0, this add. time coincides with add. time s+2 of period II or add. time d+2 of period I		
d=3+2n for n=0. For n≥0 see period I. (A)	(1) P pulse derived from GP gated through R53 as a result of the coincidence of the NO signal and a signal from the Q_γ receiver or GP gated through R56 by a signal from the N'_γ receiver. or (see period I) DP gated through R83 by a signal from stage 1 of the program ring.	(1) (a) Sets the N receiver. (b) Gated through R114 when the like sign signal closes R113. P sets the D_B receiver or gated through R113 when the unlike sign signal closes R114, P sets the D_A receiver.	(1) During add. time d+1, then, the numerator accumulator receives either the complement of the denominator (when the numerator and denominator have the same signs) or the denominator (when the numerator and denominator have unlike signs). While these receivers are set, the corresponding neons are on. At the end of add. time d+1, these receivers are reset by a GP.
d+1	(1) DP	(1) (a) Gated through R133 by a signal from the N_γ receiver, sets the Q_α receiver. (b) Gated through R136 by a signal from the D_B receiver, sets the +1 receiver or, gated through R137 by a signal from the D_A receiver, sets the −1 receiver.	(1) During add. time d+2, then, the quotient accumulator receives 1 in a given decade place if the denominator was subtracted from the numerator or receives the complement of 1 if the denominator was previously added to the numerator. The neons corresponding to these receivers are on as long as the receivers are set. The Q_α receiver is reset by a CPP and the +1 or −1 receiver is reset by a DP at the end of add. time d+2.

SHIFT SEQUENCE

[Requires two add. times: s+1, s+2]

	This add. time coincides with add. time d+2 above		
s=3+2n for n≥1.	(1) S pulse produced when a GP is gated through R54 as a result of the coincidence of an O signal and a signal from the Q_α receiver.	(1) (a) Sets the S_α and NAC receivers.	(1) (a) During add. time s+1, the numerator is transmitted (with clearing) from the numerator accumulator and received in the shift accumulator. At the end of add. time a+1, a CPP resets the S receiver and NAC receiver.

TABLE 6-6.—DIVISION PERIOD II—SHIFT SEQUENCE—Continued

[Zequires two add. times: s+1, s+2]

Add. time (and Prog. Ring Stage)	Signal	Effect	Comment
		(b) Sets the D'_γ receiver	(b) There is no numerical effect on the division from the setting of the D'_γ receiver since there is no data for the denominator accumulator to receive during add. time s+1. This receiver is reset at the end of add. time s+1 by a DP.
		(c) If gated through R69 as a result of the coincidence of signals from the places switch and place ring, produces an SS pulse (see Table 6-6).	(c) SS pulse terminates period II and initiates.
s+1	(1) Signal from the S_α receiver R138	(1)	(1)
(A)		(a) Gates $1'P_1$ through R58 to produce $1'P_2$ which cycles the place ring 1 stage.	(a)
		(b) Gates a CPP through R80 so that the numerator binary ring is cycled 1 stage.	(b) As a result O ceases to be emitted and NO is emitted instead.
		(c) Gates a CPP through R119 so that the N'_α and S_{AC} receivers are set.	(c) Then the shift accumulator transmits (and clears) its contents to the numerator accumulator during add. time s+2. At the end of add. time s+2, a CPP resets the N'_γ and S_{AC} receivers.

TABLE 6-7.—DIVISION PERIOD III—ROUND OFF OR NO ROUND OFF

[Items relevant only to the round-off case are circled. Requires 9 add. times: 1–9]

Add. Time	Signal	Effect	Comment
		This add. time coincides with add. time d+2 of period II	
0	(1) S pulse produced when a GP is gated through R54 as a result of the coincidence of an O signal and a signal from the Q_α receiver.	(1)	(1)
(A)		(a) Sets the S_α and N_{AC} receivers	(a) *During add. time 1*, then the numerator accumulator transmits (and clears) its contents to the shift accumulator. A CPP resets these receivers in *add. time 1*.
		(b) Sets the D'_γ receiver	(b) Since *during add. time 1*, there is no numerical data on the tray from which the D_γ channel receives, there is no numerical result from 16.
		(c) Gated through R69 as a result of the coincidence of signals from the places switch and place ring, produces an SS pulse.	
	(2) SS pulse	(2) Sets the pulse source flip-flop	(2) At this time, the pulse source flip-flop neon is turned off.
1	(1) CPP	(1)	(1)
(A)		(a) Gated through R80 by a signal from the S_α receiver, cycles the numerator binary ring.	(a) So that NO ceases to be emitted and O is emitted by the sign indicating circuit.
		(b) Gated through R119 by a signal from the S_α receiver, sets the S_{AC} and N'_γ receivers.	(b) So that, *during add. time 2*, the numerator accumulator receives the number transmitted (with clearing) from the shift accumulator. At the *end of add. time 2*, these receivers are reset by a CPP.
		(c) Gated by R59 produces a III Pulse	(c) This pulse is produced in every subsequent add. time of period III.
	(2) IIIP	(2) (a) (Gated by R22 (3) produces ROP)	(2) (a) ROP is produced in every subsequent add. time of period III if round off is specified.
		(b) Cycles the program ring to stage B	
		(c) Resets the D'_γ receiver	
	(1) IIIP	(1) Cycles Program ring to stage 1	(1)
(B)	(2) ROP	(2) (Gated through R87 by a signal from stage B of the program ring produces a P pulse.)	(2)
	(3) P	(3) (Sets N_γ and D_A or D_S receiver depending on whether unlike sign or like sign signal is emitted.)	(3) These receivers remain set *during add. times 3*, 4, 5, 6, and 7 (See below). They are reset at the *end of add. time 7*. Therefore, the numerator accumulator receives either the denominator or its complement five times.
3	(1) IIIP	(1) Cycles program ring to stage 2	
(1)			
4	(1) IIIP	(1) Cycles program ring to stage 3	
(2)			
5	(1) IIIP	(1) Cycles program ring to stage 4	
(3)			

TABLE 6-7.—DIVISION PERIOD III—ROUND OFF OR NO ROUND OFF—Continued

[Items relevant only to the round off case are circled. Requires 9 add. times: 1-9]

Add. Time	Signal	Effect	Comment
6 (4)	(1) IIIP	(1) Cycles program ring to stage 5	
7 (5)	(1) ROP	(1) (Gated through R88 by a signal from stage 5 of the program ring, resets the N_γ and D_A or D_B receivers.)	
	(2) IIIP	(2) Cycles the program ring to stage 6	
8	(1) ROP	(1) (Gated through R89 by a signal from stage 6 of the program ring produces a signal which, if gated through R90 by NO, passes through R128 to set the Q_α receiver and through R129. The signal from R129 passes through R43 (4) when the like sign signal is emitted and sets the +1 receiver or passes through R43 (1) to set the −1 receiver when the unlike sign signal is emitted.)	(1) Thus, if the subtraction or addition of 5 times the denominator which takes place during add. times 3 through 7 does not produce an overdraft, *during add. time 9* the quotient is increased (when numerator and denominator have like signs) or decreased (when numerator and denominator have unlike signs) by 1 unit in the last place at the right as specified by the setting of the places switch. At the *end of add. time 9*, IIIP resets and the +1 or −1 receiver and a CPP resets the Q_α receiver.
	(2) IIIP	(2) Cycles the program ring to stage 7	

TABLE 6-8.—SQUARE ROOT PERIOD I

[Requires four add. times: 1-4]

Add. Time (and Prog. Ring Stage)	Signal	Effect	Comment
0 (A)	(1) Program input pulse	(1) (a) Sets transceiver in the divider and square rooter. (b) Sets N_α or N_β receiver	(1) (b) The numerator is then received by the numerator accumulator *during add. time 1*.
1 (B)	(1) CPP	(1) Gated through R44 by a signal from the pulse source flip-flop, produces a GP pulse.	(1) This effect occurs in every subsequent add. time of a square root program except during period III.
	(2) GP	(2) Gated through R22 (6) or R22 (5) produces a SRP.	(2) This effect occurs in every subsequent add. time of a square root program except during period III.
	(3) SRP	(3) (a) Gated through R77 by a signal from the program ring flip-flop, cycles the program ring to stage B. (b) Resets the divide flip-flop if this flip-flop is in the abnormal state.	(3) (b) This turns off the divide flip-flop neon.
2 (1)	(1) GP gated through R57 by a signal from stage B of the program ring.	(1) Gated through R81 by the N− signal cycles the numerator ring to stage M if the radicand is negative.	(1) The divider and square rooter, however, does not find the real coefficient of i correctly if the radicand is negative.
	(2) SRP	(2) Cycles the program ring to stage 1	
3 (A)	(1) SRP	(1) (a) Gated through R84 by a signal from stage 1 of the program ring, sets the D_γ receiver. (b) Gated through R86 by a signal from stage 1 of the program ring, sets the +1 receiver.	(1) (a and b) Thus, during add. time 4, the denominator (twice the root) accumulator receives 1 pulse in the 10^8 decade. At the *end of add. time 4*, a CPP resets the D_γ receiver and a CPP gated through as a result of the coincidence of the NO signal and a signal from the D_γ receiver, resets the +1 receiver.
	(2) GP	(2) (a) Gated through R51 by a signal from stage 1, clears the program ring to stage A. (b) Gated through R52 by a signal from stage 1 flips the program ring flip-flop.	(2) (b) The program ring flip-flop neon is turned off at this time.

TABLE 6-9.—SQUARE ROOT PERIOD II—BASIC SQUARE ROOT SEQUENCE

[Requires two add. times; r+1, r+2]

Add. Time	Signal	Effect	Comment
	For n=0, this add. time coincides with add. time 4 of period I. For n>0, this add. time coincides with add. time s+2 or r+2 of period II.		
r(=4+2n for n≥0). (A)	(1) P pulse derived from GP gated through R53 as the result of the coincidence of a signal from the D_γ receiver and an NO signal or GP gated through R56 by a signal from the N'_γ receiver (after a shift sequence).	(1) (a) Sets the N_γ receiver. (b) Gated through R114 when the like sign signal is emitted, sets the D_B receiver or gated through R113 when the unlike sign signal is emitted, sets the D_A receiver.	(1) (a and b) Thus, during add. time r+1, the numerator accumulator receives the complement of the denominator (when N and D have like signs) or receives the denominator (when N and D have unlike signs). These receivers are reset by GP at the *end of add. time r+1*.
r+1 (A)	(1) SRP	(1) (a) Gated through R134 by a signal from the N_γ receiver sets the D_γ receiver. (b) Gated through R139 or R141 respectively by a signal from the D_B or D_A receiver sets the +2 or −2 receiver	(1) (a and b) Thus, in add. time r+2, the denominator accumulator receives two in a given decade place of the complement of 2 if the denominator was previously subtracted or added respectively. The D_γ receiver and the +2 and −2 receivers are reset by a CPP at the *end of add. time r+2*.

TABLE 6-9.—SQUARE ROOT PERIOD II—SQUARE ROOT—SHIFT SEQUENCE—Continued

[Requires two addition times: s+1, s+2]

Add. Time	Signal	Effect	Comment
		This add. time coincides with add. time r+2	
s(=4+2n for n≥1). (A)	(1) S pulse produced when a GP is gated through R54 as a result of the coincidence of an O signal and a signal from the D_γ receiver.	(1) (a) Sets the S_α and N_{AC} receivers. (b) Sets the D'_γ receiver. (c) Gated through R122 by a signal from the +2 receiver, sets the −1 receiver or gated through R-123 by a signal from the −2 receiver, sets the +1 receiver. (d) If gated through R69 as a result of the coincidence of signals from the places switch and places ring produces an SS pulse (see Table 6-10).	(1) (a) As a result, the shift accumulator receives the numerator from the numerator accumulator which transmits and clears during add. time s+1. At the end of add. s+1, a CPP resets these receivers. (b and c) During add. time s+1, then, the denominator accumulator receives the complement of 1 or receives 1 in a given decade place if during the previous sequence, the denominator accumulator received +2 or −2 respectively in the same decade place. The D'_γ receiver and the +1 or −1 receiver remain set *through add. time s+2*. (d) SS pulse initiates period III. (See chart for period III.)
s+1 (A)	(1) Signal from the S_α receiver.	(1) (a) Gates $1'P_1$ through R58 to produce $1'P_2$ which cycles the place ring one stage. (b) Gates a CPP through R80 so that the numerator binary ring is cycled 1 stage. (c) Gates a CPP through R119 so that the N'_γ and S_{AC} receivers are set.	(1) (b) As a result O ceases to be emitted and NO is emitted instead. (c) *During add. time s+2*, then, the numerator accumulator receives the contents of the shift accumulator which transmits and clears. At the end of add. time s+2, a CPP resets the N'_γ and S_{AC} receivers.
	(2) See 1c of addition time s.	(2) The D'_γ and +1 or −1 receiver remains set.	(2) Therefore, during add. time s+2, the denominator accumulator receives +1 or the complement of 1 but this time one decade place further to the right than *during add. time s+1*. At the *end of add. time s+2*, GP gated through R55 by a signal from the N'_γ receiver resets the D'_γ receiver and the +1 or −1 receiver.

TABLE 6-10.—SQUARE ROOT PERIOD III—ROUND OFF OR NO ROUND OFF PERIOD

[Requires nine add. times: 1-9. Items relevant to the round off case only are circled]

Add. Time	Signal	Effect	Comment
		This add. time coincides with add. time r+2 of period II.	
0 (A)	(1) S pulse produced when a GP is gated through R54 as a result of the coincidence of an O signal and a signal from the Q_α receiver.	(1) (a) Sets the S_α and N_{AC} receivers. (b) Sets the D_γ receiver. (c) Gated through R122 by a signal from the +2 receiver, sets the −1 receiver or gated through R123 by a signal from the −2 receiver sets the +1 receiver. (d) Gated through R69 as a result of the coincidence of signals from the places switch and place ring produces an SS pulse.	(1) (a) *During add. time 1*, then, the numerator accumulator transmits (and clears) its contents to the shift accumulator. A CPP resets these accumulators in *add. time 1*. (b and c) Thus, *during add. time 1*, the denominator accumulator receives the complement of −1 or +1 in a given decade place if in the previous square root sequence, +2 or its complement respectively was received in that decade place. At the *end of add. time 1*, IIIP (see below) resets the D'_γ and +1 or −1 receivers.
	(2) SS	(2) Sets the pulse source flip-flop.	(2) At this time, the pulse source flip-flop neon is turned off.
1 (A)	(1) CPP	(1) (a) Gated through R80 by a signal from the S_α receiver cycles the numerator binary ring. (b) Gated through R119 by a signal from the S_α receiver, sets the S_{AC} and N'_γ receivers. (c) Gated by R59 produces a IIIP.	(1) (a) So that NO ceases to be emitted and O is emitted instead. (b) So that *during add. time 2*, the numerator accumulator receives the numerator from the shift accumulator which transmits and clears. At the *end of add. time 8*, a CPP resets these receivers. (c) This pulse is produced in every subsequent add. time of period III.
	(2) IIIP	(2) (a) Gated by R22 (4) produces an ROP pulse. (b) Cycles the program ring to stage B. (c) Resets the D'_γ receiver and the +1 or −1 receiver.	(2) (a) ROP is produced in every subsequent add. time of period III if round off is specified.
2 (B)	(1) IIIP (2) ROP (3) P	(1) Cycles program ring to stage 1. (2) Gated through R87 by a signal from stage B of the program ring produces a P pulse. (3) Sets N_γ receiver and D_A or D_S receiver if the unlike or like sign signal respectively is emitted.	(1) (2) (3) These receivers remain set *during add. times 3, 4, 5, 6, 7*. They are reset at the *end of add. time 7* (see below). Therefore, the numerator accumulator receives either the denominator or its complement five times.

TABLE 6-10.—SQUARE ROOT PERIOD III—ROUND OFF OR NO ROUND OFF PERIOD—Continued

[Requires nine add. times: 1-9. Items relevant to the round off case only are circled]

Add. Time	Signal	Effect	Comment
3 (1)	(1) IIIP	(1) Cycles program ring to stage 2	
4 (2)	(1) IIIP	(1) Cycles program ring to stage 3	
5 (3)	(1) IIIP	(1) Cycles program ring to stage 4	
6 (4)	(1) IIIP	(1) Cycles program ring to stage 5	
7 (5)	(1) ROP	(1) Gated through R88 by a signal from stage 5 of this program ring resets the N_γ and D_A or D_S receivers.	
	(2) IIIP	(2) Cycles the program ring to stage 6	
8 (6)	(1) ROP	(1) Gated through R89 by a signal from stage 6 of the program ring produces a signal which if gated through R92 by NO, passes through R131 to set the D_γ receiver and passes through R132. The signal from R132 passes through R43 (3) when the like sign is emitted and sets the +2 receiver or passes through R43 (2) when the unlike sign signal is emitted and sets the −2 receiver.	(1) Thus, if the subtraction or addition of 5 times the denominator which occurs *during add. times 5 through 7* does not produce an overdraft, *during add. time 9*, the quotient is increased (when N and D have like signs) or decreased (when N and D have unlike signs) by 2 units in the last place at the right as specified by the setting of the places switch. *At the end of add. time 9*, III P resets the +1 or −1 receiver and a CPP resets the D_γ receiver.

TABLE 6-11.—PERIOD IV FOR EITHER DIVISION OR SQUARE ROOT—INTERLOCK OR NO INTERLOCK PERIOD

[Requires 2 add. times 1, 2. Items relevant to the interlock case only are circled]

Add. Time	Signal	Effect	Comment
		This add. time coincides with add. time 9 of period III.	
0 (7)	(1) CPP	(1) (a) Gated through R78 by a signal from stage 7, of the program ring, produces an F pulse. (b) Gated through R73 by a signal from stage 6 of the program ring produces an F pulse.	(1)
	(2) F	(2) Sets the interlock coincidence flip-flop	(2) This turns on the interlock coincidence flip-flop neon.
	(3) F′	(3) Resets the pulse source flip-flop	(3) So that the pulse source flip-flop neon is turned on again.
1 (7)	(1) CPP	(1) Gated through R44 produces a GP	
	(2) GP	(2) Gated through R22 (2) or R22 (1) produces a DP or through R22 (5) or R22 (6) produces a SRP.	(2) These three pulses continue to be produced every add. time of period IV but have no effect on the division or square rooting.
	(3) 1′P	(3) Gated through R46 produces 1′P_1	
	(4) CPP	(4) Gated through R31 in the NI case or (gated through R37 in the I* case) produces a signal which is gated through R33 to set the clear flip-flop and to reset the interlock coincidence flip-flop.	(4) The clear flip-flop neon goes on at this time and the interlock coincidence flip-flop neon goes off.
2 (7)	(1) CPP	(1) Gated through R98 by a signal from the clear flip-flop, produces a CL′ pulse.	
	2) CL′	(2) (a) (Gated through R34 by a signal from the interlock switch, resets the interlock flip-flop.) (b) Clears the program ring to stage A. (c) After passing through buffer R101 becomes a CL pulse.	
	(3) CL	(3) (a) Resets the clear flip-flop. (b) Clears the numerator binary ring to stage P. (c) Resets the denominator flip-flop. (d) Clears the place ring to stage 1. (e) Resets the program ring flip-flop.	
	(4) Signal resulting from the coincidence of the transceiver's being set and the clear flip-flop's being set.	(4) (a) Allows the carry clear gate to pass to the numerator and/or denominator accumulator clear circuits if clearing is specified. (b) Gates a CPP through R127 to provide a reset signal for the transceiver and a program output pulse. (c) Gates a CPP to set one of the four answer disposal receivers.	(4) (c) Thus, during the add. time following the divider's program output pulse, the answer is disposed of in accordance with the setting of the answer disposal switch. At the end of add. time 3, the answer disposal receiver is reset by a CPP.

*If the interlock input pulse is not received until k addition times after add. time 0 of period IV, this event and all events listed next to addition time 2 occur k addition times later than that indicated in this table.

TABLE 6-12.—POSSIBLE PLACEMENT OF RADICAND

[Also see Table 6-13]

Period	Add. Time	Numerator (Radicand) Accumulator		Denominator (Two Root) Accumulator		Shift Accumulator	
		Receives	Stores after receiving	Receives	Stores after receiving	Receives	Stores after receiving
Example A							
I	1	P 0 900 000 000	P 0 900 000 000				
	2						
	3						
	4			P 0 100 000 000	P 0 100 000 000		
II	5	M 9 900 000 000	P 0 800 000 000				
	6			P 0 200 000 000	P 0 300 000 000		
	7	M 9 700 000 000	P 0 500 000 000				
	8			P 0 200 000 000	P 0 500 000 000		
	9	M 9 500 000 000	P 0 000 000 000				
	10			P 0 200 000 000	P 0 700 000 000		
	11	M 9 300 000 000	M 9 300 000 000				
	12			P 0 200 000 000	P 0 900 000 000		
Shift	13			M 9 900 000 000	P 0 800 000 000	M 3 000 000 000	M 3 000 000 000
Example B							
I	1	P 2 401 000 000	P 2 401 000 000				
	2						
	3						
	4			P 0 100 000 000	P 0 100 000 000		
II	5	M 9 900 000 000	P 2 301 000 000				
	6			P 0 200 000 000	P 0 300 000 000		
	7	M 9 700 000 000	P 2 001 000 000				
	8			P 0 200 000 000	P 0 500 000 000		
	9	M 9 500 000 000	P 1 501 000 000				
	10			P 0 200 000 000	P 0 700 000 000		
	11	M 9 300 000 000	P 0 801 000 000				
	12			P 0 200 000 000	P 0 900 000 000		
	13	M 9 100 000 000	M 9 901 000 000				
	14			P 0 200 000 000	P 1 100 000 000		
Shift	15			M 9 900 000 000	P 1 000 000 000	M 9 010 000 000	M 9 010 000 000

TABLE 6-13.—INCORRECT PLACEMENT OF RADICAND

Period	Add. Time	Numerator (Radicand) Accumulator		Denominator (Two Root) Accumulator		Shift Accumulator	
		Receives	Stores after receiving	Receives	Stores after receiving	Receives	Stores after receiving
Example C							
I	1	P 2 500 000 000	P 2 500 000 000				
	2						
	3						
	4			P 0 100 000 000	P 0 100 000 000		
II	5	M 9 900 000 000	P 2 400 000 000				
	6			P 0 200 000 000	P 0 300 000 000		
	7	M 9 700 000 000	P 2 100 000 000				
	8			P 0 200 000 000	P 0 500 000 000		
	9	M 9 500 000 000	P 1 600 000 000				
	10			P 0 200 000 000	P 0 700 000 000		
	11	M 9 300 000 000	P 0 900 000 000				
	12			P 0 200 000 000	P 0 900 000 000		
	13	M 0 100 000 000	P 0 000 000 000				
	14			P 0 200 000 000	P 1 100 000 000		
	15	M 8 900 000 000	M 8 900 000 000				
	16			P 0 200 000 000	P 1 300 000 000	M 9 000 000 000	M 9 000 000 000
Shift	17			M 9 900 000 000	P 1 200 000 000		

The wrong answer will result because the significant figure, 8, of the remainder from the radicand (see add. time 15) is thrown away when shifting takes place (see add. time 17).

6.3. *Numerical Circuits*

The numerical circuits comprise the quotient place ring and its associated gates, the L1, −1, +2, and −2 receivers, the pulse gates. All of these circuits are located on the lower right hand corner of the block diagram FIGURE 46.

The quotient place ring causes the ±1 or ±2 which go to make up the quotient or the square root to arrive in the proper decade of the quotient or denominator accumulator. Also this ring causes the division or root process to be terminated when the proper number of places (as determined by the divide-root-place switch, see Section 6.1.3) in the answer have been computed. The ±1 and ±2 receivers open combinations of gates which pass groups (of the 1, 2, 2', 4 or 9 pulses) of pulses which represent the numbers +1, −1, +2, or −2.

The 10 stage place ring in the divider and square rooter serves to route the numerical data for the partial quotient or twice the square root into particular decade lines at particular times. The stages of this ring numbered 10, 1, 2, . . . , 9 on FIG. 46–F correspond respectively to decades 10, 9, . . . , 1 of an accumulator. The place ring neons numbered 10, 9, . . . , 1 on FIG. 44 correspond respectively to stages 10, 1, 2, . . . , 9 of the place ring. It is to be noted that in period II for division or square rooting respectively, ±1 or ±2 units are put into the 10^8 decade place of the answer first. A digit different from zero (or the complement of zero if the quotient is negative) occurs in the 10^9 decade place of the answer only if the divider and square rooter puts in more than 10 pulses before the first shift sequence of period II or, if 10 pulses are put in before the first shift, and carry over from the addition of one or two pulses at the end of round off cause carry over to the 10th decade place. The neon numbered 10 in FIG. 44 never lights.

At the end of a divider and square rooter program this

ring can be cycled only during period II and then, only at the end of the first addition time $(s+1)$ of each shift sequence. The cycling of this ring is accomplished by the $1'P_2$ pulse which is produced when the $1'P_1$ pulse (see Section 6.2.2) is passed through R58 by a signal from the S2 receiver.

While the place ring has been classified as one of the numerical circuits, one of its functions is purely a programming function. Stages 3, 6, 7, 8, and 9 of the ring are connected respectively to gates R72 (3, 6, 7, 8, and 9). The second inputs to these gates are connected respectively to points 4, 7, 8, 9, and 10 of the divide-square root and places switch. Upon the coincidence of a signal from the place ring and the divide-square root places switch, the appropriate gate emits a signal which allows an S pulse to pass through gate R69. The resulting SS pulse terminates period II by flipping the pulse source flip-flop into the abnormal state.

The place ring carries out its numerical functions by its control of the 2 sets of answer output gates R131, and R132. One gate from the group R131 and one from the group R132 is connected to the static output of each stage of the place ring. The second input to these gates comes from a line carrying digit pulses gated through the 1, 2, 2', 4, 9, and 1' pulse gates by the setting of the +1, −1, +2, or −2 receiver.

The routing of digit pulses into the appropriate decades by the place ring has been explained by means of a numerical example in Sections 1.3.6.3, to which the reader is referred.

It is to be noted that in the divider and square rooter as in the high-speed multiplier, standard transmitters have not been used in the answer output circuit. Therefore, the numerical data for the answer must be delivered to the quotient or denominator accumulator via either a digit tray used for no other purpose or else by means of a special cable made for this purpose. No load box is used on this digit tray.

6.4. *Interrelation of the Divider and Square Rooter and Its Associated Accumulators*

6.4.1. *Interconnections for Numerical Data*

FIG. 47 (A and B) shows the interconnections which must be made among the accumulators associated with the divider and square rooter to carry out division or square rooting programs when arguments of 10 or fewer places are involved. Divisions involving arguments with from 10 to 20 places may be handled by interconnecting accumulators 3 and 4 (for 20 digit numerators) and accumulators 5 and 6 (for 20 digit denominators). In this case another digit tray is used to connect the add output terminal of the right hand numerator accumulator to the α input terminal of the right hand shift accumulator and a second additional tray to connect the add output terminal of the right hand shift accumulator to the γ input terminal of the right hand numerator accumulator. If the denominator has more than 10 digits, the add and subtract output terminals of the right hand denominator accumulator are also connected into the latter tray.

It is to be noted that no mention has been made of interconnecting a pair of accumulators to accumulate quotients or two-roots having between 10 and 20 places. The reason for this omission is that the divider and square rooter is incapable of finding such answers in one operation because the place ring has but 10 stages and the answer output terminal but 11 leads (and a ground).

Quotients with between 10 and 19 places can be found by performing 2 division programs serially. With the divide-square root and places switch of the program control used for the first division set at 10, 9 or 10 places (depending on the relative placement of the numerator and denominator in the argument accumulators—see Section 6.4.2) of the answer are found. The round off switch of the first program control should be set to NRO and the argument accumulator clear switches to O. When the first division program is completed, the quotient as thus far obtained is then transmitted from (and cleared out of) the quotient accumulator to the left hand accumulator of a pair external to the divider and square rooter system. The left hand accumulator of this pair should be stimulated to receive this quotient through some input channel, say α. Then the α input terminal of the right hand accumulator should not be connected to the same tray as the A output terminal of the quotient accumulator. Because of the setting of the round off and argument clear switches, the divider and square rooter can then proceed on its second program, the division of the remainder from the numerator by the denominator. The quotient obtained in this way contributes 9 more places of the answer. The number stored in the 10^8 decade place of the quotient accumulator after the second division belongs in the 10^9 decade place of the right hand accumulator and the number stored in the 10^9 decade place of the quotient accumulator belongs in the units decade place of the left hand accumulator. If the numerator and denominator before the first division program have like signs, the remainder from the numerator after the first program and the denominator have unlike signs so that the quotient obtained by the second division program is necessarily negative. Therefore the second quotient must be transmitted to the pair of interconnected accumulators with its sign indication. The second quotient may be properly received in the pair of accumulators if these accumulators receive the second quotient from the quotient accumulator through an input channel different from the one used for receiving the first quotient, say the β input channel and the β input terminals of both the left and right hand accumulators should be connected to the tray to which the A output terminal of the quotient accumulator is connected. Special adaptors and shifters must then be used at the β input terminals of the right and left hand accumulators. The right hand accumulator's β input terminal should have plugged into it a shifter which shifts the data one place to the left. The left hand accumulator's β input terminal should have an adaptor which connects the left hand accumulator's PM input and 10^9, 10^8, . . . , $10'$ decade place input leads to the PM line of the digit tray and which connects the 10^0 decade place input lead to the 10^9 decade place line of the digit tray. If it is known that the numerator and denominator for all division programs will always have like sign and if the first division program is stopped after 9 places instead of 10, then the denominator and the remainder from the numerator again have like sign so that the quotient obtained from the second division is positive. Under such circumstances the second quotient should be so shifted that information from the 10^8 and 10^9 decade leads of the quotient accumulator add output is received in the units and tens decade places of the left hand accumulator and the other digits of the second quotient are received in the right hand accumulator shifted over two places to the left. The connections of the PM lead of the output of the quotient accumulator to the PM and 10^9–10^3 decade place leads of the input to the left hand accumulator may obviously be omitted.

If 9 or 10 decade places of twice the root are found by a given square rooting program, it is possible to find about as many places again of the root (notice, not twice the root) by dividing the remainder from the radicand by twice the root as thus far found. The procedure for obtaining the final answer in a pair of interconnected accumulators external to the divider and square

rooter system of accumulators is similar to that for the case discussed above for division. However, if it is desired to accumulate the root in the pair of interconnected accumulators, twice the root (resulting from the first program) should be multiplied by 0.5 before its reception in the left hand accumulator or, if it is desired to accumulate twice the root in the final accumulator, the quotient (resulting from the second program) should be multiplied by two before its reception by the pair of interconnected accumulators.

6.4.2. *Relationship Between Alignment of the Arguments and the Answer*

The operator must exercise considerable care in the placement of the arguments in the argument accumulators for division or square rooting programs in order to make the most efficient use of the divider and square rooter.

From the fact that the divider and square rooter place ring allows one unit to pass to the 10^8 decade of the two root accumulator at the beginning of a square rooting program, it is obvious that the divider and square rooter proceeds on the assumption that the decimal point of the radicand occurs an even number of places (either right or left) from the PM place of the numerator accumulator. The operator therefore, must align the radicand in the numerator accumulator so that the decimal point of the radicand occurs an even number of places to the right or left of the numerator accumulator's PM position.

A comparison between the square rooting example in Table 6–2 and the examples in Tables 6–12 and 6–13 also points to another consideration concerning the placement of the radicand. Examples A and B show radicands placed so that the correct answer will be obtained. Example C shows a radicand placed in such a way that the divider and square rooter cannot possibly obtain the correct answer. The examples in Tables 6–12 and 6–13 have all been carried through the first addition time of the first shift sequence since the reason for the impossibility of Example C shows up at that time. In Examples A and B (and also in Table 6–2) when the remainder from the radicand is shifted the 9 at the extreme left is thrown away. This 9 (preceded by sign M) is not a significant figure since it is merely the complement of a non-significant zero at the left. In Example C, however, the figure 8 at the far left of the remainder from the radicand is thrown away when shifting takes place. This figure (preceded by sign M), the complement of the digit 1, is a significant figure. Therefore, when the basic square rooting sequence is resumed after the completion of the shift sequence, it will be resumed with an incorrect remainder from the radicand. A significant figure of the remainder from the radicand will be thrown away in the first shift sequence whenever the first two decade places at the extreme left of the radicand accumulator are occupied by the number 25 or any greater number. Therefore, in general, at least one zero should precede the first non zero digit (at the extreme left) of the radicand.

If the radicand's decimal point occurs n (positive to the right; negative to the left) decade places from the PM, the decimal point of twice the root occurs

$$\frac{n}{2}+1$$

places from the PM. For example, in the computation of Table 6–2, if the decimal point is considered to occur between the digits 1 and 3 of the radicand, then n is 4 and the decimal point of twice the root occurs 3 places to the left of the PM or after the digit 8. The rule given above may be derived from considerations arising out of the material in Table 6–1.

From the fact that the divider emits +1 or −1 unit in the 10^8 decade for every repetition of the basic division sequence until the first shift sequence of period I, it can be seen that if the first non-zero digit at the left of the denominator occupies the same decade place of the denominator accumulator as the second (from the left) non-zero digit of the numerator does in the numerator accumulator, then the first (from the left) non-zero digit of the quotient occupies either the first of second decade place to the left of the PM in the quotient accumulator (see Section 6.3). If the standard alignment of the denominator is defined to mean the alignment in which the first non-zero digit of the denominator occurs one decade place further to the right than does the first non-zero numerator digit, then shifting the denominator k places to the left or right of the standard alignment, results in shifting the alignment of the quotient k places to the right or left respectively of the position described above. Since with the standard alignment of the denominator, the first (from the left) non-zero digit of the quotient may occupy the extreme left decade of the quotient accumulator, it follows immediately that the first (from the left) non-zero denominator digit must never occur in a decade place two or more to the right of the decade place of the first (from the left) non-zero digit of the numerator or else the quotient may exceed the capacity of the quotient accumulator.

Another restriction on the placement of the denominator is that the first (from the left) non-zero denominator digit must not occupy the far left decade place of the denominator accumulator. The reason for this restriction is similar to the reason for not placing the first non-zero radicand digit in the extreme left hand decade place of the numerator accumulator (see Table 6–13). If this rule is violated, a significant figure of the remainder from the numerator may be discarded when the first shift sequence of period II occurs.

If the decimal points of the numerator, denominator, and quotient respectively occur n, d, and q places from the PM place (where n, d, and q are positive when counted toward the right from the PM place), then q may be predicted by the following formula:

$$q=n-d+2$$

The following tabulation based on the example in Table 6–2 illustrates this rule.

Numerator	n	Denominator	d	Quotient	q
P 0 209.070 000	4	P 0 2.30 000 000	2	P 0 091.000 000	4
P 0.209 070 000	1	P 0 23.0 000 000	3	P.0 091 000 000	0
P 0.209 070 000	1	P 0 230. 000 000	4	(P.0 091 000 000)X10^{-1}	−1

6.5. *Examples*

The following table gives the setting of the program control switches in the different examples:

	Example 1	Example 2
Numerator receiver switch	α	α
Numerator clear switch	C	C
Denominator receive switch	β	O
Denominator clear switch	C	O
Interlock switch	I	NI
Answer disposal switch	1	1
Round-off switch	RO	RO
Root-divide place switch	D8	R10

6.5.1. *A Division Example*

Addition and pulse time:

	Discussion
0.17	Program pulse arrives at buffers R2, and R133. The output of buffer R2 (1) activates the D_β receiver. The output of buffer R2 (2) activates the N_α receiver. The output of buffer R133 activates the transceiver in the divider. The output of the cathode follower R134 opens the gates R72 (7). Buffer R28 gives a signal through the interlock switch to open the gate R34. The other buffer R17 gives a signal through the root-divide and round-off switch to open gates R22 (2) and (3).
1.1 to 1.10	The numerator and denominator accumulators are receiving the numerator and denominator. (It is assumed that the program pulse which activates the divider is used to cause the transmission of the numerator and denominator from whatever units contain them.)
1.17	A general pulse (gated CPP) passes gate R22 (2) to provide the first division pulse (DP). This DP passes gate R76 to step the program ring to stage B. The output of stage B opens gate R57. During this time the PM static lines from the numerator and denominator to the sign indication circuits are setting up.
2.17	Another DP steps the ring to stage 1 causing gates R83, R51, and R52 to open. A general pulse (GP) passes gate R57 which may or may not step the numerator ring and/or the denominator flip-flop depending upon the signs of the respective quantities.
3.17	A GP passes gate R51 clearing the program ring back to stage A. A GP passes gate R52 setting the flip-flop R41 closing the gates R76 and R77. A DP is passed by gate R83 producing a first P pulse. This P pulse activates the N_α receiver R116 and either the D_A or the Ds receiver R117 (depending upon the signs). Activating the N_α receiver causes gate R133 to open. Say that the signs are alike then the Ds receiver will be set and thus gate R136 opened.
4.17	A DP passes gate R133 and activates the receiver Q_γ. This causes gates R111 and R112 to be opened. A DP passes gate R111 setting the +1 receiver. A GP passes the buffer R136 and resets the N_α and the Ds receivers.
5.1	Gate R137 (8) passes a one pulse (1P) which passes gate R131 (1) to go into the ninth decade of the quotient accumulator.
5.17	A DP passes the buffer R63 to reset the +1 receiver. The Q_γ receiver is reset by a CPP. Assuming there has been no overdraft gate R53 passes a GP to produce the next P pulse. This P pulse sets the N_α and the Ds receivers.
6.17	Same as 4.17.
7.17	Assuming there has been an overdraft the gate R54 passes a GP which sets the N_A and the S_α receiver R138. This causes gates R58, R119, and R80 to be opened.
8.1 to 8.9	The numerator is being transmitted to the shift accumulator.
8.10	A 1'P passes gates R46, R58 and steps the quotient place ring to stage 2. The numerator accumulator clears.
8.17	A CPP passes gate R119 activating the S_A and N_α receivers. The activating of receiver N_α opens the gate R56.
9.17	A GP passes gate R56 to produce a P pulse. This starts an add cycle (since the numerator ring has been stepped). That is, this P pulse activates the N_α and the D_A receiver. Activating the D_A receiver causes gate R137 to be opened.
10.17	As in 4.17 the Q_α receiver is activated and a DP passes gate R137 to set the −1 receiver.
. . . . .	
0.10	A 1'P passes gates R46 and R58 to step the quotient ring to stage 7. The N_α and S_A receivers are set. Gate R72 (7) begins to conduct opening gate R69.
1.17	Gate R56 passes a GP to provide a P pulse which activates the N_α and the Ds receivers.
2.17	A DP passes gate R133 setting the Q_γ receiver. A DP passes gate R136 setting the +1 receiver. Assuming there has been an overdraft gate R112 begins to conduct opening gate R54.
3.17	A DP resets the ±1 receivers. A GP passes gate R54 activating the S_α and the N_A receivers. This pulse from R54 passes R69 to set the pulse source flip-flop R39. Thus, this is the last addition time in which general pulses (GP) and therefore division pulses (DP) are produced. As before the output of the S_α receiver opens gates R119, R58, and R80.
4.10	Gate R46 is now closed so no 1'P is passed.
4.17	CPP's pass gates R119 and R80 to set the S_A and the N receivers and to step the numerator ring, respectively. A CPP passes gate R59 to produce the first IIIP pulse. This IIIP pulse goes through the buffer R66 to step the program ring to stage B. It also passes gate R22 (3) to produce a round-off pulse (ROP).
5.17	An ROP pulse (a IIIP gated by R22 (3)) passes gate R87 to produce a P D or the D receiver R117 (depend- pulse which activates the N_α and D_A receivers. A IIIP pulse passes the buffer R66 to step the program ring to stage 1.
6.1 to 6.9	The denominator is added to the numerator.
6.17	A IIIP pulse steps the program ring to stage 2. The N_α and D_A receivers are not reset since there are no GP's to pass the buffer R136.
7.17	A IIIP steps the program ring to stage 3.
8.17	A IIIP steps the program ring to stage 4.
9.17	A IIIP steps the program ring to stage 5. This opens the gate R88.
10.1 to 10.10	The denominator is added to the numerator for the fifth time. Suppose that this does not produce an overdraft in which case gate R92 remains open.
10.17	An ROP pulse passes gate R88 to reset the N_α and the D_A receivers. A IIIP steps the program ring to stage 6, opening gates R73 and R89.
11.17	An ROP pulse passes gates R89, R92 (assuming there was no overdraft), and gates R128 and R129. The output of R129 sets the Q_γ receiver. The output of R128 is passed by gate R43 (2) or R43 (4) depending upon the signs and sets the +1 or the −1 receiver. A IIIP steps the program ring to stage 7. A CPP passes R73 to reset the pulse source flip-flop.
12.1 to 12.10	+1 or −1 is added into one decade of the quotient accumulator.
12.17	A CPP passes R44 and R22 (2) to produce a DP which resets the +1 or the −1 receiver. A CPP passes R78 to set the flip-flop R94.
. . . . .	
	(Wait for interlock pulse)
0.17	Interlock pulse (program output pulse of some other unit) turns on one of the buffers R38 setting the flip-flop R35.
1.17 (13.17)[1]	A CPP passes R37 and R33 to set the flip-flop R96 and reset R94. Flip-flop R96 causes gate R97 in the transceiver to open.
2.10 (14.10)	The carry-clear gate passes gates R13 (1) and R13 (2) and appears at terminals on the front panel.
2.17 (14.17)	A CPP passes R98 to produce the Cl and Cl' pulses. The Cl' pulse does the following: (1) passes gate R34 to reset R35. (2) passes buffer R102 to clear the program ring. (3) passes buffer R74 to reset the pulse source flip-flop R39. (4) passes buffer R103 to reset the D_γ receiver R104 and the ±1 receivers. The Cl pulse does the following: (1) the flip-flop R41 to reset. (2) resets the denominator flip-flop R106. (3) turns off the inverter R107 clearing the numerator binary ring. A CPP passes gate R127 in the transceiver resetting it and being transmitted. A CPP passes R26 (1) to activate one of the answer disposal transceivers.

[1] Read this time if interlock signal arrives before completion of division process.

6.5.2. *A Square Root Example*

Addition and pulse time :	Discussion
	Program pulse arrives at buffers R2, and R133. The output of buffer R2 (1) activated the N_α receiver, and the output of R133 activates the transceiver in the divider. The output of the cathode follower R134 opens the gate R72 (9). Buffer R28 gives a signal through the interlock switch to open the gate R31. The other buffer R17 gives a signal through the root divide and round-off switch to open gates R22 (3) and R22 (4).
1.1 to 1.10	The radicand accumulator (same as numerator) is receiving the number to be square rooted.
1.17	A GP (a CPP passes by gate R44) passes gate R22 (5) to produce the first square root pulse (SRP). This SRP passes gate R77 to step the program ring to stage B, opening gate R57.
2.17	Another SRP steps the program ring to stage 1 causing gates R51, R52, R84, and R86 to open. A GP passes R57 but has no effect on the denominator flip-flop since the denominator contains the number +00000 00000 at this time. If the radicand were negative the binary ring would be stepped.
3.17	An SRP pulse passes gates R84 and R86 setting the D and the +1 receivers, respectively. A GP passes gate R51 clearing the program ring back to stage A. A GP passes gate R52 setting the flip-flop R41 causing the gates R76 and R77 to close.
4.17	The output of the D_γ receiver passes gate R111, opens gate R53 which allows a GP to be passed producing the first P pulse. This P pulse activates the N and the Ds receivers (since the denominator consists of +1 in a certain decade).
5.1 to 5.10	The +1 in the denominator is subtracted from the radicand.
5.17	A GP resets the N_α and the Ds receivers (from buffer R136). An SRP passes gate R134 to set the D_γ receiver and gate R139 to activate the +2 receiver.
6.1 to 6.10	+2 is added into the denominator giving 3.
6.17	A CPP resets the D_γ and the +2 receivers. Assuming there is no overdraft gate R111 is conducting and thus, R53 passes a GP to produce the next P pulse.
7.17	An SRP activates the D and the +2 receivers. Assuming there is an overdraft this time gate R112 conducts opening gate R54.
8.17	A GP passes gate R54 and sets the S_α and N_A and D_γ receivers, and it passes gate R122 to set the −1 receiver.
9.1 to 9.10	−1 is added to the +5 that was in the denominator accumulator. The radicand is transmitted to the shift accumulator. A $1'P_2$ steps the quotient ring.
9.17	A CPP passes R119 to activate the S_A and the N_α receivers and passes gate R80 to step the numerator ring.
10.1 to 10.10	−1 is again added to the +40 in the denominator accumulator giving +39. The radicand is transmitted back (through a shifter) to the numerator accumulator.
10.17	A GP passes gate R55 to reset the D_γ and the −1 receivers. A GP passes gate R56 to produce another P pulse.
. . . . .	
0.10	A 1'P passes gates R46 and R58 to step the quotient ring to stage 9, causing gate R72 (9) to conduct and, thus, opening gate R69.
0.17	The S_A and N_α receivers are set by a CPP through gate R119. The numerator binary is stepped to minus (a minus radicand).
1.17	A GP passes gate R56 to produce a P pulse. This pulse activates the N_α and the Ds receivers.
2.17	An SRP passes gates R134 and R139 to set the D_γ and the +2 receivers, respectively. Assuming there has been an overdraft gate R54 opens.
3.17	A GP passes gate R54 activating the S_α and the N_A receivers, and passes gate R69 to set the pulse source flip-flop R39. Thus, this is the last addition time in which GP pulse, and therefore, SRP pulse will be produced.
4.0 to 11.0	What happens during these addition times is exactly a repetition of what happens in the case of division (explained in Example 1).

12.17	A CPP passes gates R31 and R33 (opened by the program ring being at stage 7) and sets the flip-flop R96.
13.17	A CPP passes gate R98 producing Cl and Cl′ pulses. The Cl pulse resets the clear flip-flop R96, and clears the quotient ring and the numerator ring. The Cl′ pulse clears the program ring, resets the pulse source flip-flop R39, and resets the D_γ and the +1 and −1 receivers. The Cl pulse resets the flip-flops R41, and R106. The output of the clear flip-flop causes the gate R97 in the activated transceiver to conduct, which in turn opens the gate R13 (4), one of the gates R26 (for answer disposal), and gate R127 in the transceiver.
14.10	The carry-clear gate passes gate R13 (4) and clears the numerator accumulator.
14.17	A CPP passes gate R127 and is transmitted as an output program pulse. A CPP passes gate R24 (1) and activates the first answer disposal receiver.

VII. FUNCTION TABLE

The ENIAC contains three function table units each of which can be used to store values of one or more functions tabulated against an independent variable and can be programmed to look up and transmit the values so stored. The function table is useful not only for storing and selecting values of a function (as the term is ordinarily defined) but also makes it possible to store and have readily available any numerical data which can be tagged with two digit numbers increasing monotonically between 0 and 99. Thus, a function table could be used to store the coefficients and constant terms of a system of simultaneous equations or programmatic information. The function table requires $r+4$ addition times to look up the value of a function and transmit it repetitively r times.

The following pages will be concerned with: program controls (7.1); common programming circuits (7.2); numerical circuits (7.3); and storage of programming information in the function table (7.4). Reference will be made to the following diagrams:

Function Table Block Diagram	FIG. 48.
Function Table Front View	FIG. 49.
Function Table Front Panels	**303**, FIGS. 50, 51.
Portable Function Table—Switch Arrangement	FIG. 52.
Use of Unmodified Function Table to Store Programming Information	FIG. 53.

7.0. *General Summary of the Function Table*

It is assumed that the reader has familiarized himself with the arrangement and operation of the elementary function table, Chapter 1.3.7.

The function table can store 104 entries of one or more functions with each entry associated with an argument between −2 and 101. By an entry is meant 12 digits any one or all of which may vary from entry to entry and two signs, either variable or constant. In addition, 8 digits, constant throughout the range of the table, may be set up manually on switches.

If a is the argument (where $0 \leqslant a \leqslant 99$) and $f(a)$ is the information stored in the function table line corresponding to value a of the argument, the function table can be programmed to look up $f(a-)$, $f(a-1)$, $f(a)$, $f(a+1)$, $f(a+2)$, or the complement of any of the preceding and, furthermore, can be programmed to transmit the number looked up repetitively from one to nine times. Four addition times are required for looking up the value of a function and one more addition time is needed for each transmission of the functional value.

The function table can also exert some program control on the accumulator used to store the argument since it is capable of transmitting a program pulse to stimulate the argument accumulator to transmit the argument to the function table and then either to clear or not clear. In addition, the function table is capable of receiving a pulse

which will stimulate it to carry out the operations noted above and then, of transmitting a program output pulse.

The physical appearance of the function table can be seen in FIG. 49. The function table has the two panels shown here and in addition, a portable function table (see ENIAC Floor Layout, FIG. 1) which extends into the center of the floor. As its name implies, the portable function table can be moved around and any of the tables (A, B, C in FIG. 1) can be used with any one of the function tables. The portable function table will be discussed in greater detail in Sec. 7.3.

In its components and method of operation the function table is very much like the high-speed multiplier. The numerical circuits consist of a portable function table (analogous to the multiplication tables), argument counters (tens and units argument rings, FIG. 48–A), argument input gates (analogous to the ier selector gates and labelled "Table Input Gates" in FIG. 48–A) table output gates FIG. 48–A (analogous to the coding gates in the high-speed multiplier), and the 1, 2, 2', 4, and 9P gates (labelled "Pulse Gates" in FIG. 48–B), all similar in function to those shown in FIG. 21 in connection with the elementary function table.

There is a difference, however, between the high-speed multiplier and the function table in the way in which the argument is fed to the function table. Here, the argument is delivered in pulse form (rather than in the form of static outputs) to the function table where it is set up in the argument counters (a decade ring counter for units place with carry-over to the 11 stage counter used for tens place of the argument). The argument input gates are then set up by the static outputs of the argument counters in the function table.

The function table's numerical circuits also include 8 constant digit switches (FIG. 48–D) which have a purpose similar to that of the table output gates except that the former are used only for digits which remain the same throughout the table. A sign which remains constant over the whole table can be set up on one of the two master PM switches (FIG. 48–D). The subtract pulse switches make it possible to transmit the 1'P over the leads for certain places when the function table transmits substractively so that complements with respect to 10 can be emitted.

The common programming circuits of the function table consist of a 13 stage program ring analogous to the program ring in the high-speed multiplier, the argument correct gates **F1** which make it possible to look up $f(a-2)$, $f(a-1)$, $f(a)$, $f(a+1)$, $f(a+1)$, $f(a+2)$, the add and subtract gates and the add and subtract flip-flops they control which make it possible for either the function or its complement to be looked up, and the argument flip-flop which controls the setting up of tens place of the argument in the argument selectors. There are also circuits for clearing the program ring and the argument counters, and for resetting flip-flops. The C and NC transmitters and their output terminals on front panel **1** (FIG. 50) which can deliver a pulse to the argument accumulators to stimulate transmission of the argument may also be counted among the common programming circuits.

The programming circuits mentioned above can be operated by any one of the function table's eleven program controls (FIG. 48–B). Each program control includes a transceiver with program pulse input and output terminals on front panel **1** correlated with an operation switch, an argument clear switch, and a repeat switch.

The $r+4$ addition times required for the looking up of a function and its repetitive transmission r times are spent in the following way:

0 Program input pulse is received.
1 Function table emits C or NC program output pulse to stimulate transmission of argument.
2 Function table receives digit pulses for the argument.
3 Argument stored in the argument counters of the function table is corrected to the value specified on the operation switch.
4 Appropriate line of the portable function table is activated.
5 Functional value is transmitted for the first time.
$4+r$ Functional value is transmitted for the r^{th} time and a program output pulse is emitted after the r^{th} transmission.

7.1. *Program Controls*

The eleven transceivers **F2** are located in the No. 1 panel of the function table, and are of standard design.

A pulse received at one of the 11 program input terminals of the function table transceivers stimulates the function table to carry out the program set up on the program switches of the control of which that input terminal is a part. Each program control offers the operator options as to:

(1) Which of five "lines" of the table is to be entered for a given value of the argument,
(2) Whether the entry tabulated on the specified line or its complement is to be looked up and transmitted,
(3) Whether or not transmission of the argument to the function table is to be stimulated by the function table,
(4) The number of times (from 1 to 9) in succession the function table is to transmit the value looked up.

The function table follows the program instructions set-up on the control in a fashion similar to that discussed previously (see accumulator and high-speed multiplier, for example). A pulse received at an input terminal flips the flip-flop **F3** of the transceiver into the abnormal state. As a result, signals from the transceiver (indirectly through inverters and/or buffers) pass through the program switches shown in FIG. 48–B directly above the transceivers and then proceed to cause the common programming circuits (see Sec. 7.2) to operate appropriately. As in units previously discussed, also, the reset signal for the transceiver's flip-flop comes from the unit's program ring on line **F4** and passes through the repeat switch of the control. After the function has been transmitted the number of times indicated by the setting of the repeat switch, the flip-flop is reset and a program output pulse is transmitted.

It is to be noted that the program output pulse is emitted after the function is transmitted. Therefore, the output pulse cannot be used to stimulate an accumulator to receive the function, but a pulse from some other source must be provided for this purpose four addition times after a function table transceiver is stimulated.

Program neons on front panel 1 (see FIG. 49) each correlated with a program control enable the observer to see which program control has been stimulated at a given time and, hence, which program should be in operation.

7.1.1. *The Argument Switch (F6)*

The argument switch has ten possible positions. The five left hand (add) positions are used when it is desired to transmit the value tabulated on a certain line; the five right hand (subtract) positions specify transmission of the complement. If a is the argument received in the function table (where $0 \leqslant a \leqslant 99$), the setting -2, -1, . . . , or 2 respectively specifies that line $a-2$, $a-1$, . . . , or $a+2$ of the portable function table is to be entered.

The function table is especially well adapted to interpolation by means of algebraic interpolation polynomials of degree 1, 2, 3, or 4 since, by setting up several program controls, the operator can readily produce functional values for values of the argument surrounding the one for which the interpolation is being carried out. Inter-

polation of degree higher than the fourth can also be done. However, in order to obtain several of the entries required for such higher degree interpolation, the argument must be changed before its transmission to the function table. For example, to interpolate by means of the Newton Gregory forward interpolation formula out to sixth differences requires $f(a)$, $f(a+1)$, . . . , $f(a+6)$. The entries $f(a)$, $f(a+1)$, $f(a+2)$ can be obtained in succession by using three program controls with operation switches set at 0, 1, 2, and by feeding a to the function table. The remaining entries may be produced by forming $a'=a+5$ in the accumulator in which the argument is stored and then using program controls set-up to produce $f(a'-2)$, $f(a'-1)$, . . . , $f(a'+1)$.

Deck 1 of the argument switch determines whether plus or minus the functional value is to be transmitted. When set on A (add), and a program control is activated, the output of tube F7' in the transceiver causes the inverter F8 to stop conducting, opening the gate F9. When the ring is in stage zero this gate passes a pulse which sets the add flip-flop F11. If the program switch is on S, then inverter F12 (the other triode) stops conducting, opening gate F13. Then, when the ring is on stage zero the subtract flip-flop F14 is set. The timing of these operations is illustrated in Section 7.2.1.

Deck 2 of the argument switch F6 determines whether the functional value itself or one of the four neighboring values is to be transmitted. If the reader will check the connections from the argument rings to the switches of the table he will note that the table number is exactly two less than the number registered in the argument rings. Thus, if x denotes the argument then normally the function table would transmit $f(x-2)$. The number transmitted and the corresponding setting of the program switch is as follows:

Program switch setting	Number transmitted	Number in argument rings
−2	f(x−2)	x
−1	f(x−1)	x+1
0	f(x)	x+2
+1	f(x+1)	x+3
+2	f(x+2)	x+4

If the program switch is set at +1, for example, gates F1 (1P and 2'P) will be opened by the output of the buffer F7 of the transceiver. When the program ring is at stage −1 gate F16 will be opened and three pulses will pass F1 (1P and 2'P) through the inverter F17 and gate F16 and into the units argument ring. This changes the argument from x to $x+3$ and the function table will now transmit $f(x+1)$. Note that stage −1 of the program ring must open gate F16 in time to pass a 1P. Since the gate is physically close to the ring there is no difficulty in doing this with the usual two to one safety factor.

7.1.2. *Argument Clear Switch*

The argument clear switch can be set at C, NC, or O. If, on a given program control, the switch is set at C or NC, at the end of the first addition time, a program output pulse is transmitted from the correspondingly labelled terminal on front panel 1 (see FIG. 50). If the argument clear switch is set at O, no pulse is transmitted from either the C or NC program pulse output terminals.

The operator can utilize the C or NC pulse to stimulate transmission of the argument to the function table by connecting the C and NC terminals to suitably set up program controls on the argument accumulator or accumulators. If the argument for a given function table is always stored in one accumulator, the C terminal can be connected to a program control on the argument accumulator set up for transmission with clearing and the NC terminal, to a program control set-up for transmission without clearing. If, on the other hand, the argument for a given function table is stored sometimes in one accumulator and sometimes in another, the operator may find it convenient to use the C pulse to stimulate transmission of the argument from one accumulator and the NC pulse to stimulate transmission from the other argument accumulator.

When the argument clear switch is set at O, the operator must provide, independently, for a program pulse to stimulate the transmission of the argument to the function table (unless the argument is to be zero). Such a pulse must be delivered to the argument accumulator one addition time after the program pulse which stimulates the function table program control since the argument must be received in the function table during the second addition time of a program.

The buffer which feeds switch F18 (that is, the cathode follower in the transceiver) serves two functions, namely, to control the transmission of the argument and the stepping of the program ring. The argument clear switch has three possible settings controlling the reception of the argument from some other unit of the ENIAC. On all three settings the fast buffer output F18 of a transceiver goes to gates F21, F22, or F23, one of which passes central program pulses which step the program ring. If the switch of the activated program control circuit is set on NC, a central program pulse passed by gate F24 (opened by stage −3 of the program ring so that F24 is open at the beginning of the program) will turn its inverter off, and pass gate F26. The pulse will then go through the transmitter F27, and appear on the front panel (terminal labeled NC, see FIG. 50). From there it can be taken (via jumpers and program trays) to some other unit of the ENIAC to program the argument transmission. If the switch were set at C the action would be similar except the output pulse would pass gate F28 and be transmitted from the transmitter F29. Supposedly, the NC circuit would be used when the argument is not to be cleared in the transmitting accumulator, and C is to be used when it is to be cleared.

These circuits are controlled by the fast buffer outputs F18 of the transceivers. Since these outputs have a small time constant the input circuits to the gate tubes have extra capacity purposely added. This delays the opening of these gates; keeping them from opening in time to pass part of the same CPP which activated the transceiver.

7.1.3. *The Repeat Switch (F31)*

This switch determines how many times the functional value is transmitted. If it is set at 3 (as illustrated) the functional value will be transmitted once when the ring F32 is set at stage one, again at stage two, and the third time at stage three. The output of stage three (which is now positive) will go through terminal three on the repeat switch and open gate F33 in the transceiver. This causes the inverter F34 to go off and opens gate F36 giving an output program pulse at the end of this addition time. The output of the buffer F37 turns off the inverter F38 opening gates F39, F41, and F42. These pass central program pulses (CPP) which clear all three rings and reset all three flip-flops.

Thus, the functional table will transmit a functional value n times in $n+4$ addition times where n is any number between one and nine. Note that the accumulator which is to receive the function must be programmed to receive during either the whole $n+4$ addition times, or during the last n of the $n+4$. Consequently, if it is programmed simultaneously with the function table, it can receive the function only 5 times using a single transceiver. If, however, it can be programmed 4 addition times later than the function table, the setting of its repeat switch can be the same as that of the function table, and the function table can transmit to it the full 9 times.

7.2. *Common Programming Circuits*

7.2.1. *The Program Ring*

The device used to clock the advance of the function table through the sequence of suboperations involved in looking up and transmitting a functional value is the program ring counter **F32** (usually abbreviated as the program ring). This is a thirteen stage counter with the first stage labelled −3 (see FIG. 48) and the last 9. The program ring neons (shown in FIG. 49) are correlated with the 13 stages of the program ring.

The program ring clears to stage −3 when initial clearing takes place and whenever a function table program is completed. The reception of a program pulse by any transceiver results in opening a gate (**F21, 22, or 23**) which allows the ring to receive a CPP each addition time as long as the transceiver's flip-flop remains in the abnormal state. Each CPP then cycles the ring 1 stage. In this section, the program ring and its effect on associated gates and flip-flops are discussed (see Table 7–1 for a summary).

Addition Time	Ring Stage	Effect
0	−3	Program pulse is received at a transceiver.
1	−3	At pulse time seventeen of this addition time the ring steps to stage −2, and (depending upon the setting of the argument reception), a pulse may be transmitted by F27 or F29. Usually the pulse transmitted here will be used to program the argument transmission from some other unit of the ENIAC.
2	−2	The buffer F43 will go on turning the inverter F44 off, opening the gates F46 and F47; allowing the argument to be received.
3	−1	Depending upon the setting of the argument switch certain of the gates F1 may have been opened. Thus, from zero to four pulses are passing the inverter F17 and at this addition time these pass the gate F16 and enter the units argument ring. Gate F48 is also opened, allowing a 1′ pulse to set flip-flop F49; this flip-flop, through buffer F51, turns off inverters F52; this in turn permits one of the table input gates to conduct and energize one entry of table.
4	0	The output of the zero stage opens the gate F53. At pulse time seventeen of this addition time a central program pulse (CPP) passes this gate, turning off the inverter F54. Depending upon the setting of the program switch, either gate F13 or F9 is open. Thus, the output of the inverter F54 sets either the add or the subtract flip-flop causing either the function value or minus the functional value to be transmitted during addition-time 5 (and subsequent addition times for repeat switch settings above 1).
5	1	Certain of the pulse gates F56 are opened during this addition time to pass 1, 2, 2′, 4 and/or 9P, and the functional value is transmitted over the digit output (SX and SY in Fig. 48–D). The output of stage 1 of the program ring connects to terminal 1 on all the repeat switches.
6	2	The functional value is transmitted a second time.
7	3	The functional value is transmitted for the third time, and (if the repeat switch is set on three as illustrated) gate F33 is opened in the transceiver. Then buffer F37 turns off inverter F38 opening gates F39, F41, and F42, causing the rings to clear and the flip-flops to be reset.

7.2.2. *The Argument Flip-Flop*

The argument flip-flop **F49** is set by a 1′ pulse passing gate **F48**. This gate is opened when the program ring is at stage −1. When the flip-flop is set it turns on buffer **F51** which turns off the inverters **F52**. This determines the time at which one of the table input gates conducts.

7.2.3. *The Add and Subtract Flip-Flops and the Pulse Gates*

Inspection of the pulse gates **F56** will show that the connections are such that when "Add" line **F57** is energized, the respective digit channels **F59** will, during the next addition time, each pass a number of pulses corresponding to its digit number; and when the "subtract" line **F58** is energized, each digit channel will pass the nines complement of its digit number.

The outputs of the pulse gates go to transmitting circuits **F61**. The outputs of these transmitting circuits go on line **F60** to the various table output gates, the zero–nine channels go on lines **F65** to the P and M terminals on the PM master switches; and through buffers **F62** they also all go to various terminals on the constant switches.

7.2.4. *Use of the Function Table for Programming*

The function table can be used to obtain program pulses on any of as many as 14 channels when a particular program control circuit is excited. The choice of output channel is controlled by any two digits of the number used as an argument, and registered in the argument accumulator.

To accomplish this, an adapter may be used in back of the function table on the cycling unit trunk. This adapter, whose construction will be obvious, will be connected so as to add a central program pulse to the 9P lines of the function table panel #2.

Now, suppose that all the switches, on the portable function table, for a particular argument are set to one; with the exception of one switch, which is set to "nine." Whenever the function table is programmed and the appropriate argument is stored in the argument accumulator a CPP will be transmitted over the channel corresponding to the switch which was set to "nine."

The nine pulse lines are used for this purpose since they also feed the PM switches. Consequently, the portable table can be used to give output pulses on any of fourteen channels (that is, twelve digit channels and two PM channels).

7.2.5. *Initial Clear*

The initial clear gate opens gates **F39, 41** and **42**. The output of **F42** resets the argument flip-flop (**F49**) and the add and subtract flip-flops (**F11** and **F14**). Gates **F39** and **F41** operate in parallel to turn off inverters **F63** and **F64**. Inverters **F63** cause the argument rings to clear. **F64** causes the program ring to clear.

If the buffer **F37** in any transceiver conducts (as it will at the end of an operation for which its program control was activated), the inverter **F38** stops conducting, opening the gates **F39, 40** and **41**, giving the same effect as the initial clear gate.

7.3. *The Numerical Circuits*

7.3.1. *The Argument Rings*

When the gates **F46** and **F47** are opened (at stage −2 of the program ring) the two digits of the argument arrive over the connected two channels of the input terminal and going through the pulse standardizers (**F67** and **F68**) step the units and tens rings to the proper position. When the program ring reaches stage −1, zero to four pulses may be passed by one of the gates **F1** to step the units ring the corresponding number of positions. If this causes the units ring to step through step nine gate **F69** will be opened to pass the carry over pulse. This pulse goes through an inverter and buffer and steps the tens ring one place. Note that the tens ring has eleven stages; also there is never any delayed carry-over problem. The argument will never exceed nine in the tens place but the carry over may give ten, thus, the extra stage.

Consider the control of the table selectors by the rings. After clearing (as illustrated) the rings each set at stage zero. This causes the inverters **F71** (0) and **F72** (0) to be non-conducting and they are so shown in FIG. 48–A. Suppose that a program control is activated, and the argument is zero. Then when the argument flip-flop is set the inverter **F52** (0) is turned off, raising the potential of both grids of the table input gate (or table selector) **F73**. Incidentally, one control grid of several other table input gates will swing positively at this time (for example, gates **F74, F76,** etc.), but since the other grid remains below cut-off (because other inverters associated with the tens ring remain on), the tubes do not conduct. A similar statement is true for all nine gates **F77**, other than gate **F73**.

Thus, when the program ring is at stage −1, one of the

table input gates begins to conduct and one of the horizontal buses of the portable table has a negative swing of potential.

The action of these inverters and gates is explained in some detail in Sections 1.2.7 and 1.3.10.

During the second addition time, as explained above, the argument is received in the function table's argument counters through the argument input terminal on front panel 1. This terminal is so wired that units and tens place of the argument must be received in the function table on the leads for the decade places 1 and 2 respectively. This may be provided for by placing a shifter at the argument input terminal if arguments delivered to the function table will always require shifting the same number of places or, if at various times there will be different shifting requirements, by placing shifters at the argument accumulator's digit input terminals. The units and tens argument neons on front panel 1 are correlated with the stages of the argument counters as indicated in FIG. 49.

In the third addition time, the argument stored in the argument counters is corrected by from 0 to 4 pulses chosen from the 1, 2, and 2' pulses in accordance with the operation switch setting. The argument counters are so connected to the argument or table input gates that if x is the number registered in the argument counters, the table input gate for argument $x-2$ sets up (during the set up period from the middle of the third addition time through the fourth). Therefore, if the operation switch is set at -2 no correction pulses are added to the argument counters; if the operation switch is set at -1, one pulse is added to the number set up in the argument counters, etc.

7.3.2. *The Table Input Gates*

There are 104 table input gates corresponding to the argument values of -2, -1, 0, 1, 2, . . . , 100, and 101. This gives a range of argument values of 0, 1, . . . , 99 with the extra values on each end for purposes of interpolation. Of the two control grids of each table input gate tube, one connects to the output of an inverter F72 controlled by the proper stage of the units ring, and the other control grid connects to the outputs of two inverters; one (F71) controlled by the tens ring, and the other (F52) by the argument flip-flop. In order for any particular gate tube to conduct all three inverters must be non-conducting. Thus, even though the argument arrives in the rings earlier, none of the table input gates conduct until the argument flip-flop F49 is set at stage -1 of the program ring. Note that this flip-flop is set by a one primed pulse (1'P). The timing here is illustrated by Table 7–2.

TABLE 7-2

Addition Time	Pulse Time	Activity
0	17	Programming pulse arrives at the function table.
1	17	Argument transmission is programmed and receiving gates (F46, 47) are opened.
2	17	Program ring steps to stage -1 opening gates F16 and F48.
3	1 to 5	Argument adjustment takes place by 0, 1, 2, 3, or 4 pulses passing gate F16.
	10	Argument flip-flop is set by 1'P.
	17	Program ring steps to stage 0 opening gate F53
4	17	Program ring steps to stage 1 opening gate F33 in the transceiver (provided the repeat switch is at one) and a central program pulse passes gate F53 to set the add or the subtract flip-flop.
5	1 to 10	Functional value is transmitted.
	17	Central program pulse passes gate F36 in the transceiver to be transmitted and to reset flip-flop. CPP also passes gates F39, F41 and F42 to clear rings and reset flip-flops.

7.3.3. *The Portable Table*

The portable table is a switching network built as a separate unit, and connects to the function table unit through two large multi-connector type plugs. Since the portable table is on wheels, the operator may quickly interchange it with one connected to any other function table.

Each portable table mounts 208 PM (sign) indication switches (two for each argument value) and 1248 digit switches (12 for each argument value). There are 104 PM switches and 624 digit switches on each side of the portable table.

7.3.4. *Table Output Gates*

The nine terminal on each of the 104 switches in the sixth column of the portable table connects to the inverter F77 (9). The output of this inverter goes to the gate F78 (9), which when opened will pass either nine or zero (no) pulses depending on whether the associated program control is on add, or subtract program respectively.

The ten positions of the switches in each column go to ten such inverters. Each output from the ten inverters goes to one grid of ten gates, the other grids being fed by the pulse gates.

Thus, if horizontal bus 11 (FIGS. 48–A and C) is energized and the sixth column digit switch is at 7 (as illustrated) the inverter F77 (7) will cease conducting and the gate F78 (7) will open. This gate will then pass 7 or 2 pulses depending upon the setting of the argument switch of the associated program control circuit.

There are 120 inverters and 120 output gates on the digit channels. The two PM channels feed four more inverters and gates F79.

The outputs of the digit gates go through respective digit lines A5 to A10 and B5 to B10 to inverters, buffers and transmitters (F81), F82 and F83 respectively), and then to terminals SX and SY. The outputs of the PM gates go to the PM master switches (PM_1 and PM_2 associated with the A and the B outputs respectively).

7.3.5. *The PM Master Switches*

The PM master switches make it possible to determine the sign for all the table entries at once instead of setting the individual PM switches on the portable function tables. This is useful only if all entries are of the same sign.

There is a PM master switch associated with each output (SX and SY). These switches determine the sign indication transmitted on the channel of the respective outputs. Each switch has three settings, Table, P and M. The following table gives results of various settings of these switches.

Master switch setting	Pulses transmitted over the PM channel	
	Add flip-flop set	Subtract flip-flop set
P	0	9
M	9	0
Table	0 or 9 depending upon the setting of the corresponding PM switch on the portable table.	

With a master PM switch set at P or M (instead of table) the sign pulses emitted by one of the table output gates for sign cannot reach the output circuit. The transmission of a constant sign set up on one of the master PM switches takes place in the following manner: The same number of pulses are delivered to the points P and M respectively on the master PM switches as are delivered to the table output gates associated with digits 0 and 9. Thus, if a master PM switch is set at P, zero or nine pulses are passed through this switch to the associated function output terminal's PM lead according as additive or subtractive transmission takes place. The case where a master PM switch is set at M is taken care of similarly.

7.3.6. *The Constant Switches and the Delete Switches*

There are eight constant digit switches, four associated with each of the outputs SX and SY (see FIG. 48–D). If the first few digits of a function are the same for all arguments used, these switches simplify the procedure for setting up the values of the function. Therefore, when some program control is activated the numbers set on these constant switches (or complements) will be transmitted over the corresponding channels regardless of the value of the argument.

The outputs of the transmitters associated with the pulse gates comes through buffers F62 to ten of the positions on each of these switches. Two other terminals on each of these switches make available the outputs of the two PM master switches here. This is to help provide the proper complements.

The delete switches are provided on each of these channels in case the operator desires to transmit nothing on one or more channels.

7.3.7. *The Subtract Pulse Switches*

Since the complementation provided by the add or subtract flip-flops and pulse gates gives complements with respect to 10^n-1, it is necessary to provide a correction pulse to get complements with respect to 10^n. The correct pulse switches enable the operator to provide this correction pulse in any of six channels on each output, namely, digit output lines A5 to A10 and B5 to B10.

The output of the subtract flip-flop F14 goes through the S inverter to the gates F84. The 1'P is passed by these gates through the inverter F86 to the buffers F87.

These subtract pulse switches enable the operator to divide the 12 variable digits set up on the portable table into arbitrary groups and cause each group to give complements with respect to 10^n.

7.3.8. *The Output Transmitters*

The outputs of the constant switches go through the delete switches directly to transmitters F83. The outputs of the table output gates go through an inverter and a buffer to transmitters F83. Special adapters can be easily built to rearrange the outputs and allow transmission onto a single digit trunk.

If the operator desires, for example, to set up a ten digit function on the table and his function is such that the constant switches cannot be used then six of the digits can be obtained from channels A5 to A10. The other four must come from four of the channels B5 to B10 and a special adapter must be used to get these ten digits onto one digit trunk.

7.3.9. *Adapters*

In designing an adapter for use on the function table outputs there are two points to watch. First, the function table outputs (which are to be used) are connected in a one-to-one manner to terminals corresponding to the trunk lines to be used. Secondly, if negative numbers are to be transmitted, then any unused lines, corresponding to accumulator decades between the PM unit and the first decade used, must carry 9 pulses in order to give the proper complements. This second objective can be accomplished by connecting the outputs of some of the master digit switches (A, to A4 or B, to B4) to the corresponding lines. The PM_1 and PM_2 positions of the master switches provides 9 pulses at the proper times.

If for any reason the master digit switches cannot be used for this purpose the adapter can be made to transmit the number onto the trunk using only channels adjacent to the PM line (line 11). In this case a shifter can be used on the input to the accumulator. The shifter provides for the extra "nines" needed for complementing purposes.

7.3.10. *Flexibility*

The function table permits great flexibility in the way in which it is set up and used. One sign and as many as 20 digits may sometimes be used for a single function. The 2 PM's, one with k and the other with $20-k$ (where $0 \leq k \leq 20$) digits, can be used for 2 functions. as a matter of fact, more than 2 signed functions can be stored by setting up numbers zero and nine for sign indication P and M respectively on switches ordinarily used for digits provided that these switches are not required for digits. Of course, in cases where the digits for a single function are transmitted through both function output terminals, it may be necessary to use adaptors, shifters and/or deleters in order to receive the functional value properly lined up in another unit.

The portable function table is arranged with 26 rows and 28 columns of switches on each of its 2 faces. Each face, thus, has the switches for 52 entries with the 14 columns of switches for 26 entries appearing on the left half of the face and those for the succeeding 26 entries on the right half. The sign and 6 digits set up on the first 7 switches (at the left) are emitted over terminal A; the next 6 digits and sign, over terminal B (see Table 7–3). Positive functional values are set up with sign P and the digits for the absolute value of the function. Negative values are set up as complements, i.e., with sign M and the digits for the absolute value subtracted from some power of 10.

The adjective "variable" is used to describe the type of function table discussed above in which the values of the function are set up manually on switches and which, with changed switch settings, can be used for storing different functions on different occasions. At present, one variable type is used with each function table unit. As the need arises, portable function tables of the fixed type in which the pattern of connections is permanently wired can be constructed and used in place of the fixed type. Such a permanent table would have the advantages of always being available for use without the necessity for tearing down a function already set up on switches, of being less expensive to build, and of being considerably smaller in size than the variable type.

Master PM switches 1 and 2 on panel 2 (see FIG. 51) of the function table are associated with the PM leads of terminals A and B respectively. These switches have the positions P, M, and Table. If the sign to be emitted over one of the terminals is constant throughout the range of the table, this constant sign may be set up on the associated master PM switch instead of on the 104 PM switches of the portable function table. For a sign varying from entry to entry however, the appropriate sign is tabulated in the PM column of the portable function table with each entry and the corresponding master PM switch is set at Table.

For each of the 8 decade places which can be filled with a constant digit, there is a digit delete switch with the positions "delete" and "on" and an associated constant digit switch with the positions 0, 1, . . ., 9, PM_1, and PM_2. (See Table 7–3 for the decade place leads associated with these switches.)

With a digit delete switch set at delete, no pulses are transmitted over the decade place lead associated with the delete switch. With a delete switch set at on and the associated digit switch at d (where $0 \leq d \leq 9$), d or $9-d$ pulses are transmitted over the correlated decade place lead according as additive or subtractive transmission respectively takes place. With a digit delete switch set at "on" and the associated constant digit switch set at PM_1 or PM_2 the sign pulses emitted respectively over the sign lead of the A or B function output terminals are duplicated on the correlated decade place lead. This is true whether the pulses emitted over the sign lead are those specified on a portable function table PM switch or on the master PM switch.

TABLE 7-3.—FUNCTION OUTPUT TERMINAL LEADS AND ASSOCIATED SWITCHES

Lead	Associated Switches for Terminal A			Associated Switches for Terminal B		
PM	Master PM Switch 1 and Portable Function Table Switch in Column 1			Master PM Switch 2 and Portable Function Table Switch in Column 14		
10	Constant Digit and Digit Delete Switches		A4	Constant Digit and Digit Delete Switches		B4
9	Constant Digit and Digit Delete Switches		A3	Constant Digit and Digit Delete Switches		B3
8	Constant Digit and Digit Delete Switches		A2	Constant Digit and Digit Delete Switches		B2
7	Constant Digit and Digit Delete Switches		A1	Constant Digit and Digit Delete Switches		B1
6	Portable Function Table Switch in Column 2.	Subtract Pulse Switch	A10	Portable Function Table Switch in Column 8.	Subtract Pulse Switch	B10
5	Portable Function Table Switch in Column 3.	Subtract Pulse Switch	A9	Portable Function Table Switch in Column 9.	Subtract Pulse Switch	B9
4	Portable Function Table Switch in Column 4.	Subtract Pulse Switch	A8	Portable Function Table Switch in Column 10.	Subtract Pulse Switch	B8
3	Portable Function Table Switch in Column 5.	Subtract Pulse Switch	A7	Portable Function Table Switch in Column 11.	Subtract Pulse Switch	B7
2	Portable Function Table Switch in Column 6.	Subtract Pulse Switch	A6	Portable Function Table Switch in Column 12.	Subtract Pulse Switch	B6
1	Portable Function Table Switch in Column 7.	Subtract Pulse Switch	A5	Portable Function Table Switch in Column 13.	Subtract Pulse Switch	B5

When the function output of a terminal is to be received in an accumulator with the variable digits in decade places at the right and with no other information provided for b (where $1 \leqslant b \leqslant 4$) decade places at the left (such as constant digits or digits from another function output terminals), and when some or all function values emitted may be negative, the PM_1 or PM_2 setting of b of the constant digit switch provides a means of filling these decade places at the left with the nines needed to represent a negative number. If all entries associated with a function output terminal are tabulated as either positive or negative numbers (i.e., with the master PM switch set at P or M), the same end may be achieved by setting b constant digit switches at 0 or at 9 respectively. (See Table 7–4 which follows the discussion of the subtract pulse switches.)

The digit delete switch correlated with a decade place lead is set at delete when it is desired to leave a decade place completely blank as is required, for example, if a variable digit from another function output terminal is to be inserted in that place.

The subtract pulse switches A and B5–10 have the positions 0 and S. If a subtract pulse switch is set at S when subtractive transmission takes place (see Sec. 7.3.7), the 1'P is emitted over the decade place lead associated with the switch (see Table 7–3) to make a 10's instead of a 9's complement. Complements with respect to 9 are emitted in the decade place leads associated with subtract pulse switches which are set at 0. In the usual applications of the function table, at most one of the A and/or one of the B subtract pulse switches would be set at S. There is, however, nothing in the design of this unit to preclude setting a greater number of these switches at S if the operator so desires.

TABLE 7-4.—ILLUSTRATIONS OF THE USE OF SWITCHES ON PANEL 2 OF THE FUNCTION TABLE

Line	Setting of Portable Function Table Switches
x	P123 000 795 642 M
x+1	M 764 000 421 508 M

EXAMPLE 1

Setting of Constant Digit Switches (All Digit Delete Switches set at "On."):

A4 at PM^1 B4 at PM^2
A3 at PM^1 B3 at PM^2
A2 at PM^1 B2 at PM^2
A1 at 3 B1 at PM^2

Subtract Pulse Switches: A8 at S B5 at S (all others at 0).

Transmit	For Argument	Number Emitted	
		Over Terminal A	Over Terminal B
Add	x	P 0 003 123 000	M 9 999 795 642
Add	x+1	M 9 993 764 000	M 9 999 421 508
Sub	x	M 9 996 877 999	P 0 000 204 358
Sub	x+1	P 0 006 236 999	P 0 000 578 492

EXAMPLE 2

Setting of Constant Digit Switches:

A3 at 0 B4 at 9
A2 at 0 B3 at 9
A1 at 0 B2 at 9
B1 at 9

Digit Delete Switch A4 set at "Delete" (all others set at "On"). All Subtract Pulse Switches set at 0.

Transmit	For Argument	Number Emitted	
		Over Terminal A	Over Terminal B
Add	x	P 0 000 123 000	M 9 999 795 642
Add	x+1	M 0 000 764 000	M 9 999 421 508
Sub	x	M 0 999 876 999	P 0 000 204 357
Sub	x+1	P 0 999 235 999	P 0 000 578 491

7.4. *Storage of Programming Data by Means of the Function Table*

When only a part of a total function table storage capacity (3744 variable digits and 624 variable signs for the 3 function tables) is required for the tabulation of numerical data, the remaining storage capacity can be used as memory for programming instructions. This can be done either with a function table operating in the same way as described in Sec. 7.3 when numerical functions are stored and transmitted or, more conveniently, with a small change in the circuits containing the 1, 2, 2', 4, and 9P gates.

First, let us consider the use of the unmodified function table for programming memory. Suppose there are, say, 14 different programs (P_1–P_{14}) one or more of which are to be stimulated at various times in a computation. We could then assign one column on a portable function table to each of the 14 programs and assign one line of the portable function table to each occasion on which it is necessary to make a choice as to which of the 14 programs is or are to be stimulated. Then the switches on a given line of the portable function table are set at P or 0 in the columns corresponding to programs which are not to be stimulated and at M or a number different from zero in the columns corresponding to programs which are to be stimulated. An accumulator is set aside to store the argument for the function table.

Now, when choice of program is required, a program pulse is sent to a function table program control set up for additive transmission. In the fifth addition time following the program input pulse, digit pulses are emitted over function output terminals in the decade place leads corresponding to switch settings different from P or zero. At the end of the fifth addition time a program output pulse is emitted. The digit pulses are taken through adapters at the function output terminals to lines in program trays and then to dummy programs for conversion to program pulses. The program output pulses of the dummy programs are taken to the program controls on which are set

up those of the 14 programs which are to be stimulated (see FIG. 53). The function table's program output pulse can be taken to a program control of the accumulator containing the argument which is set-up for a "receive-C" program in order to increase the value of the argument by one.

In the example shown on FIG. 53, all 14 columns of switches on a program table are devoted to the storage of programming information. With the function table in its unmodified form, however, there is no reason why some of the columns cannot be used for numerical data and others for programming data.

The disadvantage inherent in using the function table in its unmodified form to store programming information is the necessity for expending dummy programs to convert the digit pulses emitted from the function output terminals into program pulses (see Sec. 4.5.1). With only a small amount of labor the function table can be adapted so that program pulses are transmitted from the function output terminals instead of digit pulses. The simplest way to make this change is to disconnect the 9P gates (F88 and F89) from the line in the synchronizing trunk which carries the 9P and to connect these gates, instead, to the line which carries the CPP. This may be done by means of an adaptor at the point where the synchronizing cable plugs into the back of panel 2. No wiring changes are necessary. If this change is made, when the function table transmits additively, a CPP is emitted over the decade place leads corresponding to portable function table (or even constant digit switches) set at either M or 9. Notice, these CPP are emitted from the function table at the end of the fifth addition time. As always, no pulse of any kind is emitted over a decade place lead whose corresponding switch is set at P or 0. In this way, the necessity for converting digit pulses into program pulses is obviated. The pulses emitted from the function output terminals can be taken directly to the program controls on which are set up the various programs among which a choice is made.

It should be noted that a numerical function cannot be set-up alongside of programming data on a given portable function table when this modification is made unless the function is pathologic to the extent that its tabulated values never have the digit 9 or sign M.

In connection with this discussion of the role of the function table as programming memory, mention might also be made of the fact that the function table's program controls provide a convenient way of delaying a program pulse from 5 to 13 addition times.

VIII. THE CONSTANT TRANSMITTER AND CARD READER

The constant transmitter stores eighty digits on relays (A_L to H_R in FIGS. 55–A and C) and twenty digits on constant set switches (J_L, J_R, K_L and K_R in FIG. 55–C). Provision is made for twenty PM signs, sixteen associated with the numbers stored on relays and four associated with the numbers set on the switches. One of these PM signs is associated with the five digits of each relay group. Thus, the constant transmitter can store twenty five-digit numbers and their proper signs. Provision is made to associate certain groups in pairs to form ten digit numbers by means of "constant selector" switches, which are manually set. In one addition time the constant transmitter can transmit to some other unit of the ENIAC any group of five or certain groups of ten digits and the associated sign, depending on the setting of these switches.

Whenever it is desired to set up new constants on the relays in the constant transmitter, the card reader must be programmed to read a new card. This does not change the digits set on the constant set switches; these have to be changed manually. The numerical information is derived by electrically sensing the presence or absence of perforations in predetermined regions of the card using conventional sensing arrangements and the information so derived is stored in the relay bank.

The reader completely reads a card and stores the information on relays in the constant transmitter in 0.48 second. After about 0.3 second the starting circuits of the card reader are reset and will be able to remember a second signal to read (generally this fact is insignificant since computations cannot be started until the initial data is read into the constant transmitter and, also, there is no program output from the reader to start any computation until the end of the reading cycle). If in some manner it is arranged to program the next reading of a card before the first cycle is completed (this must not occur before say 0.4 second after the initial read program and this only allows a 33% safety factor) then, due to the clutch not dropping out, the reader will read a card in 0.36 second.

Thus, the reader can read normally as many as 125 cards per minute not allowing for any computations in between. On the other hand, since each card reader time unit corresponds to about 170 addition times, and there is an interval of about 1.2 units between the finish pulse and the dropping of the holding cam contact, it seems that even though the output of the reader is used to reprogram the reader that this same pulse can be used to cause transmissions from the constant transmitter safely (safety factor=2:1). During the period of 100 addition times after this pulse, numbers could be transmitted from the constant transmitter. By the device mentioned above the speed of reading can be increased to as much as 160 cards per minute.

The description given here will be in terms of the following diagrams: (1) Constant Transmitter Cross Section, FIGURE 54; (2) Constant Transmitter Block Diagram, FIGURE 55; (3) Constant Transmitter and Reader Block Diagram, FIGURE 56; (4) Card Reader Diagram, FIGURE 57; (5)Constant Transmitter Front Panels, FIGURES 58, 59, 60; (6) Constant Transmitter Front View, FIGURE 64; (7) Cam Time Table, FIGURE 65. The discussion will be divided up into the following sections: (1) Constant Transmitter program controls; (2) card reader program controls; (3) numerical circuits of the constant transmitter; and (4) card reader.

8.1. *Constant Transmitter Program Controls*

8.1.1. *The Groups of Numbers*

As indicated above the constant transmitter stores twenty five-digit numbers and as many as twenty PM signs. These are divided into five-digit groups called A_L, A_R, B_L, B_R, . . . , H_L, H_R, J_L, J_R, K_L, and K_R (FIGURES 55–A and C). The first sixteen groups A_L to H_R are read from punched cards while the last four groups J_L to K_R are set on the constant set switches.

8.1.2. *Transceivers*

There are thirty transceivers in the constant transmitter. These are associated in groups of six. The first six transceivers (U1, U2 in FIGURE 55–B) control the first four five-digit groups of numbers A_L to B_R. The next six control the groups C_L to D_R, et cetera. Finally, the last six transceivers control the groups J_L to K_R which can be set on the constant set switches (see panel two of constant transmitter, FIGURE 59).

Two transceivers of a group of six are illustrated at U1 and U2 in FIGURE 55. These are for programs numbered one to six and control the first four five-digit groups of numbers. The output from the cathode follower of each transceiver connects to two decks of the associated constant selector switch U3. The cathode follower is used to drive the switch because fast operation of the circuit is required to make possible transmission of a constant during the addition time following the addition time in which the program pulse is received. The other outputs of the transceiver are unused.

8.1.3. *The Program Control Circuits*

Associated with the relays of digit groups one to four

(likewise for five to eight, nine to twelve, and thirteen to sixteen) there are eighty-eight tubes U4 (FIGURE 55–A). In each group there are four gate tubes for each of the five digits (as the 1, 2, 2', and 4 coded system is used to form the digits) and two gates associated with the PM indication. There are six constant selector switches U3 associated with each such set of 88 gate tubes (switches one to six with groups one to four, for example). The output terminals of these switches go directly to the grids of the gate tubes.

Switches 25 to 30 are associated with the gates controlled by the constant set switches on panel two of the constant transmitter. There are only 84 gates U4 associated with these switches since the gates associated with the correction pulse are omitted. (This means that the operator sets up complements here as complements with respect to 10^n and not 10^{n-1}).

Whenever a program pulse is received on the input terminal of a program control, at 1*i* say, the output of the cathode follower goes to the two decks of the constant selector switch. The results of the various settings on this switch are given in the following table, wherein all gate designations refer to gates U4.

TABLE 8–1

Constant Selector Switch	Result	
	Deck 1	Deck 2
A_L	The cathode follower potential opens the PM gates A'1 and A'21 (of gates U4).	The cathode follower potential opens the digit gates for group 1, that is gates B' to L', 1 and 21, of gates U4.
A_R	Gate A'41 (PM) is opened.	The PM gate A'62 and digit gates B' to L', 41 and 61 are opened. (A'61 controls the correction pulse).
A_{LR}	The PM gate A'1 is opened.	The PM gate A'62 and the digit gates B' to L' 1, 21, 41, and 61 are opened.
B_L	The PM gates A'2 and A'22 are opened.	The digit gates B' to L'2 and 22 are opened.
B_R	The PM gate A'42 is opened.	The PM gate A'63 and the digit gates B' to L'42 and 62 are all opened.
B_{LR}	The PM gate A'2 is opened.	The PM gate A' 63 and the digit gates B' to L'2, 22, 42, and 62 are all opened.

Since the constant selector switches are connected in parallel, within any group of the same alphabetical letter "back circuits" would be created should one switch be turned to L or R when another is turned to LR. For example, in the first group of six constant selector switches, if one is set at A_{LR}, no other can be set at A_L or A_R without transmitting superfluous digits (in the case of a positive number), or the extraneous transmission of 9P and 1'P over certain channels (negative number). This means that if the number stored on groups one and two relays is transmitted as a ten digit number, then at no other place in the computation can it be considered two five-digit numbers, or vice versa.

If an activated program control has its switch set to A_L, the five digits of group one will be transmitted on channels 6 to 10. If the number is negative nine pulses will be transmitted over the PM channel (A'1 of U4 turns off the inverter U7 opening the gate L43 of gates U6) and the correction pulse will be transmitted over the PM channel (A'21 of U4 turns off the inverter U8 opening the gate A45 of U9). In this case nothing is transmitted over channels one to five.

If an activated program control has its switch set at A_R the five digits of group 2 will be transmitted over channels one to five. If this number is negative nine pulses will be transmitted over channels six to ten and over the PM channel (A'41 of U4 (group 2) turns off the inverter U11 opening the gates F to K45 and L44 of U12) and the correction pulse will be transmitted over channel one (A'62 of U4 (group 2) turns off the inverter U12' opening the gate U13). The nine pulses transmitted over channels six to ten give the complement with respect to 10^{10} and make it unnecessary to use a shifter in the digit transmission line.

If an activated program control has its constant selector switch set at A_{LR} the ten digits of groups one and two will be transmitted over channels one to ten. If the number is negative nine pulses will be transmitted over the PM channel (A'1 of U4 turns off the inverter U7 opening the gate L43) and the correction pulse will be transmitted over channel one (A'62 of U4 (group 2) turns off the inverter U12' opening the gate U13).

The groups one to sixteen (or A_L to H_R) behave in a manner similar to above. The gates associated with the constant set switches (J_L to K_R) behave similarly except for the correction pulse (as explained above, or see Section 8.3.2).

8.2. *Reader Program Controls*

The reader program controls are located in the initiating unit (see FIG. 25). The card reader can be caused to read a card, (provided certain conditions are fulfilled in the reader), either by a program signal arriving at terminal R*i* on the front panel (FIG. 24) or by pushing the reader start button on that panel.

8.2.1. *Starting*

If the reader start button is pushed the resulting pulse goes through the special pulse standardizer (K100, reader start unit, see FIGURES 25–A and 55). The ouput of the special pulse standardizer turns off the inverters K101 causing the buffers K102 and K103 to go on. This sets the flip-flops K37 and K43. The driving tube K104 goes on closing the starting relay U23 located in the constant transmitter (panel #3). If a program pulse is used to start the reader it comes in over R*i* turning on the buffer K105 and setting the flip-flop K37, but not the flip-flop K43.

8.2.2. *Resetting*

After the reader starts to read the card a signal (a gate voltage) comes back over lead No. 129 (see FIG. 55–B) from the reader causing the flip-flop K37 to reset. This signal occurs early in the card reading cycle (when the minus indication is being read—before the digits are read (see cam time-table, FIG. 65)). After this reset signal has arrived any subsequent program pulse arriving over R_1 sets the flip-flop and closes the starting relay. This causes the reader to continue and read the second card before stopping. The reset signal arrives from 800 to 1200 addition times after the read program signal.

8.2.3. *The Finish Signal*

Just as the card reader finishes reading the card a signal is sent over lead No. 127 to the special pulse standardizer (K106) causing the flip-flop K42 to be set. This opens the gate K44 and if the flip-flop K43 is then set the inverter K107 will go off opening the gate K46. The CPP passed here sets the flip-flop K47 opening gate K48. This passes a CPP which goes through the transmitter K108 to the reader program output K39 (R_0). This same pulse goes through an inverter and buffer K109 and resets all three flip-flops.

The flip-flop K47 is a synchronized flip-flop, that is, it is set by a CPP gated by K46. The flip-flop K42 is not synchronized since it is set by a signal from the card reader. Thus, the gate K46 may be opened in such a way that it will pass only part of a CPP. If it fails to set the flip-flop K47 no harm is done since the next CPP will also be passed by K46 and will set the flip-flop K47. This flip-flop being set by a CPP will open the gate K48 in ample time for the next CPP. This arrangement insures that a standard synchronized program pulse is transmitted out on R_0.

8.2.4. *Interlock*

Since the process of reading a card takes a very large number of addition times it is desirable to be carrying on

part of the computation while this is being done. There will be a place in the sequence of computations where the numbers in the constant transmitter are used for the last time. At this addition time the reader may be programmed to read the next card. Since, generally, it will not be known which process, that of reading the next card or that of completing the rest of the sequence of computation, will be finished first, an interlock feature is provided. The final output program pulse of the sequence of computation is plugged to R_1. Thus, flip-flop **K43** is set at the end of the sequence of computations while flip-flop **K42** is set when the reader is finished. Only when both of these things have happened will the gate **K44** conduct and open the gate **K46**. finally giving a program pulse out of R_0.

The reader start button through buffer **K103** also sets the interlock flip-flop **K43**. Therefore, when the reader start button is pushed the reader reads a card and a reader program output pulse is obtained at R_0 at the proper time.

The initial clear gate causes all of these flip-flops to be reset. Note that when the ENIAC is turned on the starting flip-flop **K37** may come on in the set position and before a CPP arrives to reset it the reader may read one card.

8.3. *Numerical Circuits of the Constant Transmitter*

The numerical circuits of the constant transmitter comprise the sixteen groups of storage relays A_L to H_R and their associated gates **U4** et cetera, the constant and PM set switches (on panel 2) and their associated gates, the inverters **U10** and the pulse gates **U12** and the inverters, buffers and transmitters **U15**.

8.3.1. *The Storage Relays and Their Gates*

This description of the storage relays will be given in terms of the constant transmitter cross section drawings (FIGS. 54–A and 54–C). On those drawings there appear a wiring diagram of group one relays (FIG. 54–A), a schematic diagram of group one relays (FIG. 54–C), a coding cam time table (FIG. 65), and a cross section of the electronic circuits (FIG. 54–B).

As the card goes through the reader the positions on the card pass under the reading brushes in the following order (see the cam time table, FIG. 65 or FIG. 54–A).

12, 11, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9

There are eighty columns on the card and all of these pass under the reading brushes at once. Punches in the 11 position will be used to indicate minus signs, while punches in, say, position four represent the digit four in that column.

To simplify the following discussion it will be assumed that leads numbered one to eighty of the Reader connections go directly to the corresponding reading brush. Actually, these eighty connections may be made in any desired manner simply by rewiring the standard IBM plugboard on the Reader.

The relay labeled R_{AB} (see FIGURES 54–C and 56–B) is a PM isolating relay which handles the first three groups A_L, A_R, and B_L. Referring to FIGURE 65 it is seen that cam **CB9** makes contact during the reading of the eleven position on the card. If there happens to be an 11 or 12 punch in whatever column the minus indication for group one is placed, say column one, a circuit will be made through connection **97**, contact R_{AB}, and the pick-up coils of relays PM_1 and PM_2. When these relays are picked up they are held by a contact on PM_2. This holding is controlled by connection **81** (for group one) and lasts at least (it may last longer, see Section 8.4.5) until the next card has begun to be read.

The following table gives the various combinations of coding relays that are closed during the various positions of the card reading (see FIGURES 54–C and 56–B.

TABLE 8–2

Card position	12	11	0	1	2	3	4	5	6	7	8	9
With no minus indication				C_1		C_1		C_1		C_1		C_1
					C_3	C_3			C_3	C_3	C_3	C_3
											C_5	C_5
							C_7	C_7	C_7	C_7	C_7	C_7
With minus indication			C_1		C_1		C_1		C_1		C_1	
			C_3	C_3	C_3	C_3			C_3	C_3		
			C_5	C_5								
			C_7	C_7	C_7	C_7	C_7	C_7				

The reader can check this table in the following manner. If the number is positive the coding relays C_1 to C_8 are connected in pairs to the coding cams **CB2**, **CB4**, **CB6**, and **CB8**. The coding cam time table shows that as position seven of the card, for example, is under the reading brushes coding cams **CB2**, **CB4**, and **CB8** are making contact. If seven was punched in the first column storage relay **1A**, **1B**, and **1D** will be activated through the contacts on coding relays C_1, C_3, and C_7. Contacts on the storage relays will cause gate tubes **L'1**, **K'1**, and **K'21** of gates **U4** to be opened, ultimately causing the 1, 2, and 4 pulses (altogether seven pulses) to be transmitted over channel ten. If there had been a minus indication punch the PM relays (PM_1 and PM_2) would be closed (and held by the circuit through connection **81**) and the coding relays would be connected to coding cams **CB1**, **CB3**, **CB5**, and **CB7**. If again, seven were punched in the first column, only cam **CB3** is making contact when the seven passes under the reading brushes and the contact on C_3 causes storage relay **1B** to be picked up. Ultimately, this causes the two pulses (complement of seven) to be transmitted over the tenth channel. Since the PM relays are closed, a contact on PM_1 causes gates **A'1** and **A'21** to be opened,. These gates provide (for a five digit number) for the minus indication (nine pulses on the PM channel) and for the correction pulse (to give complements with respect to 10^n).

8.3.2. *The Constant and PM Set Switches (J_L to K_R)*

FIGURE 55 shows that these switches connect directly to the gates for the numbers J_L to K_R. Only the switches for the first and tenth digits are drawn out in detail for the groups J and K. There are four PM switches, so these twenty digits can be used in groups of five and the signs of any one group set independent of the others. If they are to be used for ten digit numbers then both PM switches (J_L and J_R, for example) must be set to P or to M depending upon the number.

The constant set switches consist of four parts mounted on two decks. The moving portion makes contact in such a manner as to open the 1, 2, 2', and 4 gates in various combinations corresponding to the digit to which the switch is set. The gates opened by various switch settings are indicated by the crosses in the following table.

TABLE 8-3a

Gates	Switch Setting									
	0	1	2	3	4	5	6	7	8	9
1		X		X		X		X		X
2			X	X			X	X	X	X
2'									X	X
4					X	X	X	X	X	X

In the case of negative numbers read from cards the coding relays automatically take the complements with respect to 10^{n-1}. This is not true of the constant set switches for groups J_L to K_R, that is, in setting up a negative number on these switches the operator must take the complement himself. No correction pulse is pro-

vided by these PM switches so negative numbers are set up as complements with respect to 10^n. The following table illustrates various switch settings.

TABLE 8-3b

Number to be set up	PM Settings		Switch Settings									
	J_L	J_R	1	2	3	4	5	6	7	8	9	10
+23456 on J_L and +78901 on J_R	P	P	2	3	4	5	6	7	8	9	0	1
−12345 on J_L and +78901 on J_R	M	P	8	7	6	5	5	7	8	9	0	1
12345 on J_L and −78901 on J_R	P	M	1	2	3	4	5	2	1	0	9	9
12345 67890 on J_{LR}	P	P	1	2	3	4	5	6	7	8	9	0
−12345 67890 on J_{LR}	M	P	8	7	6	5	4	3	2	1	1	0

8.4. *The Card Reader*

The Card Reader, FIGURES 56–A and 56–B, will be described in terms of the wiring diagram FIGURE 57. Surrounding this drawing are zones of latitude (A–D) and longitude (1–7) which give the locations of the relays and cams. Note that the various parts of one relay (for example, the hold coil, pick-up coil, and various contacts) may be located in widely different places on this drawing. The zones locate all of these parts. The terminal posts are located in the panel behind the motor generator. The connections to the Card Reader plug (which plugs into a socket on the constant transmitter panel number three) are pictured in the upper right corner of the drawing. Since the Card Reader circuit is well known, and the drawing is self-explanatory, it will not be described in greater detail than is necessary to show its relation to the relays and gates of the Constant Transmitter.

8.4.1. *The A.-C. Circuits*

The Reader receives its A.-C. power by a standard 110 volt plug which plugs into a socket on the bottom of panel three of the constant transmitter. Power is furnished to this plug only when the ENIAC is turned on, plugs at the bottom of other panels, except printer panel #2, have power on them all the time. The A.-C. power goes through a switch located on the Reader to the motor-generator and through contacts (on H.D. relay at 1A) on a relay (pick-up coil at 2B) to the drive motor. Thus, when the power comes on the motor generator starts up. When it reaches speed the 40 volts D.-C. cause a green light (on the front of the Reader) to come on and the H.D. relay to close starting the drive motor. The H.D. relay prevents the drive motor from operating in case of failure of the motor generator.

8.4.2. *Starting Circuits*

When cards are initially placed in the magazine, the magazine card lever contact (Mag. at CLC at 2B) is closed. This causes relay R1 to pick-up. At this time neither the auxiliary read switch nor the ENIAC starting relay (in the constant transmitter, see FIGURE 55) can cause the reader to operate since relay R2 is not activated.

If in this case, the initial start key is pushed, the reader will operate (assuming card magazine switch closed, that is, there are not too many cards in the card magazine) and feed a card into position before continuous roll #1 (that is, in position ready to be read by the control #1 reading brushes). When the card is in position here, relay R2 is activated by card lever contact #1. Now either the auxiliary read switch or the ENIAC starting relay can cause a card to be read. The initial start switch, since relays R1 and R2 are each activated, cannot cause a card to be read at this point. Thus, upon closing either the auxiliary read switch, or the ENIAC starting relay the card passes under the #1 (control) reading brushes and stops in position before the #2 read brushes.

If any of the control arrangements (like plugging to control hubs on the plug-board) are being used the "control" instructions are now remembered by certain relays in the Reader. Note, that this memory depends upon the 40 volt output of the motor-generator on the reader.

With the first card in position before the #2 read brushes, a card lever contact (CLC #1) causes R60 to be activated. If the auxiliary read switch is again operated this card will be read by the #2 brushes and the (signed) numbers stored in the constant transmitter relays.

In practice the relay timing is such that in initially placing cards in the reader (by placing cards in the magazine and depressing the initial start key) the reader may feed cards up to position before the #2 read brushes by running through two cycles. In this case it is ready to immediately read the first card. If the first card was fed only into position before the #1 or control brushes (one cycle) no harm is done. If the reader is now programmed to read, relay R60 being open, it will read the 1st card by the control brushes and no reset or finish signal will be given out. Then, the starting relay still being closed, the reader will immediately start another cycle in which the first card passes under the #2 brushes. When the cards are in position, relays #1 and #2 are activated by the card contact levers (Magazine CLC., CR. #1, CR. #2) and the start key becomes ineffective. After relays #1 and #2 are activated, contacts on them (at 3B) enable the auxiliary start key to cause a card to be read. A starting relay located in the constant transmitter (see FIG. 55) has a contact connected in parallel with this auxiliary start key. A unit located in the initiating device (described in 8.2) causes this starting relay to close and thus causes the reader to read a card.

8.4.3. *Numerical Circuits*

There are two sets of 80 reading brushes, the first (#1) are the control brushes and the second (#2) are the ones which read the numbers and their signs. The number two reading brushes (at 6B) read the numbers and PM signs on the cards and via connections on the plug board carry the corresponding signals to the storage relays in the following ways:

(1) Directly to the storage relays (hubs located at 6D).

(2) For a column in which the PM punch occurs the connection is from the reading brush hub to one of the PM hubs (labeled "minus control" on the plug-board) (at 6D in FIG. 57) and from the other PM hub to the corresponding storage relay hub.

(3) Or, if desired, the connections from the reading brushes to the storage relays may be by way of the group selector relay contacts (at **6B** and **6C**). In this manner certain control punches may cause information from one set of reading brushes to go to either one of two sets of storage relays, or such control punches may cause one set of storage relays to receive information from one of two sets of reading brushes (see Sections 8.4.4 and 8.4.5).

8.4.4. *Group Selection*

There are sixteen five-pole, double-throw relay switches (relays **R24** to **R55**, two relays to each switch, hold coils at **4C** and **5C**, contacts at **6B** and **6C**). The coils at **4C** and **5C** serve for picking up and for holding. These five-pole, double-throw switches may be used to rearrange the information coming into the storage relays. These relays are picked up by contacts on relays **7** to **22** (at **4C** and **5C**) in series with the cam **P6**. Once they are picked up they are held by cam **P7**.

Referring to the cam time table (FIG. 65) we see that relays **7** to **22** may be picked up any place in the card cycle, that is, from any punch (since cam **P5** makes contact all this time). If any of these relays have picked up, cam **P6** will cause the corresponding relays **24** to **55** to pick up at the end of the card cycle. Once they are picked up cam **P7** holds them until the end of the next card cycle. Since the card going under the control brushes will go under #2 read brushes exactly one card cycle later, this means that a group selection control punch will activate the group selection relays during the time the card is passing under the #2 read brushes.

8.4.5. *Reset Control and Reset Shunt*

The storage holding relays (contacts at **7B**, pick up coils at **3C**) **4**, **5**, and **6** cause the relays in the constant transmitter to hold their information. The time table shows that cam **CB10** causes these relays to hold from position 12 on one card until 13.7 on the next card. That is, the information read from one card is normally dropped out at the beginning of the reading of the next card.

By plugging from the reset control hubs to the reset shunt the corresponding constant transmitter relays can be caused to hold their information until such time as the relays **56** to **58** are activated.

By proper plugging on the plug board connection can be made from the #1 read brushes through the pick up coil of relay **23** to the digit selector. When relay **23** is activated relays **56** to **58** will be picked up by cam **P8** at 7.6 in the card cycle. A contact on relay **57** and cam **P1** causes relay **59** to pick up at 9.5 in the card cycle.

Suppose that reset control is operated from a "three" punch in some column in what will be called a *master card*. Card without this "three" punch (in that same column) will be called *detail cards*.

At the end of a cycle in which such a master card passed under the control (#1) brushes relays **23**, **56** to **58**, and **59** have all picked up. During the next card cycle the master card will pass under the #2 read brushes. Relay **59** holds until near the end of this cycle preventing either a reset or a finish signal. Inspection of the reader starting circuit in FIGURE 55 shows that the starting flip-flop **K37** is still set and that the starting relay is still activated so the reader immediately goes on to read another card. The relays which are shunted (by plugging reset control to reset shunt on the plug board) will hold the information read from the master card until another master card comes along. New information will be put into the other relays for each detail card.

8.4.6. *Coding Cams*

The coding cams are located at **6A** and **7A** in FIGURE 57. They directly operate the coding relays located in the constant transmitter. See 8.3.1.

8.4.7. *Reset Signal*

Cam **P4** produces the reset signal at time 12 in the card cycle. This signal will be sent to the constant transmitter (actually to the initiating unit) only if relay **R60** is activated and relay **R59** is not. Relay **R60** is activated only when cards are in position at the #2 read brushes (see CR#2 at **3B**, that is, continuous roll #2). Relay **R59** is activated only when a "master" card (a card with a punch operating reset control relay **23**) is at the #2 read brushes.

8.4.8. *Finish Signal*

Cam **P3** produces the finish signal at time 9.5 in the card reading cycle. As with the reset signal this signal is obtained only if relay **60** is activated and relay **59** is not.

IX. PRINTER AND CARD PUNCH

The printer and gang card punch are the means used in the ENIAC to permanently record the results of any stage of the computations performed by the machine. It will be obvious that any suitable recording means could be employed for this purpose—for example, the neons which instantaneously display this result could be photographed by means energized by a signal from the ENIAC. Conversely, such photographic data could be optically scanned by known photoelectric means to provide an alternative "reader" of input data, instead of the card reader described in the preceding chapter, or magnetic recording and transcribing means could be employed. Because of the availability of the card reading equipment, and the relative ease with which it could be adapted to the purpose, it was decided to use this equipment, which will be described below in sufficient detail to show the relationship between the gates and tubes of the ENIAC and the gang card punch equipment.

The printer causes eighty digits and as many as sixteen PM signs which are stored in certain accumulators and possibly the master programmer to be punched on cards. In the case of complements (which represent negative numbers) the printer relays cause the card punch to punch the true negative number and a corresponding sign indication (an 11 punch).

When operating continuously the card punch can punch a card in 0.61 second. However when starting from rest, the inertia of the punching mechanism makes the punching time 0.82 second. The units of the ENIAC associated with the printer (eight accumulators, say, and five decades of the M.P. do not have to wait while the complete punching cycle takes place but only 0.4 second. If the punch is programmed before the end of the first cycle to punch a second card then the two cards will be punched in 1.4 seconds. However, if the second program signal comes any time after the first cycle is completed the punch essentially loses a cycle (because of the clutch dropping out) and the punching of two cards will take at least 2.0 seconds.

Therefore, if there is no more than approximately 2,000 addition times between printing programs, the punch will punch almost 100 cards per minute. A small increase in the number of addition times between printing programs will cut this down to not more than 50 cards per minute. It should be emphasized that while all these figures are valid for new equipment, they may vary with time, temperature, punch wear, and so forth.

The program control circuits for the printer are located in the initiating unit. When programmed to print, the card punch will start, the relays in the printer will be set up by the static outputs of the various decades and PM units, a reset signal will come from the punch to the program control circuit, and the punch will complete the punching cycle. The reset signal can be used to continue computation in the ENIAC. Since the set up time of the relays is small compared to the time for punching a card this arrangement prevents undue waste of time while the card is being punched. When the card

punching cycle is completed an interlock signal comes from the punch to the printer allowing the relays to set up anew provided another print program signal came along in the meantime. This constitutes a mechanical interlock arrangement.

On the printer there are sixteen "print" switches which enable the operator to print or not print any one of sixteen groups of five digit numbers and the associated PM indication. There are sixteen coupling switches which make possible the printing of groups with ten or more digits. These coupling switches serve no purpose when printing positive numbers. In printing negative numbers they take care of the carry over in the process of taking the complements and also gang the PM relays for the coupled groups.

The discussion will be divided up in the following manner: 9.1, Program Control Circuits; 9.2, Numerical Circuits of the Printer; and 9.3, Gang Card Punch.

The following diagrams relate to the printer and card punch:

Card Punch	FIGURE 66.
Printer Block Diagram	FIGURE 67.
Printer Front Panel	FIGURES 61, 62, 63.
Printer Cross Section	FIGURES 68–A and 68–B.
Initiating Unit Front View	FIGURE 23.
Initiating Unit Front Panel	FIGURE 24.
Plug Board for Gang Punch	FIGURE 70.
Cam Time Table	FIGURE 69.
Initiating Unit Block Diagram	FIGURE 25–A.

9.0 *General Sumary of the Card Punch and Printer*

Data stored in electronic counters of certain units of the ENAIC is taken to an array of tubes in the printer by static output leads which run along a trough at the top of the ENIAC. For each 5 digit group (of the total of 80 digits which can be punched on one card) there are 5 rows of 10 tubes each for the input of digital data. These tubes are labelled (FIGS. 68–A and 68–B) by a letter from A to E followed by a number between 0 and 9 inclusive. In addition, for each 5 digit group, there are 3 tubes for recording minus indication belonging to the group. Associated with each input tube is a printer relay. The printer relays for digits are labelled in the same way as are the tubes. The relays for minus sign indication are labelled **M1**, **M2**, and C_0. The last relay C_0, is referred to as the carryover relay. A printer relay is activated when its associated tube goes "on." The hold contacts on these relays are connected to the holding cam in the punch (see FIG. 66) so that when this cam breaks at time 9.5 in the card punching cycle the printer relays release. The card punching cycle is divided into 14 units as is the card reading cycle discussed in Chapter VIII.

It is to be noted that the input tubes and printer relays are set up in accordance with the digital information as it is stored in the accumulators connected to the printer, i.e., complements are set up as such. In this chapter, the word complement is restricted to mean the complement of a positive number. Complements are converted to negative numbers before punching takes place through the intervention of relays C_1 through C_5, the PM relays, **M1** and **M2**, and the carry-over relay, C_0. The carry-over cam in the punch (see FIG. 66) also plays a part in this conversion.

In the card punch, as in the reader, there is an emitter with 12 stages (12, 11, 0, . . . , 9 with stage 11 the minus punch stage, located at **10**C, FIG. 66). Certain stages of the emitter are connected through so called PM transfer contacts on the minus relays (**M1** and **M2**) to contacts on the printer relays which register digital information. The latter, in turn, are connected through transfer contacts on the relays C_1 through C_5 to lines which carry signals for punches in the various columns to the computer result exit plugs on a card punch plug board. By means of plug board wiring, these signals can be delivered to the punch magnets (see FIG. 66) for any desired column of the card.

Each of the 80 punch magnets operates a lever with a little head on it. When a punch magnet is activated, the lever moves forward and a hammer bar in the punch hits the head of the lever against a punch shaft. Thus, a hole is punched in the column with which the lever is associated. Since, throughout the punching, the card moves forward in synchronism with the emitter, the hole is punched in the digit row corresponding to the activated printer relay for that column.

Data may be punched in all 80 columns of the card or, if desired, certain columns of 5 digit groups may be left blank. If the print switch of a 5 digit group (see FIG. 62), which has the positions "print" and "off," is set at off, the printer input tubes for the group of numbers do not set up and punch signals for that group are not delivered to the card punch. No punch is made in a column for which there is no plug board connection between computer result exit plug and punch magnet plug.

The total of 80 digits can be broken up into signed 5, 10, 15, . . . , or 80 digit groups by means of the coupling switches on panels 1, and 3 of the printer. The numbering on these switches corresponds to the numbering of the printer relay groups. When a coupling switch is set at C, the 2 five digit groups whose numbers appear on that coupling switch nameplate are considered as one for sign indication purposes and for complementation. If two adjacent coupling switches are set at C, the three groups whose numbers appear on the switches are considered as a single 15 digit group, etc. The use of PM adaptors is also involved in the coupling or isolation of five digit groups.

Certain programming circuits for both the printer and punch are located in the initiating unit of the ENIAC and others are in the punch itself. Located at the initiating unit (see FIGS. 68, 67 and 25–A) are the printer program pulse input terminal **K52** (P_1), start flip-flop (**K51**), finish flip-flop (**K53**), synchronizing flip-flop (**K54**), program output pulse transmitter **K111** and terminal **K56** (P_0). Neons correlated with these flip-flops are shown in FIGURE 23. The start flip-flop operates a printer start relay located in the printer.

On the punch there are start and stop switches and a master-detail switch (which should, however, always be set at master). Inside the punch (see FIG. 66) are found a start relay (**R10**), the motor hold relay (**R9**) and H.D. No. 1 motor relay, relays **1** and **3** which are associated respectively with the die card lever contact (Die CLC in FIG. 66) and the magazine card lever contact (Mag. CLC), and relay **23**. The program controls in this and the preceding paragraph have to do with starting and stopping the printer and punch and will be discussed at greater length in the following sections.

In addition to the switches and relays mentioned above, two of the cams in the punch, the interlock and reset cams, act as programming circuits. The timing for these cams is shown in FIGURE 69. When the interlock cam makes contact, and when the starting relay located in the printer (see FIGURE 67) is activated as a result of the reception of a program pulse by the printer program pulse input terminal, the input tubes are connected to 20 v., which allows all groups with print switch set at print to set up. When the interlock cam breaks (12.8–13.3), the input tubes cannot set up. The reset cam which makes in the period 11.2 to 11.8 provides a reset signal for the start flip-flop **K51** and sets the printer finish flip-flop **K53** which results, finally, in the transmission of of a program output pulse by the printer (see Sec. 9.1).

9.1. *Programming Circuits of the Printer and Card Punch*

The printer program control circuits comprises most of two plug-in units in the initiating device and the printing switches located on panel two of the printer. The cir-

cuits located in the initiating device are represented in block diagram form in FIGURES 67–A, 68–A and 25–A.

A program pulse received at the printer program pulse input terminal on the initiating unit flips the printer start flip-flop K51 into the abnormal state. The resulting signal from the start flip-flop energizes the start relay in the printer.

Provided that there is at least one card in the magazine (so that Mag. CLC, FIG. 66, is closed and relay 3 is activated) and provided that there is a card in the punch position (so that Die CLC is closed and relay 1 is activated), the signal from the printer start relay carried to the punch over circuit I–11 activates R23. As long as the printer stop switch is not thrown and under the conditions noted above for Mag. CLC and Die CLC the circuit to the punch start relay (R10) through R23 BL is now closed so that R10 is activated. Now, with contact R10 BL closed, the motor hold relay (R9) and the H.D. No. 1 motor relay in parallel with it are activated so that the drive motor starts up. Also, with R10 BU closed the printer clutch is activated so that a card is pushed through the punching apparatus. R10 holds through its hold contact R10 AL until cam P5 breaks at time 9 in the punch cycle.

9.1.1. *The Printing Switches*

The printing switches simply disconnect the power (200 v. line) to the digit and PM relays of each group. Thus, if the print switch for a particular group is set at "off," the relays of that group cannot pick-up and thus nothing will be punched in the corresponding position on the card.

9.1.2. *Starting Circuit*

Any pulse arriving at the printer program input terminal P_I (see FIG. 25–A) will (through the buffer K112) set the flip-flop K51. This causes the driver K113 (which has its cathode at 20 volts and has the starting relay as its load) to come on, closing the starting relay (located in the printer panel No. 3). This flip-flop will be reset by a signal arriving from the punch through the buffer K114. (It can be reset by an ICG, see Section 9.1.5).

9.1.3. *Reset and Program Output*

After the printer relays have set up (these relays set up when the interlock cam makes contact and the starting relay is activated) near the beginning of the card punching cycle (at card time 11.2) the reset signal will arrive at the printer from the punch. This signal passes through the special pulse standardizer K110 (in unit K115, see FIG. 68–A; for a description of this circuit see Section 1.2.12). The output of this pulse standardizer sets the finish flip-flop K53 and also through the associated inverters K117 provides a reset signal for the starting flip-flop described above.

The finish flip-flop K53 opens the gate K57 passing a CPP which sets the flip-flop K54. The output of this flip-flop gates a CPP (gate G58) which resets the two flip-flops passing through the transmitter K111, and appears at the printer output terminal K55 (P_o) on the initiating unit front panel (see FIG. 24). At the time of initial machine use, starting with the punch at rest about 1900 addition times elapsed between the reception of a program pulse at P_I and the output program from P_o.

This double flip-flop arrangement is a synchronizing device. Since the timing of the reset pulse depends upon the mechanical operation of the punch it will generally not be synchronized with the CPP in the ENIAC. The output of the gate K57 will be synchronized, but it cannot be transmitted since the flip-flop K53 may be set at such a time that it would pass a substandard pulse. If the CPP passed by K57 is weak and does not set the flip-flop K54 no harm is done for the next CPP (K53 is not reset in this case) will be standard and will set K54. The circuits comprising these flip-flops and their associated gates tubes are relatively slow (the rise time is on the order of 50 μ-seconds). Thus, if a CPP sets the flip-flop K54, the gate K58 will open only in time to safely pass the CPP which arrives one addition time later, and the output of gate K58 will always be a standard pulse. Note that this program output occurs before the card punching cycle is completed (assuming the punch starts from rest and at the time of writing this specification this time was approximately 1950 addition times).

9.1.4. *The Interlock Cam*

The interlock cam makes contact near the end of the punching cycle (card time 13.3) and breaks near the PM punch of the next card cycle (time 12.8) (see the time table FIG. 69). This cam and a contact on the starting relay (in series) connect the cathodes of all the tubes in the printer to 20 volts. When this circuit is open the cathodes rise (see the 2K, 10 watt resistor near the starting relay in FIG. 67) to about 200 volts. Since this is about the same potential as the plates, any signal on the grids (and generally there will be signals on certain of the static outputs) will not cause any of the tubes to go on and set up their corresponding relays.

The printer may again be programmed to print any time after the reset signal has arrived (see Section 9.1.3). However, except for the activation of the starting relay, nothing will happen until the end of the cycle which the punch is in; until the interlock cam makes contact. This furnishes a mechanical interlock arrangement. The second print signal cannot cause any tubes to conduct and relays to set up in the printer until the first punching cycle is complete. At time 9.5 in the first cycle, the holding cam breaks contact releasing all relays in the printer. At time 13.3 the interlock cam makes and (provided the start relay is activated) the printer relays set up in the new way and a second card is punched.

Table 9–1 gives the timing of the printing sequence.

TABLE 9-1

Approx. Add. Times	Time Secs.	Card Time	Activity
0	0	D	Printer program pulse arrives (at initiating unit).
			Starting relay closes (in printer).
			Card punch starts and relays set up.
		13.6	Carry-over cam makes.
		14.5	Holding cam makes.
		12.8	Interlock cam breaks (this turns off all tubes in printer and, thus, releases the accumulators and master programmer for other activities).
		11	PM indications are punched.
1900 to 2000	.4	11.2	Reset cam closes causing: (1) Starting flip-flop to reset. (2) Printer program output pulse to be transmitted.
			ENIAC proceeds with other computing.
		11.8	Reset cam breaks.
		0	
		1 to 9	Digits are punched.
		9.36	Carry-over cam breaks.
		9.45	Holding cam breaks.
3050	.6	13.3	Interlock cam makes. Relays will set-up again as soon as starting relay is closed. Note that the next printing signal may arrive any time after the reset cam breaks, that is, any time *after* 11.5.
		D	Punch stops unless starting relay has been closed.

Clearly, the programming in the ENIAC must not be arranged so that a second print program input pulse arrives at P_I before the reset signal has been given out by the punch and the flip-flop K51 has been reset. Hence, no pulse should be supplied to the printer program input until after a pulse has been emitted from the printer program output P_o. Any pulse arriving after the reset signal but before the end of the card punching cycle (that is, during the period 11.2 to D) will be remembered and will cause the punch to continue and punch the next card.

9.1.5. *Initial Clear*

The only place that the initial clear gate is used in the printer circuits is to reset the starting flip-flop K51 (FIG. 25–A in the initiating unit).

9.2. *The Numerical Circuits of the Printer*

Of the sixteen relay groups, groups one and sixteen and parts of groups two and fifteen are represented in FIGURE 67. Assume that the plug-board is so wired that the columns (A, B, C, D, and E) correspond to the first five columns on the card. Suppose, furthermore, that the PM indication for this five digit group is to be punched in column one or A.

There are fifty digit triodes in group one (actually 25 6SN7's) and three PM triodes. The grids of these tubes connect direcly by a 51 line cable to the static outputs of the decades and PM unit of an accumulator. Just one PM line goes to the three grids of the PM tubes.

The tubes in each column are denoted by A0 to A9, B0 to B9, et cetera; that is, the second symbol denotes the digit represented by that tube being on. The grids of these tubes are connected to the normally negative outputs of the stages of the decade rings. The PM line in the cable goes to all three PM tubes (the tubes driving the carry-over relay C_0' and the PM relays M1 and M2).

The leads from the emitter arrive at the upper left corner of FIGURE 67. These emitter leads go through transfer contacts on the relays M1 and M2 to the various digit levels in the five columns of relays.

All the digit and PM relays have holding contacts connecting them to a line controlled by the holding cam. The holding cam makes at the beginning of the punch cycle (at time 14.5, see Table 9–1) and breaks at the end of the cycle (at 9.45). These holding contacts cause any relays which are picked up by tubes conducting to remain up until the end of the cycle. Thus, the printer tubes need to conduct only long enough to safely pick up the relays. This determines the length of contact made by the interlock cam (13.3 to 12.8) (note that if the punch stops between cycles then the tubes begin to conduct at time D=13.5 when the starting relay is activated). Once the relays are picked up the tubes can be turned off by the interlock cam and all the units which connect statically to the printer groups whose print switch is "on" can then be released to participate in further computations.

If the interlock cam has made contact and the starting relay is closed, then one digit relay (in each column) picks up, corresponding to the actual number registered in the decade of the accumulator or master programmer. All three PM relays will pick up together if the number is negative.

Suppose the number P12345 is registered in the decades and PM unit of an accumulator associated with group one relays. If the print switch of group one is set to print and the starting relay is closed (assuming the interlock cam is making contact) then the tubes A1, B2, C3, D4 and E5 will conduct closing relays A1, . . . , E5.

As the card passes under the punches, pulses arrive from the emitter over the emitter lines. Since the above nmber was positive all three PM relays (C_0, M1 and M2) are unactivated. This means that there is a connection from emitter line "one" through the transfer contact on M1, through the contact on A1 to the transfer contact on C_1, and on to the punch magnet (via the punch plug board) for column one on the card. Thus, when the one position on the card is under the first column punch a signal from emitter line "one" will (through this circuit) cause "one" to be punched in the first column of the card. The circuits for the above number and for M12378 are illustrated by the rows in the following tables. In these tables (A) denotes that the relay is in the abnormal or activated position while (N) means that the relay is in the normal position.

The resistance-capacitance circuits found on the contacts of the carry-over relays (and on one contact of the starting relay) are to prevent arcing at the contacts. The protection is necessary only on contacts which carry relative heavy loads, and not only prolongs the life of the relay but provides more reliable operation.

In the case of the number M12370, the minus indication will cause relay C_0 to be activated which in turn (assuming the coupling switch 1–2 is set to "0") causes C_5 to operate. Since the last digit is zero, relay EO (group 1 relays) will be activated which will cause C_4 to operate.

TABLE 9-2.—CIRCUITS FOR THE NUMBER P12378

Emitter Line	PM Relay transfer contact	Digit relay contact	Carry-over relay transfer contact	Line to Punch Magnet (via plug-board)
1	M1 (N)	A1	C_1 (N)	1
2	M1 (N)	B2	C_2 (N)	2
3	M1 (N)	C3	C_3 (N)	3
7	M2 (N)	D7	C_4 (N)	4
8	M2 (N)	E8	C_5 (N)	5

TABLE 9-3.—CIRCUITS FOR THE NUMBER M12378 (−87622)
[Relays C_0, C_5, M1 and M2 are now activated, C_1 to C_4 normal, coupling switch at 0]

Emitter Line	PM Relay transfer contact	Digit relay contact	Carry-over relay transfer contact	Line to Punch Magnet (via plug-board)
8	M_1 (A)	A1	C_1 (N)	1
7	M_1 (A)	B2	C_2 (N)	2
6	M_1 (A)	C3	C_3 (N)	3
2	M_2 (A)	D7	C_4 (N)	4
2	M_2 (A)	E8	C_5 (A)	5

NOTE.—In the above tables (N) means the relay is in normal or unactivated position while (A) means it is in the abnormal or activated position.

The carry relays C_1, C_2 and C_3 will not be activated so the circuits take complements with respect to ten (modulo ten) in the units and tens place and with respect to nine in the other places.

It is essential that the carry-over cam breaks before the holding cam does. If the holding cam were to break first, then a string of carry-over relays which may have picked up would be dropped by the contact on relay C0 and since the carry-over relays which have picked up are connected in parallel the load here would soon burn up the contact on C0. Since the carry-over cam breaks first (at 9.36 as against 9.45 for the holding cam) the contact on C0 will not be breaking any current.

There is one PM unit in each accumulator and there are two sets of PM relays (one set with each five digit group). Thus, to print ten digit negative numbers the PM static output must be connected to both sets of PM tubes. This is accomplished by the use of an adapter which connects the two PM lines to the one static output. In case of twenty digit operation an adapter must be used to connect the four sets of PM tubes to the PM static output of the left hand accumulator.

The adapters for the ten digit operation are installed in the backs of the respective accumulators. This adapter is a plug and two sockets; the plug goes into the PM static socket (on the PM-clear plug-in unit) and the two sockets receive the two PM lines of the two static cables. The adapters for more than ten digit operation are best installed in the printer (behind front panel No. 2) (those for ten digit operation could be installed here, too).

To make it possible to print the actual numbers registered in certain decades (regardless of sign) there is a ground lug on the printer plugs which normally connect to the static PM leads. Another adapter (a socket with a jumper inside) used here grounds the grids of the PM tubes. This prevents them from conducting; if the grids are allowed to "float" the tubes may or may not conduct.

Such an adapter must be used, for example, whenever printing numbers from decades in the master programmer.

9.3. *The Gang Card Punch*

The gang card punch will be described in terms of FIGURE 66. This punch was constructed in the following manner: An unfinished standard gang summary punch was removed from the assembly line and certain details, such as cams and column split relays were added to make a punch for use with the ENIAC. This means there is some unused apparatus in the punch; for example, there is a set of control reading brushes and the continuous roller is in for the regular set of reading brushes. This also explains why there are shunts on some relay contacts. The master-detail switch located on the front of the punch simply acts as an on-off switch for the punch magnets ("on" corresponds to "master").

9.3.1. *The A.-C. Circuit*

The A.-C. connection is normally plugged to the outlet on the bottom of panel two of the printer. Power is furnished to this outlet only when the ENIAC is turned on. Outlets on all other panels except panel three of the constant transmitter have power all the time. Thus, if it is desired to operate the punch without turning on the ENIAC one of the outlets of one of the other printer panels may be used.

When the A.-C. power is turned on H.D. relays No. 2 and No. 3 close starting the motor generator and closing the 40 volt D.-C. circuit. The green light on the front of the punch indicates that the motor generator is operating properly. The drive motor is started by the closing of contacts on H.D. relay No. 1. The pick-up coil for this relay is in parallel with **R9**. **R9** is picked up by a contact on **R10** and another contact on **R10** operates the clutch. Thus, relay **10** is the starting relay.

9.3.2. *The Starting Circuit*

There are three card lever contacts,

(1) Die card lever contact (Die CLC)
(2) Magazine card lever contact (Mag. CLC)
(3) Brush card lever contact (Br. CLC)

which activate relays **1**, **3**, and **7**. These card lever contacts determine if the cards are being fed in properly. There is a die contact which determines if the punch die is in proper position. If the die contact is open, neither the start key on the punch, nor the starting circuits of the ENIAC will operate the punch. The various card lever contacts are by-passed by the start key on the punch. Thus, it can be used to feed the cards into position when they are first put into the magazine.

If the magazine runs out of cards the punch will stop. If the starting relay is closed the printer relays will pick up and the punch will operate the moment new cards are placed in the magazine. The operator should hold down the stop key when putting new cards in this case. Otherwise, the punch may start before the cards are firmly seated and may fail to feed the first card.

To start the punch, the ENIAC completes the circuit from terminals one to eleven. This, through contacts on relays **1** and **3**, closes **R23**. A contact on **R23** causes **R10** to close. Contacts on **R10** cause **R9'**, relay H.D. No. 1, and the clutch to pick up. Relay **9** and H.D. relay No. 1 are held by **R10** and by the continuously running cam (C.R. cam). Relay **10** in turn is held by cam **P5**. Thus, when the starting relay is closed in the printer, relays **9** and **10** pick up and hold until the end of the card punching cycle. At that time they drop out as does H.D. No. 1. The clutch drops out when relay **10** drops and the drive motor coasts to a stop.

Note that the operator must use the initial start switch to feed cards into position when starting, since with cards only in the magazine the ENIAC starting circuits will not operate.

A card stacker switch opens the starting circuit when too many cards are in the stacker. When the cards are removed the machine will continue to operate in the proper manner.

9.3.3. *The column Splits (PM Circuits)*

The pick-up coils of the column split relays are located at **5C** in FIGURE 66. These relays are activated by cam **P2** during the time that the 11 and 12 positions of the card are passing under the punches (actually, from 13.6 until 11.6). The relays act as a sixteen-pole, double-throw switch (see contacts at **7** and **8A** and B) and connect the punches (via plug-board connections) to the minus indication terminals (at **8D**) during the 11 and 12 positions of the card and to the computer result exit terminals (8D) during the rest of the card cycle. This makes it possible to punch a PM indication and a digit of a number in the same column.

9.3.4. *The Punch Magnets*

The circuits to the punch magnets is completed by contacts on relays **43** to **56**. These relays are activated by a circuit through the master-detail switch (with switch setting on "master"), a normally closed contact on, **R14** and cam **P12** (makes at 14.3 and breaks at 9.3).

9.3.5. *The Emitter*

The emitter is located at **10C**. It turns in synchronism as the card passes under the punch magnets, that is, the emitter connects to line 3, for example, when position three is under the punches. If the circuit is completed from emitter line three back to the punch magnets then three will be punched.

9.3.6. *The Plug-Board*

Instructions for plug-board connections appear in FIGURE 70. The eighty-digit outputs appear on eighty hubs on the plug-board. The eighty punch magnets appear on eighty other hubs. Thus, information can be rearranged on the card in any desired manner.

X. MASTER PROGRAMMER

The master programmer is a central programming unit whose primary function is to direct and stimulate the performance of the program sequences of various levels which enter into a computation. While the master programmer is capable of stimulating the performance of individual programs, it is usually not required for this purpose. It is, however, essential to use the master programmer to accomplish the iteration of a program sequence into a chain or to link together chains and program sequences. The master programmer can link programs together either serially or on the basis of magnitude discrimination. The master programmer may also be used as a counter in that it is capable of storing numbers (without sign, however) and also of adding by counting pulses. This latter feature enables the operator to store values, say of the independent variable, in the master programmer. Certain decades of the master programmer have been connected to the printer so that a number stored in these decades can be printed.

Reference will be made to the following diagrams:

Master Programmer Front View ..... FIGURE 71.
Master Programmer Front Panels ..... FIGURES 72–A and B.
Master Programmer Block Diagram ..... FIGURES 73–A to D.

The master programmer occupies two panels. The two panels are practically identical in function and in appearance. The block diagram, FIGURE 73, refers to the left hand panel; however, by changing some of the terminology, it can refer equally well to the right hand panel. Thus, in the following discussion only the left hand panel will be considered. In the left hand panel the decades are numbered from 11 to 20 (reading from right to left as in an accumulator) and the steppers are named A, B,

C, D, and E (from left to right). In the right hand panel the decades are numbered from 1 to 10 and the steppers are named F, G, H, J, and K.

10.1. *Introduction*

The master programmer contains only program circuits, there being no numerical or common programming circuits. The program circuits will be divided into two types, namely, *stepper circuits* and *decade counter circuits* or *decade units*. The decade counter circuits are represented in FIGURE 73 by the ten rectangles along the top of the drawing. The five steppers are represented by the rectangles along the bottom. The decade counter circuits are divided into groups, each group being associated with a stepper. To give flexibility *decade associator switches* are provided which change a decade circuit from one group to another.

10.2. *Decade Counter Circuits (FIG. 73)*

10.2.1. *Decade Ring*

The decade rings used in the master programmer are ten stage ring counters located on plug-in units. The clear inverter (**Y1**) is also located on the same plug-in unit. The pulse standardizer and the carry circuits associated with the ring are on a separate plug-in unit. In fact, for each pair of decades the pulse standardizers (**Y2** and **Y3**) and carry circuits (**Y4**, **Y6**, **Y7** and **Y8**) are on one plug-in unit.

Provision is made for making static cable connections to any decade ring of the master programmer. This would enable the operator, for example, to register an independent variable in certain decades of the master programmer and to print it whenever desired.

The normally positive outputs of the stages of the decade ring go to the respective positions on the six decade switches, **Y72**. The common connection of each switch (**Y13**, etc.) connects to the grid of the inverter tubes **Y14**. If there is a coincidence between the setting of any decade switch and the position of the decade ring the corresponding inverter will be turned off. Since all the switches are illustrated as setting at "7" all the inverters would be turned off if the decade ring was stepped to stage seven.

The carry circuit.—Whenever a decade is stepped to stage "nine" the static output causes gate **Y6** to open. If another pulse is fed into the pulse standardizer the ring will step to zero and a pulse will pass gate **Y6** (or gate **Y4** for even numbered decades), go through the inverter and buffer **Y8** and thence to an association switch or, in some cases, directly to the input of the pulse standardizer for the next decade to the left.

The carry circuit is spread over parts of three plug-in units, and thus, necessarily has a very poor time constant. Actually, the rise time for the circuit comprised of stage nine of the ring and gate **Y6** on a separate plug-in unit (four times the time constant)—approximately the time for the signal to reach 97% of its maximum amplitude is on the order of one-half an addition time. Thus, any sequence of digit pulses which would produce a carry-over cannot be fed into the decades of a master programmer during any one addition time. There are other situations (see the discussion of clear circuits below) where digit pulses cannot be fed into these decades.

The clear circuits.—This ring is cleared by a CPP passing gate **Y16**, for example, and turning off the clear inverter (tube **Y1**) on the decade plug-in unit. This clear circuit is operated either by the initial clear gate arriving at the buffer **Y17**, say, or by the operation of one of the coincidence gates **Y18** in the stepper circuits (E). Generally, one of these coincidence gates will conduct when there is a coincidence between the position of the stepper ring, the settings of a number of decade switches and the position of the corresponding decade rings.

Since the clearing is accomplished by a CPP passing gate **Y16** (in decade 11) the decade cannot be stepped by any number of digit pulses (arriving over the direct input **11***di*) which will step it past a coincidence position. This restriction is not because of the time constants. Actually, for the clearing to take place the ring must come to (and stay on) the coincidence position (that is, the position corresponding to one of the decade switch settings) so that gate **Y19** is set up at pulse time 17; and pulse time 17 is some time (at least seven pulse time) after the last digit pulse arrived. In fact, *digit pulses should not* be used to step this ring to a coincidence position. The rise time of this clearing circuit (as well as the stepper clear circuits) is on the order of one-half an addition time (10 pulse times). Thus, the circuit can be expected to operate satisfactorily only when stepped to the coincidence position with a program pulse (CPP). Note that the time constant of these circuits vary considerably depending upon the positions of the association switches and the stepper considered.

Note that there is no provision for delayed carry-over (as in an accumulator). This means that two associated decades cannot be stepped simultaneously in a manner which produces a carry-over.

10.3. *The Stepper Circuits*

10.3.1. *The Stepper Ring*

The stepper contains a six stage ring located on a plug-in unit. On the same plug-in unit is a pulse standardizer and a set of inverter tubes connected to the outputs of the ring. The set of outputs of the ring which go through inverters go to two sets of six gates each, gates **Y18** and gates **Y21**. The other outputs of the stages of the ring go to the respective positions on the stepper clear switch. The common terminal of this switch goes to gate **Y22**. When **Y22** is open any pulse arriving from buffer **Y23** will clear the stepper back to stage one. The stepper will clear to stage one in the following cases:

(*a*) When the initial clear gate is applied, gate **Y24** opens letting through a CPP which turns the inverter **Y26** off clearing the ring.

(*b*) A pulse arriving over the clear direct input (*cdi*) turns the buffer **Y27** on and the inverter **Y26** off.

(*c*) If the stepper is set at stage five and the stepper clear switch is at five (as illustrated) the gate **Y22** will be open. A pulse passed by gate **Y19** or from the buffer **Y28** on the stepper direct input (*di*) will turn the inverter **Y29** off and the buffer **Y23** on. This will cause the inverter **Y31** to go off causing the gate tube **Y22** to conduct. This in turn causes the clear inverter **Y26** to go off and clear the ring.

The stepper clear circuit.—The stepper clear circuits will not operate in one pulse time (the rise time for this clear circuit is about one-half an addition time). This means that the stepper ring can be stepped with digit pulses only if the ring is not stepped onto the coincidence position (that is, onto the stage corresponding to the setting of the stepper clear switch).

The stepper direct input.—A direct input (through buffer **Y28**) is provided to step the stepper ring. In this case the associated decade units ring is not stepped and no output program pulse is obtained. Note (above) the restrictions on the kinds of pulses supplied to this input.

The stepper input.—The flip-flop **Y32** and the associated gate **Y33** has a time constant approximately equal to that of the slow buffer output of a transceiver. This means that this input (E_I for example) must never be pulsed later than pulse time four. That is, it can be pulsed by a CPP, 9P, 1P, 2P, or 2'P; but not by 4P, 1'P, or generally by any digit output of an accumulator.

Note that if E_i and E_{cdi}, for example, are pulsed simultaneously, the stepper will clear first and the output pulse will be from E_1o.

10.3.2. *The Program Transmitters*

In the lower right hand corner of the rectangle (FIG. 73–D) containing the stepper circuits there are six gates **Y21** and six standard transmitters **Y34**. One of these

gates will be open depending upon the position of the stepper ring. Any pulses arriving from the buffer Y36 will be transmitted through one of these channels. In the illustration the stepper is setting at stage one so any pulses from Y36 will be transmitted through the left hand gate Y21 (1) and will appear on the output terminal E_1o. Note that a lead Y37 comes from the master programmer clear (MPC) to all these gate tubes. This lead goes to the screens of the gate tubes. Whenever the initial clear is activated a relay located in the initiating unit changes these screen voltages from 150 to 0 volts. This blocks these gates, that is, even if a signal arrives on both control grids the tube will not conduct. As explained in Section 2.1.2., the effect of the initial clear is to clear decades back to their first stages and let the program circuits run out their sequences. By program jumpers various program controls in the machine may be connected in a sequence that will take several hundred addition times to run out. These sequences may be tied together by the master programmer so they would take a very long time to run themselves out or even repeat indefinitely. To prevent this tying together and, thus, make the time for initial clearing reasonably short the output gates in the master programmer are blocked in this manner. A period of about one half second will be sufficient (including a safety factor) for any possible sequence set up in the other units of the ENIAC to run out, and, therefore, the initial clear lasts for approximately one half second.

10.3.3. *The Program Receiving Circuit*

The input program will ordinarily come in by the terminal E_1 causing the buffer Y38 to go on setting the flip-flop Y32. The output then takes a positive swing opening gate Y33. The next CPP is passed resetting the flip-flop and turning off the inverter Y39. This causes the cathode follower Y36 to go on giving a positive pulse to the grids of the gates Y21. This also turns the buffer Y41 on giving a negative pulse to the pulse standardizer of decade 11.

As described above, 10.3.2, one of the six gates Y21 is open depending upon the position of the stepper. Thus, for every pulse put into E_1 a pulse is sent into decade 11 and a pulse comes out of one of the terminals E_1o to E_6o one addition time later.

Pulses fed into E_1i cause the stepper to step, and pulses fed into $11i$ cause the decade to step. Neither of these causes any pulses to be given out at the outputs E_1o to E_6o.

10.3.4. *The Coincidence Gates*

The coincidence gates are tubes Y18 for stepper E. Whenever any one of these gets a signal on both grids the inverter Y42 goes off and the gate Y19 is opened. This passes the next CPP to the inverter Y29 and the buffer Y23. The output of Y23 goes to the pulse standardizer Y43 stepping the ring and it also turns the inverter Y31 off. If the gate Y22 is open the clear signal from Y26 safely overrides the stepping signal from the pulse standardizer and the ring clears back to stage one. Also, a pulse on the clear direct input (E_{cdi}, Y27) or a CPP passed by gate Y24, when initial clear is activated, will safely (that is with adequate safety factor) override any stepping signal.

The output of the stepping gates also goes to the clear circuits in the decade counter causing the decade to clear back to zero. Again, this clear signal overrides any stepping signal.

Stepper E, with the decade associator switch for decade 12 setting has illustrated, as only one decade associated with it. Consider stepper D. This stepper has decades 12 and 13 associated with it. Looking at stepping gate Y44 (1) it is seen that one of the grids connects to both the inverter Y14 (1) of decade 13 and, through the D—E associator switch, to the corresponding inverter Y14 (1) of decade 12. If either inverter is conducting the grid on Y44 (1) will be sufficiently negative to prevent it from conducting. This constitutes a multiple coincidence arrangement. That is, in order for Y44 (1) to conduct three inverters must go off, namely Y14 (1) of decades 12 and 13 and Y46 (1) in the stepper ring unit. Consider stepper C. If five decades are associated with stepper C then in order for any stepping gate (not shown) to conduct the inverter in the stepper ring unit must go off along with the five inverters in the respective decade units.

Steppers A (FIG. 73-B) and F (not shown) may be used without any associated decades. When the A—B association switch Y12 (or the F—G) sets at B (or G) the screens of the coincidence gates (e.g., Y47) are switched from 150 to 0 volts. This prevents any of these gates from conducting, and thus, gate Y19 of A never conducts. This means that the stepper ring can be stepepd only by pulses introduced over the direct input. The stepper clear direct input functions as before. Any pulses arriving over the program input will be transmitted over one of the six outputs depending upon the position of the stepper ring.

Any of the other steppers may be made to operate in the above manner by removing the gate Y19 in the plug-in unit. Note, that the only difference in the operation of these other steppers (as compared to A or F) is that certain decades will count the pulses coming in on the stepper program input. These decades will clear at positions depending upon the settings of the decade switches but there will be no corresponding change in the stepper position. This clearing could be prevented and, thus, the total number of program pulses counted by removing the coincidence gates (Y44, for example) instead of gate Y19.

10.4. *Association Switching*

All the decade units are exactly alike, and the stepper units only differ with respect to the number of decades that can be associated with each one. FIGURE 73 shows that decade 12 can be associated with either stepper D or E. Decade 14 can be associated with either C or D, decade 18 with either B or C, and decade 20 with either A or B. When decade 20 is associated with stepper B then stepper A has no associated decade (see above).

The decade associator switch Y12 is a nine pole double throw switch. The six poles on the left handle the outputs of the inverters associated with the decade switches. The seventh pole takes care of the clear circuit, the eighth the input to the next decade on the left, and the ninth the input of the decade to be associated. In the case of decade 20, since there is no decade to the left, the eighth pole takes care of the input to decade 20, and the ninth pole is used to change the screen bias of the coincidence gates.

Consider the associator switch for decade 12. As illustrated this decade is associated with stepper D. The following table illustrates what happens for the two positions of the associator switch for decade 12:

TABLE 10-1

	Associated with D	Associated with E
Outputs of the inverters Y14 of decade 12.	Go to stepping gates Y44.	Go to stepping gates Y18.
Decade clear input (to Y43).	Goes to the output of the stepping gates Y44.	Goes to the output of the stepping gates Y18.
Input to decade 13....	Goes to the carry over circuit of decade 12.	Goes to the buffer Y41 of stepper D.
Input to decade 12....	Goes to the buffer Y41 of stepper D.	Goes to the carry over circuit of decade 11.

Thus, when decade 12 is associated with stepper E, decade 11 acts as a units decade and 12 as a tens decade in counting the number program pulses coming in at the terminal E_1. Therefore, the two decades can

TABLE 10-2.—PROPERTIES OF MASTER PROGRAMMER INPUTS

t=addition time when terminal is pulsed unless otherwise noted.
s=stage of stepper counter before a pulse is received.
d_s=number set up on decade switches associated with stage s of stepper counter.
c=number set up on stepper clear switch.

Input Terminal	Pulse Input	Effect of Reception of a Pulse	Addition Time Effect Occurs
Stepper Input	Program pulse at end of add. time t or PM pulses during add. time t+1.	1. Output pulse is transmitted through output terminal corresponding to stage s of stepper counter. 2. Decade counters cycle 1 stage in units place 3. If input cycles decade counters d_s: (a) decade counters clear to zero (b) stepper counter cycles to (s+1) mod c	t+1. t+1. t+2. t+2.
Stepper Input A or F with decades dissociated.	Program pulse at end of add. time t or PM pulses during add. time t+1.	1. Output pulse is transmitted through output terminal corresponding to stage s of stepper counter. 2. (No decade counters) 3. (No decade counters)	t+1.
Stepper Direct Input	Digit or program pulse	1. No output pulse is transmitted 2. Decade counters do not cycle 3. Stepper counter cycles 1 stage for each pulse received	Immediately.
Stepper Direct Input A or F with decades dissociated.	Digit or program pulse	1. No output pulse is transmitted 2. (No decade counters) 3. Stepper counter cycles 1 stage for each pulse received	Immediately.
Stepper Input	Program pulse at end of add. time t.	1. Output pulse is transmitted through output terminal associated with stage (s+p) of stepper counter.	t+1.
and Stepper Direct Input	Program pulse at end of add. time t or p digit pulses during add. time t+1.	2. Decade counters cycle 1 stage in units place 3. Stepper counter cycles 1 stage for each pulse received at stepper direct input terminal. 4. If decade counters are cycled to stage d_{s+p}: (a) decade counters clear to zero (b) stepper counter cycles to (s+p+1) mod c	t+1. Immediately. t+2. t+2.
Stepper Input	Program pulse at end of add. time t.	1. Output pulse is transmitted through stage (s+p) mod c	t+1.
and Stepper Direct Input A or F with no decades.	Program pulse at end of add. time t or p digit pulses during add. time t+1.	2. (No decade counter) 3. Stepper counter cycles 1 stage for each pulse received	Immediately.
Decade Direct Input	Program pulse	1. No output pulse is transmitted 2. Decade counter cycles one stage 3. If decade counters are cycled to stage d_s: (a) decade counters clear to zero (b) stepper counter cycles to stage (s+1) mod c	Immediately. t+1. t+1.
Stepper Clear Direct Input	Program pulse or digit pulses	1. Stepper counter clears to stage 1	Immediately.

count as many as 99 pulses coming in at E_1. When decade 12 is associated with stepper D, decade 11 acts as a units decade in counting the number of pulses coming in at E_1 and cannot count more than 9 pulses. In this case decade 12 acts as a units decade in counting the number of pulses coming in at D_1.

Consider stepper C. If both decades 14 and 18 are associated with stepper C then the five decades (14 to 18) can count as many as 99,999 pulses arriving at terminal C_1.

10.5. *Programming the Master Programmer*

One aspect of master programmer control is provided by the switch settings (decade associator, decade, and stepper clear). The other aspect is the input terminal (decade direct, stepper, stepper direct, or stepper clear direct) which is pulsed. Table 10-2 summarizes the properties of the master programmer inputs.

It is to be noted that in the master programmer, each stepper with its associated decades functions as a unit independently of the other steppers and decades. For this reason, it is possible to stimulate some or all of them simultaneously.

It is even permissible to pulse more than one of the input terminals of a given stepper-decade combination simultaneously. For example, a decade direct input terminal and a stepper input terminal may be pulsed simultaneously because the cycling of the decade counters due to the former is completed before that due to the latter begins. A stepper input and stepper direct input terminal may also be pulsed simultaneously because the latter affects only the stepper counter and does so immediately while the former affects the decade and, if it affects the stepper counter, does so two addition times after the input. On the other hand, the stepper direct input should not be pulsed two addition times after the stepper input or one addition time after a decade direct input because of the conflict that would arise if the decade counters were thus cycled to the settings of the decade switches.

XI. THE TRANSMISSION SYSTEM AND SPECIAL DEVICES

This chapter contains a definition, and some description of the digit and program trunks which carry the pulses representing digits or program signals from one unit to another; also various special devices such as shifters, deleters, adapters, static cables, and so on.

11.1. *Trays and Trunks*

It is necessary to transmit pulses representing digits or program signals from one unit of the ENIAC to another. Furthermore, this must be done in an entirely different manner for each new problem that is put on the ENIAC. Thus, the interconnection systems must be very flexible. For this purpose trays and jumpers are used.

11.1.1. *Trays*

A tray is essentially an eleven wire transmission line, capable of being connected to other trays and to the digit terminals and program terminals of the various units.

A detailed description of both digit and program trays has been given in 4.2.7.

These trays are stacked on the front of the various units of the ENIAC, some above and some below the program control panels. Generally, the program trays will be placed below the control panels and the digit trays will be placed above. There is room for about twelve trays to fit above and twelve below the control panel of a unit, although a much smaller number will ordinarily be sufficient.

11.1.2. *Jumpers*

Cables or jumpers are used to connect the trays to the digit terminals and program terminals. There are two kinds of jumpers. One, a program jumper, consists of a single wire and ground and is used to connect a socket on a program tray to a program socket on one of the units. The other, a digit jumper, has eleven wires and a ground and is used to connect an outlet on a digit tray and to a digit terminal of a unit. This last type of jumper is also used to connect trays together.

11.1.3. *Trunks and Lines*

A single wire and ground, running through several program trays, jumpers or program cables and thus connecting a number of program terminals to one another, is called a *program line*. A set of eleven wires and ground used to transmit a ten-digit number and its sign and running through several digit trays, jumpers or cables, is called a *digit trunk*.

One set of digit trays (9) are connected together to form the cycling unit trunk. This carries the various pulses and gates produced by the cycling unit around to the various units of the ENIAC. Nine trays are sufficient here since the printer does not connect to this trunk.

11.1.4. *Load Boxes*

Each wire of a digit trunk and each program line has one load resistor connected to it. These resistors are assembled in boxes, and one box is to be plugged into an otherwise unused outlet at the end of one of the end trays of each set connected together by jumpers. This makes it possible to have the flexibility of being able to connect varying numbers of digit and program terminals to the trunks and program lines.

11.1.5. *Load Units*

The pulses and gates transmitted over the trays must have rise times better than ½ microsecond. This sets an upper limit to the value of the time-constant, RC, where R is the equivalent resistance of the transmitter, and C is the capacity of the trays and interconnector cables. The value of R has been made low by using two triodes (pentodes connected as triodes) in parallel, with the load in the cathode circuit. To lower it further would require more tubes and appreciably more power. It is therefore necessary to design the trays and connecting cords so that the maximum C to be driven is never larger than 5,000 micromicrofarads. Capacities from one line to another must be kept to a small fraction of the capacity to ground, in order to avoid cross-talk effects.

The flexible shielded cable which is available for use in making interconnection cables has a capacity of about 30 micromicrofarads per foot. If each cable is three feet long, and 30 such cables are used on a given trunk line, the capacity thus added may be of the order of 3500 mmfd. This leaves no more than 1500 mmfd. capacity for the trays and their short interconnection cables or jumpers. If eight trays are used, a tray and its jumper must have a capacity less than 200 mmfd. Since an eight foot length of shielded cable would have more than this, it is not possible to use this for running digit trunks and program lines the length of the ENIAC. Special coaxial lines would not only be expensive, but would excessively complicate the job of connecting in the sockets which are to occur every two feet.

The tray design which has been adopted is nearly equivalent to a coaxial line with convenient openings every two feet. The shielding is not perfect, but cross-talk is reduced to less than five percent for even the worst combination of conditions. The maximum cross-talk then amounts to a two-volt pulse, which can have no effect since it is applied to the grid of input tubes biased at −20 volts, with cut-off at −8 volts.

Clearly, there canont be too many jumpers connected to a particular digit trunk or program line or else the capacity given above would be exceeded. To assist the operator in determining the maximum safe loading the following term is introduced.

One load unit is a capacity of 160 micromicrofarads. The following devices will each be called one load unit:

(1) *A program or digit cable.*—If the cable is only three feet long, it will account for about 90 mmfd. The balance is allowed for the portion of the circuits which will be internal at the particular panel to which the cable is connected.

(2) *A tray and its short jumper* for connecting the next tray. The tray accounts for about 120 mmfd. and the balance easily accounts for the jumper.

The standard transmitters used on the regular program and digit outputs (not certain multiplier and divider outputs) are designed to transmit into a line containing *not more than 60 load units.* Actually program transmitters can transmit into as many as 120 load units with the usual 2:1 safety factor. (The reason for this is the difference in shape of the CPP as compared to the 10P.)

11.2. *Deleters*

A deflector is usually used to delete non-significant figures, and is therefore used on the add or subtract output digit terminals. Various types of deleters and the connections made in each are illustrated in FIGURE 74. A deleter merely open-circuits the lines corresponding to unwanted digits. Note that when a deleter is used on the output of an accumulator the significant figure switch should be set to the number of figures not deleted. In this case, the subtract pulse well be sent out over the line belonging to the significant figure furthest to the right, next to the deleted digits. Thus, the subtract pulse is not deleted.

11.3. *Shifters*

A shifter is used to shift the digit lines to either the right or the left, and is placed on the input terminals of an accumulator. Thus, a shifter is generally used to multiply by powers of 10. An example of +2 and a −2 shifter are given in FIGURE 75.

A+ shifter.—A shifter multiplies by positive integral powers of ten. In the case of a +2 shifter (FIG. 75) any pulses arriving over the units channel (terminal 1 of the socekt "S") goes to terminal 3 (hundreds) of the plug (P). The plug is inserted in the input digit terminal of the accumulator. Note that terminals 9 and 10 of the socket are not connected and that terminals 1 and 2 of the plug are connected to ground. This grounding prevents the grids of the corresponding input gates from picking up any cross-talk or other noise.

A− shifter.—The − shifter multiplies by negative integral powers of ten. In this case, the unused terminals of the socket (see FIG. 75) are not connected but the unused channels of the plug "P" must be fed with nine pulses in case of a negative number in order to give the proper complement. Thus, if M99430 is mutiplied by one tenth the result is M999430. Thus, the PM line (terminal **11** on S) must be connected to terminals **9**, **10**, and **11**, on P in the case of a −2 shifter. An adapter of this type *must be used on the input* to an accumulator since otherwise the PM transmitter would have to drive three different digit lines instead of just one digit line and three grids of the input gates to the accumulator.

11.4. *Pulse Amplifier Unit*

A pulse amplifier unit consists of eleven standard transmitters which interconnect to trunks. Since the buffer unit transmits in only one direction, two units would be needed to completely interconnect two trunks. In counting the load units on a particular digit trunk, for example the input to the buffer unit counts as only one load unit and since the buffer unit contains its own transmitters none of the load units of the trunk transmitted into count as being on the first trunk. Thus, these buffer units allow the operator to practically double the number of units which may be connected together via a digit trunk system.

The buffer units are designed to sit on top of a group of program or digit trays. The units contain their own transformers for supplying the heater voltages. The D.-C. power and the A.-C. power for the heaters is furnished by sockets located near the floor between accumulators nine and ten and between accumulators fourteen and fifteen.

11.5. *Static Outputs*

Each decade and PM unit of every accumulator has a static output socket, accessible from the back. To avoid capacity loads on the counter circuits, a large resistance is placed in series with each static output line. The time constant thus introduced into the static output circuits is large enough so that one addition time must be allowed for the operation of other circuits from these outputs. However, because the system is a static one, there is no cross-talk problem, and unshielded wires can be used for the static cables.

Static cables are used to interconnect units in the following cases:

(1) To connect the multiplier and multiplicand accumulators to the multiplier.

(2) To connect certain accumulators and perhaps certain decades of the master programmer to the printer.

(3) To connect the PM unit of the numerator and denominator accumulators to the divider.

11.6. *Special Devices*

11.6.1. *Special Program Jumpers*

As well as the regular program jumpers described in Section 11.1.2 there are *loaded program jumpers* and **Y** *program jumpers.*

A loaded program jumper is to be used when connecting one program output directly to another program input. The jumper is physically characterized by having an extra long plug at one end which contains the built-in load resistor. Such a jumper must *never* be used in connection with a program line which enters a tray system which has its own load box.

A Y-program jumper is a jumper with three plugs attached. It is used to connect two nearby program terminals (input or output) to the same program line. It has no built-in resistor so one connection *must* go to a program tray system which has a load box.

11.6.2. *Accumulator Interconnection Cables*

There are special interconnection cables and load boxes for use with accumulators which determine whether they act as ten digit accumulators or whether two accumulators act as a twenty digit accumulator.

11.6.3. *Multiplier Interconnection Cables*

The multiplier interconnection cables fall into two classifications. First, those that connect the multiplier to its associated accumulators, and secondly, those that interconnect the three multiplier panels. In the latter classification, damage to circuit elements and short circuits across the power supply may be caused by erroneously plugging a cable into the wrong socket. This possibility is avoided by removing prongs from plugs, and filling corresponding socket holes (where not used) in such patterns that erroneous connections are impossible.

Reference should be made to the following diagram:

Interconnection of High-speed Multiplier with Associated Accumulators---------- FIGURE 43

11.6.4. *Divider Interconnection Cables and Adapters*

Since the divider and square rooter serves largely to program its associated accumulators, those interconnections which must be established between the two units mentioned for the purpose of communicating program instructions are made through cables as illustrated in FIGURE 47, which drawing makes further reference to special cables and adapters used.

11.6.5. *Function Table Adapters*

In order to disconnect the 9P gates from the synchronizing trunk line carrying the 9P, and to connect these gates to the line carrying the CPP in the same trunk, an adapter is used. This adapter is connected where the synchronizing pulse trunk plugs into the back of panel No. 2 of the function table.

11.6.6. *Other Adapters*

The remaining adapters may be classified as: (1) special digit adapters, (2) digit-program adapters, and (3) printer adapters.

The first group consists of adapters which combine shifting and deleting characteristics and are made up in obvious fashion in accordance with the combination desired.

The second group serves to make possible the use of digit trays as program trays. Each adapter consists of a box with a 12-prong digit plug at one end, connected to a mounted group of 11, two-opening program sockets at the other. These correspond to the 12-prong sockets in the digit trays, and the two-prong plugs on program cables.

The third group consists of two adapters. Adapter A connects the static output of stage M (of the printer interconnection cable to accumulator or master programmer decade counter stages) to the PM lead in each of two static output cables. Adapter B is used when no connection is desired to the PM lead in the static output cables.

By the use of the term "electronic" in such expressions as "electronic means" and "electronic speeds" we intend the ordinary meaning of these expressions as is now customary in the art, and particularly to differentiate our device from any devices which may employ or include mechanical elements for performing analogous functions. This is considered to be in practice a difference in kind rather than one of degree, since mechanical elements have substantial inertia which reduces the order of attainable speeds or frequencies to a point thousands of times slower than those attainable by electronic means. This difference, in practice, causes the problems involved to be so distinct, and the skills required in their solution to be so unrelated, that entirely different training and education are involved in the two fields, as is common knowledge.

By the term "arithmetical operations" as used in the following claims, we means the ordinary operations of arithmetic including addition, subtraction, division, multiplication and the extraction of square roots.

We claim:

1. Means for producing electric pulses in sequence, electronic means for alternately transmitting certain ones of said pulses as recurrent differentiated groups, electronic means for selecting particular pulses from one of said differentiated groups to represent quantitative values, electronic means for selecting particular pulses from another of said differentiated groups to represent certain qualitative values, reading means responsive to pulses representing both the qualitative and quantitative values for reading data to be processed upon command of at least one of said qualitative pulses, storing the data thus read, and making the data available in the form of data pulses in response to at least one other of said qualitative pulses, and electronic means for receiving said data pulses and responsive thereto for performing electrical switching operations of a nature determined by selected ones of said qualitative values and of a degree determined by selected ones of said quantitative values.

2. The invention as recited in claim 1, in which the first-named means produces a series of equally spaced pulses; in which the first-named electronic means divides said series of pulses into two differentiated groups with at least one pulse recurring intermittently forming one group, the other group comprising the intervening pulses; and each of the third and fourth electronic means utilizing all of the pulses of their respective groups to represent certain values.

3. Means for producing electric pulses in sequence, elec-

tronic means for transmitting certain of said pulses as recurrent differentiated groups, first means for selectively producing particular pulses from said differentiated groups to represent quantitative values, second means for selecting pulses from said differentiated groups as control pulses to initiate certain control operations, a plurality of electronic means each arranged, upon stimulation, to perform a particular manipulation upon quantitative values represented by certain of said pulses, and a plurality of pulse-controlled electronic switching means each associated with a particular one of said manipulation-performing means for energization of same and arranged to be immediately available for selective stimulation by any one of said control pulses to initiate performance selectively of any one of said manipulations.

4. The invention as recited in claim 3, including quantitative-pulse-responsive means for storing selected ones of said quantitative values, and means responsive to said control pulses for actuating said storage means.

5. The invention as recited in claim 4, including means to control pulses for transmitting from any of said storage means pulses corresponding to the stored quantitative values.

6. The invention as recited in claim 5, including electronic switching means operable by said control pulses for routing said transmitted quantitative values to any of said manipulation-performing means.

7. Means for producing recurrent groups of coded electric pulses which comprise a plurality of stages of electronic flip-flop devices serially arranged as a stepping device to be responsive to input pulses to step said stepping device by actuating a successive stage for each received pulse, means for deriving an electric pulse from each said stage when it is actuated, said stages being serially ring connected to form an endless chain for cyclical operation, means for producing uniformly spaced pulses, means for conducting said pulses to said stepping device, a conductor, and means included in said first named means for deriving a signal from each stage of said stepping device when said stage changes its condition of actuation, and responsive to said signals for selectively controlling the electrical connection of particular ones of said last-named pulses to said conductor to produce cyclically recurrent groups of pulses coded in accordance with said selection.

8. In an electronic computing system a multiplicity of pulse responsive units constructed to receive numbers pulses having numerical significance and to receive control pulses having definite control characteristics, means to transmit to said units control pulses and numbers pulses in a correlated order including means to establish a selective relation between certain control pulses and certain predetermined units, said units being constructed to receive numeratively numbers pulses when stimulated by a control pulse, certain of said units being constructed for arithmetic operations and including means responsive to terminal arithmetic operation therein to transmit a control pulse effective on predetermined units for intercommunication of numerical content between one and another of said units.

9. An electronic computing machine comprising arithmetic units of respective numerating functions, means to transmit thereto numerical data and distinctly characterized control signals in pulse signal form, said units being constructed to receive such pulses, and being also responsive to individually characterized control signals to perform respective arithmetic operations on numerical data so transmitted thereto, means included in each said unit to emit pulse signals significant of the numerical result of respective arithmetic operations completed therein, and means included in each of certain at least of said units responsive to completion of respective arithmetic operations in said units to emit one at least of said control signals, characterized significantly in relation to the integration of results from two or more said units.

10. The machine of claim 9 wherein certain of said control signals are characterized so as to stimulate selectively certain of said units in synchronism with a predetermined instant of time related to the arithmetic functions of two or more of said certain units last named, whereby the numerical result in one will be transmitted to at least one other and the latter caused to integrate its contained data and the communicated data.

11. The machine of claim 8 wherein said units are constructed to receive pulses of numerical significance only when stimulated by a pulse specially characterized in relation to such unit and its receptive function, and wherein said units are constructed to emit signals significant of arithmetical content only when stimulated, and means to transmit pulses coordinated temporally with at least two of said units to stimulate such units coactively.

12. The structure of claim 8 in which the said means to transmit said pulse signal forms includes means to generate within each of successive operation periods of arbitrary duration, a frame of discrete pulses having a basic pulse frequency which is submultiple of the duration of the frame in transmission, including a succession of pulses of numerical significance and control pulses differently timed within said frame, said transmission means including also coincidence devices in each of said units constructed to receive pulses of said frame, whereby said coincidence device are partially stimulated by such received pulses, and means to transmit control pulses selectively in relation to said units timed selectively with respect to certain pulses of numerical significance in said frame to complete the stimulation of respective coincidence devices, said coincidence devices being responsive to such completed stimulation to emit a pulse to an internal element of the respective unit for arithmetic operation of such unit therewith.

13. The structure of claim 8 in which the said means to transmit said pulse signal forms includes means to generate within each of successive operation periods of arbitrary duration a frame of discrete pulses having a basic pulse frequency which is a submultiple of the duration of the frame in transmission, including a succession of pulses of numerical significance and control pulses differently timed within said frame, said transmission means including also coincidence devices in each of said units constructed to receive pulses of said frame, whereby said concidence devices are partially stimulated by such received pulses and means to transmit control pulses selectively in relation to said units timed selectively with respect to certain pulses of numerical significance in said frame to complete the stimulation of respective coincidence devices, said coincidence devices being responsive to such completed stimulation to emit pulse to an internal element of the respective unit for arithmetic operation of such unit, therewith, said frame of pulses including ten successive digit pulses for decimal digits and cipher, each pulse being at a given part of a respective pulse interval in said frame, and nine successive nines pulses in the same intervals as the last named digit pulses but out of phase therewith, and means to stimulate said units in coincidence alternatively with either the said digit pulses and the nines pulses.

14. In a device of the character described, a cycling device constructed to form and transmit intermittently a frame of discrete pulse signals of respective significant characteristics, a conductor means, a plurality of pulse responsive devices capable of predetermined arithmetic functions in response to predetermined ones of said pulse signals communicated thereto, said pulse responsive devices operatively associated with said conductor means in controlled normally non-responsive relation to certain at least of the pulses of said frame, said pulse responsive devices constructed to respond selectively to control pulses delivered thereto to function in accordance with particular pulses of said frame of pulses, means to form and transmit control pulses selectively to said pulse responsive de-

vices at respective times particular to the occurrence of predetermined pulses of said frame of pulses and in a mutual relation coordinated with a desired final output of pulses appropriate to the mutual significance of some at least of the pulse signals of said frame of pulses which have been next last effective at said pulse responsive devices.

15. The structure of claim 14 in an electronic computer wherein the said frame of pulses includes at least a number of pulses of numerical significance, said control pulses being selectively timed for each pulse responsive device to coincide with pulses of predetermined digit value in said frame, and said pulse responsive devices being constructed to perform arithmetical functions in response to such coincident pulses of the frame.

16. The structure of claim 14 in an electronic computer wherein the said frame of pulses includes at least a number of pulses of numerical significance, said control pulses being selectively timed for each pulse responsive device to coincide with pulses of predetermined digit value in said frame, and said pulse responsive devices being constructed to perform arithmetical functions in response to such coincident pulses of the frame, and wherein pulses in said frame other than those of numerical significance, are characterized individually in respect to function times of the apparatus, including control pulses.

17. The structure of claim 14 in an electronic computer wherein the said frame of pulses includes at least a number of pulses of numerical significance, said control pulses being selectively timed for each pulse responsive device to coincide with pulses of predetermined digit value in said frame, and said pulse responsive devices being constructed to perform arithmetical functions in response to such coincident pulses of the frame, and wherein pulses in said frame other than those of numerical significance are characterized individually in respect to the duration of particular function operations of the apparatus, and include control pulses effective on other like apparatus and also control pulses having special functional relation to other apparatus effective when coincident with other control pulses of correlated limited characteristics.

18. The structure of claim 14 in an electronic computer, wherein the said frame of pulses includes a series of pulses serially transmitted at a standard pulse time, which is a submultiple of the duration of transmission of said frame of pulses, and pulses of other arithmetic significance in the pulse times of said series on several respective conductors.

19. The structure of claim 14 in which certain of said pulse responsive devices are assigned and constructed for characteristic arithmetical functions associated respectively with positive and minus values, and said control pulses include positive and minus control pulses selectively related to units for said characteristic arithmetical functions.

20. In an electronic final signal system, a cycling device constructed to form and emit discrete signal pulses of respective significance, a bus conductor in conducting relation to said cycling device to transmit said pulses, a plurality of pulse operated devices capable of receiving and transmitting any of said pulses, arranged in receiving relation to said bus conductor and normally in controlled non-responsive relation to said pulses, said pulse operated devices including means to respond to control pulses selectively delivered to the pulse operated devices to energize the latter to respond to selected related ones of said signal pulses and to transmit a signal appropriate to the significance of the selected signal pulses and their order, means to form and transmit to said pulse operated devices control pulses at times related with the occurrence of said pulses and in a relation coordinated with a desired sequence of operations thereby to effect said transmission.

21. The structure of claim 20 in which said signal pulses comprise frames of pulses that include pulses of numerical significance by their sequence in said frame as transmitted, and other pulses of partial functional characteristics similar to those of said control pulses, whereby to energize said pulse operated devices when related with certain said control pulses first named.

22. In an electronic final significant group signal output system, a pulse generating unit constructed to form and transmit a complete frame of discrete signal pulses of respective significance, a bus conductor in conducting relation to said pulse generating unit to transmit said pulses, a plurality of pulse operated devices capable of receiving and transmitting any of certain pulses of said frame of pulses and arranged in receiving relation to said conductor normally in controlled non-transmitting condition in relation to said frame of pulses, said pulse operated devices being responsive to distinct respective control pulses to transmit pulses of said frame of pulses, and means to form and transmit to said pulse operated devices selectively respective control pulses at times selectively related to the occurrence of said frame of pulses and in a mutual relation coordinated with a desired sequence of operations and circuits associated with said means to transmit a final signal group appropriate to the numeration significance of all of the transmitted pulses of one or more of said frames.

23. The structure of claim 22 wherein said frame of pulses includes numerically significant pulses and functionally significant control pulses, the last named having a cooperative value in relation to certain signal pulses to affect the nature of the operation of said pulse operated devices.

24. The structure of claim 22 wherein said frame of pulses includes numerically significant pulses and functionally significant control pulses constituting at least a part of said means to form and transmit control pulses.

25. In an electronic computer, a multiplier unit comprising a multiplication table conductor gridwork having coupling resistances connecting selected intersections thereof in a predetermined pattern, gates at the leads to respective ones of those conductors which extend in one direction in said gridwork responsive to coinciding pulses, means to transmit gate pulses commonly to the gates to partially stimulate all of said gates within a predetermined time interval, gates at the leads to respective conductors extending across the last named conductors responsive to coinciding pulses, means to pulse the last named gates simultaneously to partially stimulate the same in the same said time intervals as the first named pulses, and means to transmit digits pulses of a multiplier and a multiplicand selectively to the first named and second named gates respectively in coincidence with the times of said partial stimulations and of potential constituting the remainder at least of the operating potentials respectively of the first and second named gates.

26. An electronic computing system comprising in combination a plurality of arithmetic units responsive to control pulses entered therein to receive and operate computatively with coincident pulses of numerical significance, means to establish routines of mathematical procedure and numerical information comprising constants of a problem as pulse signals and to transmit the same in a sequence to said system as a whole problem, each of certain of said signals individually characterized in relation to the part of a routine which a given part of the system is required to perform and each of other certain signals being individually characterized in its functional effect in the system in relation to a given numerical value, said system being constructed to transmit said data at electronic speeds to and between one or more units of the system in a predetermined order according to the characterization of the pulses, to one or more of said units of the system serially or simultaneously according to said characterization of control pulses, and means to initiate a sequence operation of the system responsive to said control pulses, including means to inhibit communication to said units of any of said composition of pulses, yieldable to coincidence of special control pulses related to the condition of operation of said system and units, and respon-

sive selectively to an initial one of said special control pulses, and to respective ones of said special control pulses, said units being constructed to emit certain at least of said special control pulses effective on otherwise uninhibited units and to emit pulses of numerical value significant of a content of the emitting unit.

27. In an information processing system, a first information accepting device having the property of performing a predetermined operation on entries therein, a second information accepting device having the property of performing a predetermined operation on entries therein, a third information accepting device having the property of performing a predetermined operation on entries therein, an information exchange bus system, normally inoperable input and output devices linking each of said information accepting devices with said information exchange bus system, first and second control stimulus generators associated respectively with said information accepting devices and supplying a control signal at the termination of the respective operation performed by said information accepting devices, an operative connection linking the output of said first control stimulus generator with the input device feeding said second information accepting device, an operative connection linking the output of said second control stimulus generator with the input device feeding said third information accepting device, and apparatus selectively conditioning said output devices for operation.

28. In an information processing system, a first information accepting device having the property of performing a predetermined operation on entries therein, a second information accepting device having the property of performing a predetermined operation on entries therein, a third information accepting device having the property of performing a predetermined operation on entries therein, an information exchange bus system, normally inoperable input and output devices linking each of said information accepting devices with said information exchange bus system, first and second control stimulus generators associated respectively with said information accepting devices and supplying a control signal at the termination of the respective operation performed by said information accepting devices, an operative connection linking the output of said first control stimulus generator with the input device feeding said second information accepting device, an operative connection linking the output of said second control stimulus generator with the input device feeding said third information accepting device, recycling apparatus in one of said information accepting devices responsive to control signal input thereto for repeating said predetermined operation, and apparatus selectively conditioning said output devices for operation.

29. In a date processor adapted for iterative operation in the solution of problems, a first re-entrant information data processing loop characterized by the performance of a plurality of modifications on information appearing in coded pulse form passing therethrough during each passage in an iterative operation, a second open information path, apparatus comparing information circulating in said first loop with reference data, and an information flow governing device transferring the contents of said loop into said second path and interrupting the flow of information around said first loop under the control of said comparing apparatus to thereby terminate said iterative operation.

30. In apparatus for storing and reproducing numbers, a counting register, a signal transfer link conditioned for transmission by passage of said counting register through a predetermined state, a source of continuously repeated pulse groups separated by more than two pulse times, a gate adapted to deliver a single pulse group to said counting register, a connection between said source and said signal transfer link, and an output memebr excited from said signal transfer link.

31. In apparatus for storing and reproducing numbers, a counting register, a signal transfer link conditioned against transmission by passage of said counting register through a predetermined state, a source of continuously repeated pulse groups separated by more than two pulse times, a gate adapted to deliver a single pulse group to said counting register, a connection between said source and said signal transfer link, and an output member excited from said signal transfer link.

32. In computing apparatus, a first number storage register, a second number storage register, a function table representing partial product values in a predetermined number system, apparatus impressing the contents of said first and second storage registers on said function table, means for combining the resultant partial products, and means for adding a term controlled by the contents of one of said registers to such combined partial products.

33. In computing apparatus, a first number register, a second number register, a cycling unit developing control pulses devoted to the exertion of control functions, a third number register, information interchange apparatus linking said first, second and third number registers, said control pulses acting on said information interchange apparatus initially to effect a one of addition and subtraction operations selectively of the number in said first register with the number in said second register and enter tallies in said third reigster, and sign sensing apparatus responsive to the sign of the remainder for altering the information interchange apparatus to effect the other one of the addition and subtraction operations in response to overdraft.

34. In information processing apparatus, a first information processing device, a second information processing device, a first control device associated with said first information processing device and initiating operation thereof in response to an input stimulus and emitting a first output stimulus in response to completion of the operation of said first information processing device, and a second control device associated with said second information processing device and initiating operation thereof in response to a stimulus from the output of said first control device and emitting a second output stimulus in response to completion of the operation of said second information processing device.

35. In a data processing system, a first information entry receiving device, a second information entry receiving device, apparatus mutually responsive to said entries and proceeding progressively through character entries, and control apparatus interrupting the operation of said mutually responsive apparatus when an adjustable number of characters have been accommodated.

36. In data handling apparatus, a plurality of information receiving and delivering devices, an information interchange network linking said information receiving devices, a signal network delivering a predetermined pattern of control and information impulses to said information interchange network, and apparatus for manually controlling the advance of said signal network through said impulse pattern.

37. In data handling apparatus, a plurality of information receiving and delivering devices, an information interchange network linking said information receiving devices, a signal network delivering a predetermined pattern of control and information impulses to said information interchange network, a first continuous signal source governing said signal network, and a second non-continuous signal source alternatively governing said signal network.

38. In signal responsive apparatus; a first signal controlled combination of electric circuits sequentially passing through a plurality of mutually distinct and exclusive states in response to the application of signals thereto, a second signal controlled combination of electric circuits sequentially passing through a plurality of mutually distinct and exclusive states in response to the application of signals thereto, an electric network characterized by

a plurality of mutually exclusive states of electric equilibrium, a first circuit controlled by said first signal controlled combination for placing said electric network in a predetermined one of said states of electric equilibrium, a first control bus, a gate jointly controlled by said electric network and signals existing on said first control bus connected in operating relationship with said second signal controlled combination of electric circuits, and an electric circuit delivering stimuli to said electric network capable of transferring said network from said one predetermined state of electric equilibrium to another predetermined state of electric equilibrium.

39. In data processing apparatus; a first network including a plurality of electric circuits passing through a plurality of distinct mutually exclusive states of electrical equilibrium in response to the application of signal pulses thereto, a second electric network having at least two different states of electrical equilibrium and normally in one of said states, and an electric circuit transferring said second network from said one of said states to the other of said states in response to the establishment of predetermined conditions in said first electric network, and data transmission means controlled by said second electronic network.

40. A multiphase generator comprising a source of recurring equally-spaced pulses, a pulse generator having a plurality of outputs, means utilizing said spaced pulses for operating said pulse generator to develop sequential trigger pulses at said outputs, a plurality of square wave generators arranged to remain in one or the other of two conditions, one square wave generator being provided for each phase to be generated, certain of said outputs being connected to trigger sequentially said square wave generators to said one condition, and means utilizing certain of said outputs for sequentially triggering said square wave generators in the same order to said other condition.

41. A multiphase generator comprising a source of recurring equally-spaced pulses, a pulse generator having a plurality of output terminals, means utilizing said spaced pulses for operating said pulse generator to develop sequential trigger pulses at said terminals, a plurality of square wave generators arranged to remain in one or the other of two conditions in the absence of a trigger potential, the number of square wave generators being determined by the number of phases to be generated, certain of said terminals being connected to conduct pulses to trigger sequentially said square wave generators to said one condition, and means utilizing certain of said terminals for conducting pulses to trigger sequentially said square wave generators in the same order to said other condition.

42. In a device of the character described, an electronic accumulator, electronic carry means for each order of said accumulator, means adjustable to produce true or complement entry into said accumulator, means controlled by carry from the highest order of said accumulator and means responsive to a complement adjustment of said entry means to control said last-named means to produce an indication of the true or complement nature of a quantity in said accumulator.

43. An electronic multiplier wherein a multiplicand and a multiplier are entered into pulse responsive devices and the product of said multiplicand and multiplier is indicated by a pulse responsive result register; a pulse source, having a plurality of outputs that respectively emit different numbers of pulses during any given multiplication, for providing pulses to effect multiplication of a multiplicand by the respective digits of the multiplier; gate circuit means respectively and independently interconnecting said source and said result register and said source and said multiplicand receiving device to effect pulse entry into said result register; and sequencer circuit means electronically coupled to said multiplier receiving device for rendering, conjointly with said multiplicand receiving device, said respective gate circuit means responsive to pulses from said source in accordance with the order of the multiplier by which the multiplicand is next to be multiplied.

44. In an electronic multiplier having a multiplicand receiving device for receiving a multiplicand, a multiplier receiving device for receiving a multiplier and an arithmetic device having a plurality of orders for manifesting the product of said multiplicand and multiplier in response to pulses; a carry circuit for effecting pulse carry from a first order to a second order and including a carry trigger circuit having two stable conditions alternately assumed and set to a one of said stable conditions; a source of pulses; a buffer circuit connected between said carry trigger circuit and said second order and nonresponsive to said carry trigger circuit when it is set to said one condition; and a logical "and" gate having its output connected to said carry trigger circuit and responsive to pulses from said source to switch said carry trigger to its other stable condition to render said buffer circuit responsive to effect carry to said second order.

45. An electronic multiplier wherein each digit of a multiplier causes separate multiplication of a multiplicand and the product of that multiplication is entered directly into a device for indicating the product of said multiplicand and multiplier including a source of pulses, a cyclically operable multiplicand receiving device steppable in response to successive pulses through the different digit positions of the numerical system employed and capable of manifesting each digit of a multiplicand entered therein when stepped through the corresponding positions, first gate circuit means connected between said source and said multiplicand receiving device, a device for indicating the summation of pulses transferred thereto, second gate circuit means connected between said summation indicating device and said source, and connections joining said multiplicand receiving device and said second gate circuit means for permitting the transfer of pulses from said source to said device in response to a manifestation of each digit of said multiplicand.

46. An electronic calculator comprising a source of pulses including means for producing a plurality of pulse trains, a register, means for performing a given mathematical operation in response to two preselected numbers and entering the result thereof in said register in direct response to said source of pulses that respectively have different numbers of pulses during the mathematical operation, coincidence electronic circuits connected between said first-named means and said register for rendering said pulse trains selectively effective to actuate said register to enter said result, and electronic circuit means responsive to said source of pulses for rendering said coincidence circuits effective.

47. A read-out system for a multi-decade counter having an input circuit and an output circuit for each decade thereof, said read-out system comprising the combination of means for applying ten impulses to said input circuits, a multi-denominational read-out device operable to register amounts according to the complements of amounts entered thereinto, control devices for the various denominations of said read-out device, and means for operatively connecting said output circuits to respective ones of said control devices.

48. A read-out system for a multi-decade counter, each decade having N stable counting states, said read-out system comprising the combination of means for applying a number of impulses to each of said counter decades equal to N, a multi-denominational read-out device having a registering element in each denomination thereof, said registering element being adapted to have a count progressively advanced therein to register amounts of progressively varying values, actuating devices for advancing the count in respective ones of said registering elements in synchronism with said first mentioned means, control devices for respective ones of said registering elements, and means controlled by each of said decades upon regis-

tering a total of N stable counting states for actuating respective ones of said control devices.

49. A read-out system for a multi-decade counter having an output circuit and an input circuit for each decade thereof, said read-out system comprising the combination of means for applying ten impulses to said input circuits, a multi-denominational read-out device having a registering element in each denomination thereof, said registering element being adapted to have a count progressively advanced therein to register amounts of progressively varying values, means for advancing the count in said registering elements in synchronism with said first mentioned means, control devices for respective ones of said registering elements, and means for operatively connecting said output circuits to respective ones of said control devices.

50. In a data processor, a program device for effecting a sequence of operations for said data processor, a control register responsive to electrical signals for conditioning said program device in accordance with the content of said register to effect a corresponding set of operations for said data processor, a counter responsive to electrical signals, a circuit for advancing said counter upon operations by said data processor, means responsive to said counter for changing the content of said register to effect a sequence of operations for said data processor, and a circuit for altering the content of said register to modify said sequence of operations for said data processor.

51. In a data processor, a program device for effecting a sequence of operations for said data processor, a control register responsive to electrical signals for conditioning said program device in accordance with the content of said register to effect corresponding operations for said data processor, a storage device having a plurality of selectable positions, each position adapted to store any one of a plurality of values, a circuit for selecting one of said positions when an operation is performed by said data processor, means responsive to each selected position of said storage device for changing the content of said register to effect a sequence of operations for said data processor, and a circuit for modifying the content of said register to modify said sequence of operations for said data processor.

52. In a data processor, a program device for effecting a sequence of operations for said data processor, a control register responsive to pulses for conditioning said program device to effect said sequence of operations, a first circuit for incrementally changing the content of said register upon the performance of operations by said data processor, and a second circuit for altering the content of said register, said program device responding to an alteration of the content of said register for varying the sequence of operations effected in said data processor.

53. In a data processor, a program device for effecting a sequence of operations for said data processor, a control register responsive to electrical signals for conditioning said program device in accordance with the content of said register to effect operations for said data processor, a counter responsive to electrical signals, a circuit for advancing said counter upon the performance of operations by said data processor, and means responsive to an intermediate count of said counter for altering the content of said register.

54. In a data processor, a program device for effecting a sequence of operations for said data processor, a stepper responsive to electrical signals for conditioning said program device to effect said operations, a first circuit for advancing said stepper upon the performance of operations by said data processor, and a second circuit for transmitting a value to said stepper for altering the setting of said stepper, said program device responding to an alteration of the setting of said stepper for varying the sequence of operations effected in said data processor.

55. In a data processor, a program device for effecting a sequence of operations for said data processor, a counter responsive to electrical signals coupled to said program device, a first circuit for advancing said counter upon the performance of each operation by said data processor, and a second circuit for transmitting a signal representing a value to said counter for altering the content of said counter, said program device responding to said counter for varying the sequence of operations of said data processor in response to an alteration of the content of said counter.

56. In combination with a data processing system, a program device comprising storage means having a plurality of selectable value-storage positions, a register for registering a value, means for entering a value into said register, means responsive to the value in said register for selecting a corresponding one of said plurality of selectable storage positions, and means responsive to the value stored in the selected position of said storage means to program the operation of the data processing system.

57. Apparatus according to claim 56 wherein further means are provided for incrementally altering the content of said register.

58. In a data processor, a program device having a plurality of output lines for effecting a sequence of sets of operations for said data processor, a first register for exercising a first control of said program device, a second register for exercising a second control of said program device jointly with said first register, means for sequentially altering the content of said registers according to a plan to effect one sequence of operations in said data processor, and means for selectively modifying the content of one of said registers to modify said sequence of operations.

59. In combination, a controller for operating a data processing device to perform data processing operations, said controller including first means having a plurality of output lines for transmitting program signals to said data processing device, second means coupled to said first means for supplying pulses to said first means, a counter circuit coupled to supply signals to said first means for selecting given output lines of said first means, said first means responding to signals from said counter circuit and pulses from said second means to distribute pulses on selected output lines of said first means for operating said data processing device, and pulse responsive means for selectively altering the content of said counter circuit.

60. The apparatus of claim 59 wherein said first means includes a plurality of logical "and" circuits connected to said output lines and said logical "and" circuits are conditioned by signals from said counter circuit to pass pulses from said second means.

61. A data processing system comprising a plurality of component parts each capable of operating independently of the others and each adapted to perform an operation, an individual control unit for each said component part, a programmer including a register for storing a value therein, means responsive to the content of said register for initiating operation of a corresponding one of said control units, means for supplying signals to said programmer to incrementally alter the value in said register, and a circuit for introducing a new value into said register.

62. The apparatus of claim 61 including means in at least one of said component parts for supplying a signal to said circuit.

63. In combination, a data processor capable of performing a plurality of different operations, apparatus for repetitively performing an operation a selected number of times comprising, a first register, means coupled to said first register for setting said first register to represent a first given number, a second register settable to a second given number, a circuit for supplying signals to said data processor for performing said operation, means for changing the first given number in said first register when said operation is performed, and a circuit coupled to said first and second registers for manifesting a signal upon a pre-

determined relation being established between the number represented in said first register and the number represented in said second register to indicate the performance of said operation the selected number of times.

64. In a data handling device capable of performing a plurality of different operations, apparatus for performing a selected number of operations comprising, a counter, means coupled to said counter for setting said counter to represent a first given number, a register settable to a second given number, means for supplying stepping signals to said counter and output signals to said data handling device for performing a selected number of operations, and means coupled to said register and said counter for manifesting a signal upon an equality between the number represented in said counter and the number represented in said register to indicate the performance of the selected number of operations.

65. In an electronic data processing system, a matrix comprising a plurality of matrix information positions, a register adapted to receive pulse signals, input gating means coupling said register to said matrix to select an information position in said matrix, output coincidence gating means coupled to said matrix and having at least two inputs, said output gating means being arranged to have the energization state of a first input thereof controlled by the selected matrix information position, and pulse means coupled to a second input of said output gating means for controlling the energization state of said second input, said output gating means being operative to transmit a signal when said first and second inputs thereof are at given energization states respectively.

66. In an electronic data processing system, memory means having both data and program information stored therein, a single register for receiving and storing information signals, and signal responsive gating means coupling said register to said memory means for producing signals indicative of either data or program information from said memory means in dependence upon the informational content of the signals stored in said register.

67. In a data processing machine, memory means having both data items and program items stored therein, said memory means having a plurality of logical "and' circuits associated respectively with said stored items, pulse responsive register means for receiving addresses to enable selected ones of said "and" circuits thereby to read out selected items stored in the memory means, and output means for transmitting each selected item from said memory means.

68. In a data processing system, memory matrix means for storing a plurality of data items, said matrix means having input lines and output lines, an input register, pulse responsive means for selectively storing information signals in said register related to at least one of said stored data items, means for producing control pulses, means responsive to at least one of said control pulses and further responsive to the information signals stored in said register for energizing at least one of said input lines to select at least one of said stored data items, and output means for transmitting said selected data items via at least one of said output lines.

69. In a data processing system, memory means storing a plurality of data items, register means, means for selectively feeding input signals to said register means, signal modifier means coupled to said register means for altering signals in said register means in a succession of steps, and control means coupling said register means to said memory means and responsive to the successively changing contents of said register means for transmitting signals corresponding to a succession of said stored data items out of said memory means.

70. In a data processing system, static memory means storing a plurality of data items, pulse responsive means for receiving an argument and thereafter selecting a data item corresponding to the argument received and thereafter altering said selection in a succession of steps, and means responsive to the successively changing selection of said data items for transmitting signals corresponding to the selected data items out of said memory means.

71. In a control system, a register having first and second groups of stages, input means for selectively storing signals in selected stages of said first and second groups of stages, a gating matrix comprising a plurality of gating means each of which has at least first and second control lines, coupling means for coupling said first group of register stages to selected ones of said first control lines respectively and coupling said second group of register stages to selected ones of said second control lines respectively, said coupling means being normally inoperative to feed signals from at least one register stage group to its associated gating control lines, and signal control means coupled to said normally inoperative coupling means for selectively rendering said coupling means operative, whereby to transmit signals from said register stages to said gating control lines thereby to open selected ones of said gating means in accordance with the signal contents of said register stage groups.

72. Means for producing electric pulses to represent items of quantitative information, means for producing further pulses to represent items of control information, memory means having items of information stored therein, register means, first control means responsive to said quantitative information pulses for storing data in said register means, second control means jointly responsive to said control information pulses and to the data stored in said register means for selecting a particular one of the items of information stored in said memory means, and output means responsive to said selected item of information for producing a pulse output characteristic of said selected item.

73. In a control system, first signal means having an output, second signal means having an input, selectively enabled transmission means for transferring signals from the output of said first means to the input of said second means, a flip flop having set and reset inputs, said flip flop having an output adapted to enable said transmission means upon occurrence of a control signal at said flip flop set input, a source of spaced control pulses, normally disabled gating means coupling said control pulse source to the reset input of said flip flop, means coupling said flip flop output to said gating means to enable said gating means along with said transmission means upon occurrence of a control signal at said flip flop set input, and means for selectively applying a control signal to said flip flop set input thereby to enable said transmission and gating means for a limited period of time automatically terminating when the next subsequently occurring one of said control pulses resets said flip flop.

74. A device having a plurality of static storage locations, a transmission system fed by said storage locations; control means, including an address register means settable to selected addresses by numerically coded signals, for supplying signals to said storage locations to select among such storage locations, in accordance with the numerical content of said address register, a one of said storage locations for reading the data stored in the selected storage location out to said transmission system; and an arithmetic device for supplying numerically coded signals to said address register to set said address register for selecting a one of said storage locations.

75. A device having a plurality of storage locations, a transmission system coupled to said device, control means including an address register for supplying informational signals to said device and being operative to select among such storage locations, in accordance with the informational content of said address register, at least one of said storage locations for reading the data stored in the selected storage location out to said transmission system, said control means including circuits for selectively modifying by a chosen amount the informational content

of said address register thereby to selectively read data from different ones of said storage locations.

76. A device having a plurality of storage locations, control means including an address register for supplying signals to said device and operative to select among such storage locations, in accordance with the numerical content of said address register, a one of said storage locations for reading out a predetermined portion of the data stored in the selected storage location, means coupling said device to said address register, input means for supplying numerically coded signals to said address register to set said address register for selecting a one of said storage locations, and an arithmetic device for providing numerically coded signals to said input means.

77. A device having a plurality of memory storage locations, a transmission system coupled to said memory storage locations, control means having an address register for supplying signals to said memory storage locations to select among such memory storage locations, in accordance with the numerical content of said address register, a one of said memory storage locations for reading the data stored in the selected memory storage location out to said transmission system, said control means including a program ring, and a device settable to a numeric value for reading data out of the selected memory storage location to said transmission system until a predetermined relationship exists between said program ring and said settable device.

78. A data handling device including storage means having a plurality of storage devices, each storage device including means for storing data therein, addressing means coupled to said storage means for extracting data stored therein, first input means for supplying address signals to said addressing means, and second input means coupled to the addressing means for supplying signals to modify selectively the address so as to read sequentially from selected storage devices in the storage means.

79. In a data processing system, memory means having at least first and second portions, said first memory means portion having data stored therein characteristic of predetermined functions respectively of a first plurality of possible arguments, and said second memory means portion having control information stored therein characteristic of predetermined program operations respectively to be initiated by a second plurality of possible arguments, a pulse responsive argument register for receiving and storing an argument, and pulse responsive gating means coupling said register to both of said memory means portions for producing an output signal from a selected one or the other of said memory means portions in dependance upon whether the argument stored in said register is one of said first or of said second plurality of possible arguments.

80. In a data processor, a storage device for storing and making readily available any one of a plurality of values stored therein comprising, a settable element for each value to be stored, means for setting said elements to store a plurality of values, electrical circuits for uniquely associating each of said values with a tag value, a tag register for receiving and registering sets of coded tag signals, a source of coded tag signals, means for transmitting sets of coded tag signals to said tag register, circuits responsive to said tag register for reading the value associated with the registered tag from said storage device during a time interval wholly independent of the value of said registered tag, and means for incrementally altering a tag value transmitted to said tag register.

81. A data input device to be used with a data processing system which employs a data bearing medium, comprising reading means for reading data from a data bearing medium, encoding means including a plurality of elements each of which has a weighted value for a particular code and at least two of which have different weighted values, control means connecting said reading means to said encoding means to activate one or more of said elements in response to a signal from said data bearing medium thereby encoding the data from said data bearing medium into said particular code, said encoding means including means for converting its output into pulses conforming to said code, and data processing means for receiving said pulses and performing a data processing operation thereon.

82. In a data processing system, the combination of reading means to accept data to be processed, intermediate storage means coupled to said reading means to receive data therefrom and temporarily store said data in the form of electrical signals according to data segments wherein each data segment has the same number of order positions, pulse generating means connected to said intermediate storage means to generate one or more pulses in response to data segments stored therein, the pulse or pulses generated in response to each segment being representative of a numerical value of the segment, and data processing means for receiving said pulses and performing a data processing operation thereon.

83. In a data processing system, the combination of reading means to accept data for processing, temporary storage means connected to said reading means to receive at speeds below electronic speeds and temporarily store data in the form of electrical signals from said reading means as well as to read-out the stored data in pulse form at electronic speeds, pulse responsive data processing means connected to said temporary storage means to receive data in pulse form therefrom at electronic speeds and to process such data at electronic speeds, further temporary storage means for receiving the processed data at electronic speeds from the pulse responsive data processing means, and output means for receiving the stored data in said further temporary storage means and producing an indication of the result of the processing operation at speeds below electronic speeds.

84. A data processing system as defined in claim 83 having a plurality of reading means together with a plurality of said first-named temporary storage means, pulse operated selection means for selecting among said first-named temporary storage means, and program means for the system for providing program pulses to the various parts of the system in a desired sequence.

85. A data output device to be used with a data processing system, comprising recording means for recording data on a data bearing medium at speeds below electronic speeds, signal generating means to process data at electronic speeds, transfer means coupling said signal generating means to said recording means to enable only certain of said data signals to pass to said recording means, control means coupled to said transfer means to selectively activate said transfer means, said control means being connected to receive output signals from said data processing system, and inter-locking means coupled to said control means to enable said output signals to be received by said control means only after said recording means has recorded the data which had been previously held by said transfer means.

86. In a data processing system, a data input device comprising means for reading data from a data bearing medium; means for temporarily storing said data for use by said data processing system in data processing operations, logical "and" circuits coupled to said temporary storing means and responsive to control pulses supplied by said data processing system for selectively transmitting said temporarily stored data to said data processing system in pulse form, first signal generating means responsive to operation of said reading means for generating a signal indicating that data has been read from said data bearing medium; said data processing system including second signal generating means for generating a signal which indicates that a given data processing operation has been terminated; and control means coupled to both said first and second signal generating means and jointly responsive to occurrence of signals from both said first and second

signal generating means for enabling a further operation in said data processing system.

87. A data processing system comprising a first data retention device adapted to transmit signals at a first rate, a second data retention device adapted to receive signals in pulse form at a second rate, said second rate being substantially higher than said first rate, an intermediate storage device coupling said first data retention device to said second data retention device including means for converting the data into pulse form, transfer and control means operably associated with said intermediate storage device for rendering said intermediate storage device receptive to receive signals from said first data retention device at said first rate and to transmit said received signals to said second data retention device at said second substantially higher rate, and data processing means for receiving said pulses and performing a data processing operation thereon.

88. In a data processing machine, a pulse responsive central processor operating under control of a first timer at a first rate, a peripheral data handler operating under control of a second timer at a second rate, storage means for temporarily storing data, means under control of said first timer for transferring data between said storage means and said central processor at said first rate, and means under control of said second timer for transferring data between said storage means and said peripheral data handler at said second rate, whereby said central processor and said peripheral data handler are made compatible, said storage means and central processor each including means to effect transfers therebetween in pulse form.

89. A data processing machine comprising, memory means for storing data to be processed, reading means for reading said data from said memory means and for converting the data into pulse form, a multiplicity of interconnected pulse responsive processing units for producing output pulses representative of the results of a processing operation, at least one of said units being connected to said reading means to receive the pulses emitted by the reading means, and printing means connected to at least one of said units for printing the results of said processing operation.

90. Apparatus comprising pulse responsive storage means having a plurality of orders for storing received pulses and including output means for transmitting the contents of said storage means; at least two groups of input means, each of said groups coupled to said storage means for the transfer of pulses thereto; an information signal producing unit for each of at least two of said groups of input means, each of said units adapted to emit pulses in response to a signal; means for and operatively associated with each of said groups to selectively activate one of said groups including signal responsive control means to enable a selected one of said groups of input means; and sequencing means adapted to provide a signal to a selected one of said control means and to the selected one of said units associated with the selected control means to effect the transfer of pulses to said storage means in accordance with a desired routine and thereafter to provide a finish signal when said transfer has been effected.

91. In a computer, pulse responsive means for solving arithmetic problems at electronic speeds and having a plurality of inputs each for respectively receiving pulses representing numbers, said inputs having logical "and" circuits for controlling entry thereto of pulses from a plurality of different sources, and pulse operated program means for selectively operating said logical "and" circuits to enable reception on the different inputs from said different sources respectively.

92. A computation control circuit comprising means for producing pulses at a radio frequency rate to represent quantitative data, means for producing control pulses, computation means for selectively performing an arithmetic operation in a sequence of steps, means for feeding said quantitative data pulses to said computation means, and means responsive to said control pulses for controlling the step sequence of said arithmetic operation performance.

93. In a data processing system, first and second memories each including plural orders, data transfer means for interrogating the first memory with pulses and transmitting its contents in pulse form to the second memory, said data transfer means including means for effecting a multiplicity of transfers from the first to the second memory, and counter means for counting the data transfers effected by said data transfer means and for terminating the transfer operations.

94. In a data handling system, utilization means, a plurality of data sources, signal transfer means linking said sources to said utilization means, a selector means for rendering a preselected one of said sources effective to transfer data to said utilization means, a counter means for counting the number of data transfers from said selected source to said utilization means, and a control circuit operatively coupled to said counter means and further coupled to said selector means to terminate transfers from said selected source after a predetermined number of such transfers and to switch a different one of said sources to said utilization means.

95. A data handling system as defined in claim 94 in which said utilization means comprises two separate memories, each data source feeding a separate one of said memories.

96. In a multipurpose computer, a multiplicity of pulse responsive units each having an input and an output, at least one unit including means for performing an arithmetic computation on two pulse signals received at a radio frequency rate at its input, said unit including means operative to develop pulse signals at a radio frequency rate at its output to represent the computed result; a source of input data including means for reproducing the input data in the form of pulse signals at a radio frequency rate, program means for routing the pulse signals from said source and from the output of at least one of said units to the inputs of the units in a selected order to cause a sequence to be selected for a particular problem, and output means responsive to the computed result.

97. An assemblage comprising an arithmetic device responsive to a data read-in signal for receiving arithmetical data manifestations and responsive to a read-out signal for reading out a computed result manifestation, cycling means for sequencing the arithmetic device through an operation and circuits producing a complete signal at the end of the operation, a plurality of registers comprising numerical data manifestation storage means responsive to an input signal for receiving data manifestations, means connecting a selected one of said registers to said arithmetic device for the transfer of data manifestations to said arithmetic device, means conecting said arithmetic device to a selected one of said registers for transfer of data manifestations to said selected one of said registers, selectively conditioned control means including a first circuit to produce said read-in signal to transfer data manifestations from a selected one of said registers to the arithmetic device and a second circuit responsive to said complete signal to produce said read-out and input signals to transfer the computed result from the arithmetic device to a selected one of said registers, both of said first and second circuits responsive to said cycling means, and automatic sequencing means including a source of program pulses conditioning said assemblage.

98. An electronic multiplier wherein a multiplicand and a multiplier are entered into pulse responsive devices and the product of said multiplicand and multiplier is indicated by a pulse responsive result register; a pulse source, having a plurality of outputs that respectively emit different numbers of pulses during any given multiplication, for providing pulses to effect multiplication of a multiplicand by the respective digits of the multiplier;

gate circuit means respectively and independently interconnecting said source and said result register and said source and said multiplicand receiving device to effect pulse entry into said result register; and sequencer circuit means electronically coupled to said multiplier receiving device for rendering, conjointly with said multiplicand receiving device, said respective gate circuit means responsive to pulses from said source in accordance with the order of the multiplier by which the multiplicand is next to be multiplied.

99. In a computing apparatus, pulse operated computing means including first and second pulse operated registers in which answers to computations performed by said means are temporarily stored, a multiplier matrix producing partial product values in a predetermined number system, apparatus impressing the contents of said first and second storage registers on said multiplier matrix, and means for combining the resultant partial products.

100. A data processing machine comprising first and second means for manipulating two number quantities for division of one as a numerator and the other as a denominator, each number having a plurality of orders, and program means for controlling the production of a quotient of said two quantities, said programming means including means for subtracting the denominator value from the numerator value until an overdraft occurs, sign indicating means for producing a sign signal indicative of the sign of the remainder, means responsive to said sign signal for shifting the remainder and denominator relative to each other so that the denominator is less than the remainder, means for adding the shifted remainder and denominator until a second change in sign of the result occurs to produce a sign signal responsive to the change in sign of the remainder, means activated by said signal for again shifting the remainder and denominator relatively so that the denominator is again the smaller and subtracting it from the remainder, and means for signalling the number of times each addition and subtraction is performed.

101. A data processing system comprising, a data processing device for calculating first and second arithmetic functions each in successive steps of operation on data signals to provide result signals which are the combination of partial result signals of the steps of operation, a controller for said device for causing the device to alter the partial result signal by a first constant value signal when in a first state for calculating said first arithmetic function and a second constant value signal when in a second state for calculating said second arithmetic function so that result signals have a different arithmetic relationship to the data signals which is dependent upon the constant value signals, and means for selectively setting said controller to a selected one of the states.

102. A data processing system comprising, a data processing device, including program means for stepping said device through a series of operations, an external source of control signals, said data processing device having interlock means coupling said source and said device for receiving said control signals and being responsive thereto for enabling said device to effect a particular operation, and means for selectively disabling said interlock means preventing interruption of said series of operations of said device.

103. A data processing system comprising, a problem-solving device for performing a series of problem-solving steps according to a predetermined plan, including interlock means for selectively interrupting said plan at a predetermined step, means for manifesting a control signal, means supplying said control signal to said interlock means, said interlock means being responsive to said control signal for conditioning said device to resume said plan and selectively operable means for enabling the operation of said device according to the plan without interruption by said interlock means.

104. A data processing system comprising: a processing device including program means for operating said processing device according to a predetermined plan, status means indicating a predetermined state of said program means, means providing a control signal, interlock means for receiving and manifesting said control signal when selected and responsive jointly to said status means when indicating a predetermined state and to said manifested control signal to control a change in the state of said program means, and settable means for selecting said interlock means.

105. Data processing apparatus comprising means providing a first program signal, means providing a second program signal, means for storing said first and second program signals, selectively operable priority circuit means for providing, when operated, a control signal when conditioned by said means storing first and second program signals, and when not operated, providing a control signal irrespective of said conditioning, and settable means for operating said priority circuit means.

106. A system including at least first and second data processing devices comprising means providing a first program signal from said first device, means providing a second program signal indicative of an interruption at a predetermined step in a routine of operations of said second data processing device, means for storing said first and second program signals, selectively operable priority circuit means for providing a control signal when conditioned by said means storing first and second program signals and when not operated providing a control signal irrespective of the conditioning, means providing said control signal to said second data processing device to resume said routine of operations, and means for operating said priority circuit.

107. A circuit for generating proceed signals between operating data processing devices, a control bistable device, a first data processing device having means for setting said bistable device to one state to indicate that said first data processing device has produced a first control signal, means for manifesting a second control signal indicative that another data processing device has completed a predetermined portion of a sequence of operations, means selectively responsive to said bistable device in said one state and said means manifesting a second control signal to set said bistable device to the other state and generate a proceed signal, and means for conditioning the last-mentioned means to provide the proceed signal irrespective of the second control signal being manifested.

108. A data processing system comprising a plurality of data processing devices, circuits for interconnecting said devices according to a program plan for exchanging program control pulses, means in one of said devices for selectively disabling the device in solving a particular problem beyond a predetermined problem solution state or permitting the device to proceed beyond said state, means in another of said devices for manifesting a control signal, and means included in said circuits for transmitting said manifested control signal to said one of said devices to enable said one of said devices to proceed after having been disabled.

109. In combination, first and second pulse responsive storage means for storing manifestations of data, a plurality of gating means having one input thereto connected to said first storage means and a second input thereto connected to said second storage means, means connecting the outputs of said gating means together such that a first program signal is produced when the data in said first storage means is similar in some characteristic to the data in said second storage means and for producing a second program signal when the data in said first and second storage means is dissimilar in said characteristic, and a control circuit responsive to said first program signal for initiating one type of arithmetic process and responsive to said second program signal for initiating another type of arithmetic process.

110. In a data processing system a sequence control

comprising a bistable device set in a first state, gating means coupled to said bistable device and conditioned thereby to emit control pulses to perform a sequence of operations, counting means coupled to said gating means for receiving pulses indicative that a predetermined operation has been performed and manifesting an indication thereof, settable means manifesting an indication of a desired number of operations to be performed, means coupled to said counting means and to said settable means and responsive thereto to detect a predetermined condition between said manifestations, and means responsive to a detection of said condition for changing the state of said bistable device from said first state to an other state to terminate the sequence of operations and begin a sequence of operations other than said first sequence.

111. In computing apparatus, a plurality of pulse-operated registers, pulse operated computing means including first and second ones of said registers in which answers to two different computations performed by said means are temporarily stored, pulse operated dividing means for dividing the value in the first register by the value in the second register including means for storing the quotient in one of said plurality of registers, and means for transmitting the contents of said last-named register out in pulse form for further computation.

112. In combination, a data processor comprising a plurality of component parts, a source of recurrent timing signals, a bi-stable circuit settable to either a first or a second condition and having input and output terminals, a coincidence circuit having at least first and second input terminals and an output terminal, a circuit for coupling said first input terminal to said source of recurrent timing signals, a circuit for coupling said second input terminal to the output terminal of said bi-stable circuit to condition said coincidence circuit to pass a signal from said source to the output of said coincidence circuit when said bi-stable circuit is set to said first condition, a circuit for coupling the output terminal of said coincidence circuit to an input terminal of said bi-stable circuit to set said bi-stable circuit to said second condition, a circuit for coupling the output terminal of said coincidence circuit to said plurality of component parts to advance said data processor through a predetermined number of steps for each timing signal appearing on the output of said coincidence circuit, and means for setting said bi-stable circuit to said first condition.

113. Apparatus according to claim 112 wherein said last-named means comprises manually operable means to produce a signal for setting said bi-stable circuit to said first condition.

114. Apparatus according to claim 112 wherein said last-named means comprises means in one of said component parts for transmitting a signal to set said bi-stable circuit in said first condition.

115. In combination, a data processor comprising a plurality of component parts, a source of recurrent timing pulses, first means for transmitting timing pulses from said source to said plurality of component parts to advance said data processor through a series of operations, means for disabling said first transmitting means, and manually operable second means for transmitting only a predetermined number of said timing pulses to said plurality of component parts upon operation of said second means.

116. In a data processing system, data processing means having a data input and data output and controlled by timing pulses, and means for supplying the timing pulses continuously for normal operation and including means to selectively provide either a first predetermined or a second predetermined number of pulses for test purposes.

117. In a data processor having a plurality of component parts and means for providing groups of pulses and feeding at least some of these pulses to said component parts to pace said component parts through their respective operations, first means operable to enable said providing means to automatically provide a plurality of said groups in succession for normal data processing operations, and second means operable to enable said providing means to provide only a predetermined number of said pulses from a single group for test purposes.

118. In a data processor having a plurality of component parts and means for providing groups of timing pulses for said component parts to pace said component parts through their respective operations under control of selectively applied control signals wherein said timing pulses are arranged in groups comprised of signals having respective significance in said data processor, means operable to enable said providing means to automatically provide a plurality of said groups in succession for normal data processing operations, and manually operable means for selectively enabling said providing means to provide a single group or a single pulse of a group upon the operation of said manually operable means.

119. In a data processor having a plurality of component parts, a source of recurrent timing pulses, a distributor for arranging said pulses in groups and for distributing certain of said pulses to certain of said component parts, and manually operable means for transmitting a single pulse to said distributor.

120. In a data processor having a plurality of component parts, a source of recurrent pulses, a distributor for arranging said pulses in groups and for distributing certain of said pulses to certain of said component parts, a first circuit for transmitting pulses from said source to said distributor to automatically pace said data processor through successive operations, means for disabling said first circuit, manually operable means, and a second circuit responsive to the operation of said manually operable means for transmitting a predetermined number only of said pulses to said distributor.

121. In a data processor, a plurality of component parts, a source of recurrent timing pulses, a distributor for arranging said pulses in groups comprised of pulses having respective significance in said data processor and for distributing certain of said pulses to certain of said component parts, a first circuit for transmitting pulses from said source to said distributor to automatically pace said data processor through successive operations, means for disabling said first circuit, manually operable means, and second circuit means responsive to the operation of said manually operable means for selectively transmitting either a single pulse or a predetermined plurality of pulses to said distributor.

122. A data processing system having a plurality of component parts intercoupled to perform given manipulations on data signals comprising, means for providing pulse signals in sequence and in definitive groups, means selecting certain of said pulses and distributing said pulses among at least some of said component parts for causing the latter to perform said manipulations in a series of operations, means providing data signals to said component parts to be operated, means operably associated with at least some of said component parts to indicate the condition of portions thereof, and means for sequencing said parts in incrementals steps to greatly increase the time intervals between certain steps for test purposes.

123. In combination, a data processor comprising a plurality of bi-stable circuit elements, a power supply therefor, a signal generator coupled to said power supply and responding thereto when the same is brought into operation to generate a signal, and means feeding said signal to said plurality of bi-stable circuit elements to preset said elements to a reference condition.

124. In a data processor, a storage means for storing digital information, an arithmetic circuit means, a programming means for controlling the transfer of information signals between said storage means and said arithmetic means, at least one of said means including a plurality of bi-stable circuit elements, a clearing signal gen-

erator for generating a signal of fixed duration upon actuation, a manually operable switching means for actuating said clearing signal generator, and means for feeding said clearing signal to said bi-stable circuit elements to preset said elements to a reference condition.

125. In a data processor, a storage means for storing values, an arithmetic circuit means, a programming means for controlling the transfer of informatian signals between said storage means and said arithmetic means, said programming means including, a recurrent pulse source, a pulse distributor network having a plurality of output terminals coupled thereto and having a cycle of operation which comprises a plurality of steps, means coupling said pulse source to said distributor to advance said distributor through its steps of operation one step for each pulse applied from said source, each of said output terminals being adapted to be energized in response to a different step of the distributor operation, a gate control circuit comprising at least one bi-stable circuit the inputs to which are coupled to different outputs from said distributor whereby said bi-stable circuit can be set from one distributor output and reset from a second distributor output, and an output terminal coupled to said bi-stable circuit operative to provide a control signal for the data processor when said bi-stable circuit is in a particular one of the two possible conditions.

126. In a data processor, a storage means for storing values, an arithmetic circuit means, a programming means coupled to said storage means for controlling the transfer of value signals between said storage means and said arithmetic means, said programming means including, a recurrent pulse source, a pulse distributor network having a plurality of output terminals coupled thereto and having a cycle of operation which comprises a plurality of steps, means coupling said pulse source to said distributor to advance said distributor through its steps of operation one step for each pulse from said source, each of said output terminals being adapted to be energized in response to a different step of the distributor operation, a digit generator coupled to at least one output from the said distributor for generating a predetermined value representing signal, and means in said data processor for utilizing said value representing signal during the operation of the data processor.

127. In a data processor, storage means for storing values, arithmetic circuit means, programming means coupled to said storage means for controlling the transfer of information signals between said storage means and said arithmetic means, said programming means including, a recurrent pulse source, a plurality of bi-stable elements connected in cascade to form a multi-stage shift circuit, said shift circuit being arranged to support a predetermined signal condition in only one stage at a time, said shift circuit further including a shift line to which an output from said source is applied for successively shifting said predetermined signal condition down the shift circuit one stage at a time in response to each successive pulse from said source, a plurality of coincidence circuits, each including at least two input terminals and one output terminal, means connecting a first terminal of each of said coincidence circuits to an output from said source, means connecting a second input terminal of said coincidence circuits to different stages in said shift circuit whereby each of said coincidence circuits passes a pulse from said source to its output terminal whenever the corresponding stage of the shift circuit is set to said predetermined signal condition, means combining the outputs of selected coincidence circuits onto a first signal output line to produce a selected pulse pattern, and means in said data processor for utilizing said pulse pattern during the operation of the data processor.

128. In a data processor, a source of recurrent pulses, a pulse distributor network having a plurality of output terminals coupled thereto and having a cycle of operation which comprises a plurality of steps, means for applying pulses from said pulse source to said distributor to advance said distributor through its steps of operation one step for each pulse applied from said source, each of said output terminals adapted for energization in response to a different step of the distributor operation, a mixer having a plurality of inputs each coupled to a particular group of different successive outputs from said distributor, an output for said mixer for manifesting the signals applied to said mixer from said distributor, and means in said data processor for utilizing the signals manifested at said output of said mixer.

129. In a data processing system, electrical data processing means having an input for receiving information to be processed, said electrical data processing means being responsive to discrete signals meeting a predetermined standard required for reliable operation, which standard includes the requirement that individual signals be shorter in time than a predetermined limit, a source of information in the form of discrete signals to be processed by said electrical data processing means, a transmission link coupling said source to said data processing means, and means for shaping the signals received at said input from said link to conform to said standard prior to further use in data processing operations.

130. In a data processing machine, pulse responsive computing means comprising plural elements each settable to either of two stable states in response to applied pulses, said computing means having a construction requiring that actuating pulses applied thereto meet a predetermined standard in order to insure reliability of the computation, means for producing pulses for setting said elements including an electrical transmission circuit having constants that may distort the pulses to a shape outside of said predetermined standard, and means in said electrical transmission circuit for shaping the pulses therein to meet said standard.

131. Apparatus according to claim 8 wherein said means to establish a selective relation includes manually operable switching means.

132. Apparatus according to claim 8 wherein said means to establish a selective relation includes manually settable plug wires for establishing certain desired connections between units.

133. Apparatus according to claim 8 wherein said means to establish a selective relation includes pulse operated means for automatically establishing the selective relation.

134. Apparatus according to claim 8 wherein said means to transmit a control pulse is effective on said predetermined units through a direct connection thereto.

135. Apparatus according to claim 8 including a program device and wherein said means to transmit a control pulse is effective on said predetermined units through the medium of said program device responding to said control pulse to in turn control said intercommunication.

136. Apparatus according to claim 8 wherein said pulse responsive units employ vacuum tubes to generate and respond to pulses for performing the computing operations.

137. Apparatus according to claim 8 wherein the construction to receive numeratively numbers pulses is that particular construction to receive numeratively in the scale of ten.

138. Apparatus according to claim 8 wherein the construction to receive numeratively numbers pulses is that particular construction to receive numeratively in which each step of the numeration includes the reception of a separate value.

139. Apparatus according to claim 8 wherein the construction to receive numeratively numbers pulses is that particular construction to receive numeratively in which each step of the numeration includes the reception of a separate value represented by a number of pulses corresponding to the value received in a given order.

140. Apparatus according to claim 8 wherein the construction to receive numeratively numbers pulses is that particular construction to receive numeratively in which the numeration is the reception of at least two separate numbers constituting different orders of the complete numbers.

141. In a data processing system, a multiplicity of pulse responsive units constructed to transmit pulses representing numbers upon stimulation by one control pulse and to receive pulses representing numbers upon stimulation by another control pulse, and means to transmit to said units control pulses and numbers pulses in a correlated order including programming means for establishing a selective relation between certain control pulses and certain predetermined units, said units being so constructed that transmission of pulses between units according to a program of said programming means performs arithmetic operations, said programming means including means responsive to the completion of an arithmetic operation so performed to transmit a control pulse effective on predetermined units for intercommunication of pulses representing numbers between one an another of said units.

142. Timing mechanism for a data processing machine comprising a source of equally spaced signals occurring at a predetermined repetition rate and each having a predetermined accurately determined duration, a stepping circuit having a plurality of stages and adapted to be stepped through said plurality of stages in a predetermined pattern, means for applying said signals to said stepping circuit to step said stepping circuit, a coincidence circuit having first and second inputs and an output, means connecting one of said stages to said first input, and means connecting said source to said second input thereby to manifest signals of said accurately determined duration at a frequency bearing a relation to said predetermined repetition rate as determined by said stepper.

143. Apparatus according to claim 37 wherein said interchange network includes a bi-stable device associated with each of said information receiving and delivering devices.

144. Apparatus according to claim 37 wherein said second non-continuous signal source selectively conditions said bi-stable devices to bring into operation the selected one of said information receiving and delivering devices.

145. In a program-controlled data processing system, means for performing a data processing operation in accordance with a sequence of program steps, data storage means, means for reading data from said data storage means, first signal generating means coupled to said reading means for selectively generating and maintaining a persistent first control signal indicating that data has been read from said data storage means; second signal generating means selectively generating and maintaining a persistent second control signal which indicates that a program step has been completed by said first-named means; control means coupled to both said first and second signal generating means and responsive to occurrence of both said first and second control signals for generating a third control signal operative to initiate a further program step, and means coupled to said first and second signal generating means for terminating both said first and second persistent control signals in response to the generation of said third control signal.

146. In an electronic computer, means for producing intermittent frames of pulses, pulse responsive arithmetic means timed by said pulses and operative to perform a plurality of sub-problems at least one during a definite number of frames and another during an indefinite number of frames, said arithmetic means including means to produce a control pulse that signals the completion of each sub-problem, and program means responsive to said control pulses to join said sub-problems together into a main routine.

147. In a data processing system, a plurality of data sources each adapted to deliver data for use in said system, a bi-stable device associated with each of said sources, signal responsive means for setting said bi-stable devices to a first state, means responsive to each said bi-stable device when set in said first state for operating its associated data source to deliver data to said system, means for setting each bistable device set to said first state to a second state upon completion of operation of its associated source, and program means for selectively supplying signals to said signal responsive means.

148. A data storage system for a data processing machine comprising pulse generating means for generating pulses to coordinate the operation of said machine, a plurality of settable elements, means for setting said elements into patterns to thereby store data, a transmission line for transmitting certain of said pulses to said elements, said plurality of settable elements including means controlled jointly by said certain pulses and the settings of said elements to manifest signals indicative of the data stored, a bi-stable device connected to receive said signals and responsive thereto to change its stable state in accordance with said signals, and a gate controlled by said bi-stable device for selectively transmitting other of said pulses for processing by said machine.

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